TQP9418

High Linearity 0.5 W Small Cell PA

Product Overview

The TQP9418 is a high-linearity two-stage power amplifier in a low-cost surface-mount package with on-chip bias control and temperature compensation circuits, suitable for small cell base station applications.

TQP9418 provides 30 dB gain and +27 dBm linear power over the 1805 – 1880 MHz frequency range. The amplifier is able to achieve −48 dBc ACLR at +27 dBm output power using 20 MHz LTE signal.

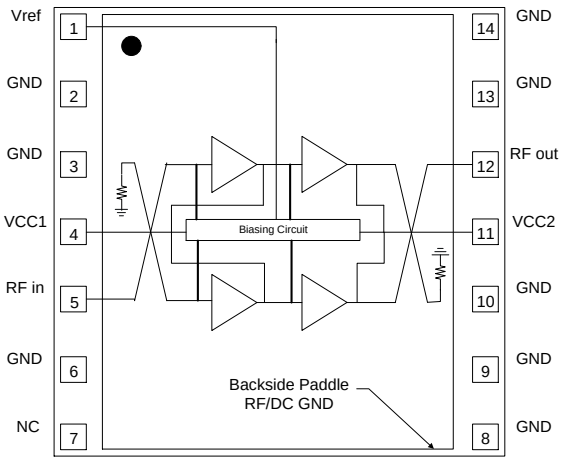
The TQP9418 integrates two high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized. The TQP9418 is available in a 7 x 7 mm surface mount package.

7 mm x 7 mm leadless SMT Package

Key Features

- 1.805 – 1.88 GHz Frequency Range
- Fully Integrated, 2 Stage Power Amplifier
- Internally Matched 50 Ω Input/Output
- −48 dBc ACLR at Pavg = +27 dBm
- 31 dB Gain
- 14.5% PAE at +27 dBm
- 420 mA Quiescent Current
- On-chip Bias Control and Temp. Comp. Circuit

Functional Block Diagram



Top View

Applications

- Small Cell / Picocell
- Enterprise Femtocell
- Customer Premises Equipment (CPE)
- Data Cards and Terminals
- Distributed Antenna Systems (DAS)
- Booster Amps, Repeaters

Ordering Information

Part No.	Description
TQP9418	High Linearity 0.5 W Small Cell PA
TQP9418-PCB	1805 – 1880 MHz Evaluation board

Standard T/R size = 2500 pieces on a 13" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150 °C
Supply Voltage (V_{CC})	+6 V
V_{ref}	+3.5 V
RF Input Power, CW, 50Ω, T=25˚C	+13 dBm
Tj at T_{CASE} = 125°C	+205°C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC1}, V_{cc2}	+3.6	+4.5	+5.25	V
V_{ref}	+2.75	+2.85	+2.95	V
T_{CASE}	−40		+85	°C
Tj at T_{CASE} max			+165	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

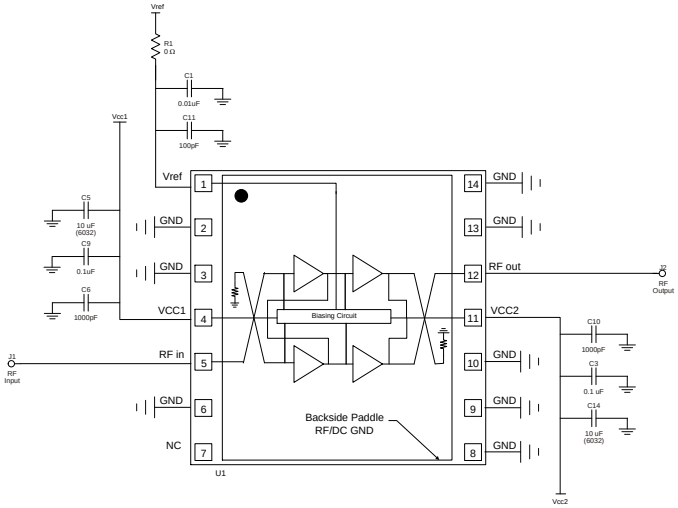
Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +4.5 V, Vref = +2.85 V, Temp= +25 °C

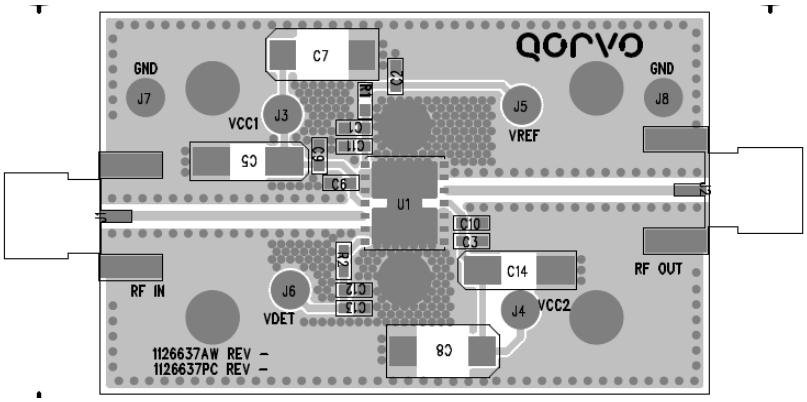
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1805		1880	MHz
Test Frequency			1840		MHz
Gain		28	31	34	dB
Input Return Loss		15	20		dB
Output Return Loss		15	25		dB
P1dB			36		dBm
ACLR	P_{OUT} = +27 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR		−48	-45	dBc
ACLR	P_{OUT} = +27 dBm, 2X20 MHz LTE E-TM1.1, 9.5dB PAR		−41		dBc
ACLR	P_{OUT} = +27 dBm, 15 MHz LTE E-TM1.1, 9.5dB PAR		−50		dBc
ACLR	P_{OUT} = +27 dBm, 10 MHz LTE E-TM1.1, 9.5dB PAR		−49		dBc
ACLR	P_{OUT} = +27 dBm, 5 MHz LTE E-TM1.1, 9.5dB PAR		−47.5		dBc
Power Added Efficiency	P_{OUT} = +27 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR	13	14.5		%
Quiescent Current, I_{CQ}	V_{CC1} + V_{CC2}	330	420	510	mA
Leakage Current	V_{CC} = +4.5V, V_{ref} = 0V		13	19.5	µA
Reference Current , I_{ref}	Temp = -40°C to +85°C, V_{ref} = +2.85V		3	10	mA
Operational Current, I_{CC}	Pout = +27 dBm		680	920	mA
Switching Speed	Rise time (10%-90%)		670		ns
	Fall time (90%-10%)		1205		ns
Spurious Output Level	Pout ≤ +27dBm, In & Out of band load VSWR ≤ 10:1		−60		dBc
VSWR survivability	No permanent degradation or failure	10:1			-
Harmonics	$2F_0$ (Pout = 27 dBm), CW signal		−42	−37	dBc
	$3F_0$ (Pout = 27 dBm), CW signal		−58	−53	dBc
	$4F_0$ (Pout = 27 dBm), CW signal		−68	−63	dBc
Thermal Resistance, θ_{jc}	Module (junction to case)			18.5	°C/W

Parameter	Conditions	-40°C	+25°C	+85°C	Units
Gain	Small Signal	33	31.3	29.6	dB
ACLR	P_{OUT} = +27 dBm, 20 MHz LTE E-TM1.1, 9.5dB PAR	-51	-49	-47	dBc
PAE	P_{OUT} = +27 dBm, 20 MHz LTE E-TM1.1, 9.5dB PAR	15.5	14.5	13.5	%
P1dB		+35.6	+36	+35.8	dBm

Test Frequency = 1840MHz

TQP9421 Application Circuit Schematic and Layout





Bill of Material - TQP9421 Evaluation Board

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	High Linearity 0.5 W Power Amplifier	Qorvo	TQP9418
R1	0 Ω	Resistor, Chip, 0603, 5%	various	
C1	0.01 uF	Capacitor, Chip, 0603, 5%	various	
C11	100 pF	Capacitor, Chip, 0603, 5%	various	
C3, C9	0.1 uF	Capacitor, Chip, 0603, 5%	various	
C5, C14	10 uF	Capacitor , Chip, 6032, 10%, Tantalum	various	
C6, C10	1000 pF	Capacitor , Chip, 0603, NPO/COG, 5%	various	

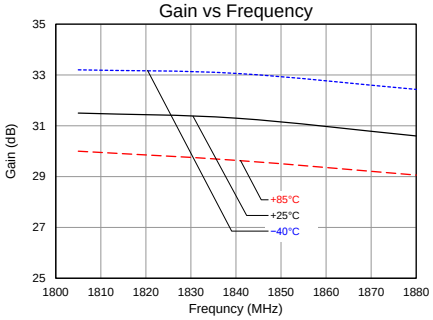
Vcc1=Vcc2=4.5V, Pout=27dBm, Signal PAR=9.5dB

LTE signal BW	5MHz	10MHz	15MHz	20MHz	2X20MHz	Units
ACLR1-Low	-47.4	-49.0	-49.9	-51.0	-40.8	dBc
ACLR1-high	-50.0	-49.8	-50.1	-51.2	-42.5	dBc

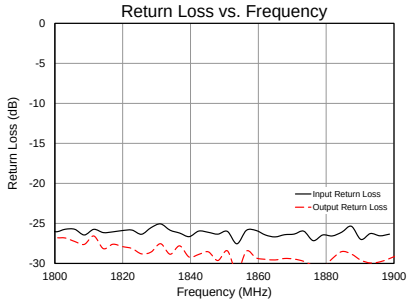
Performance Plots

Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +4.5V, Vref = +2.85 V, Temp.= +25 °C

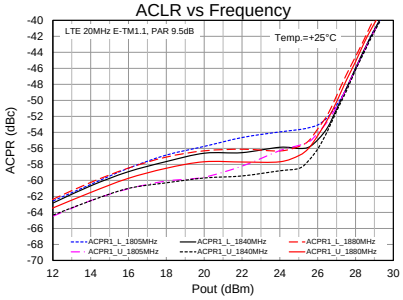
Gain vs Frequency



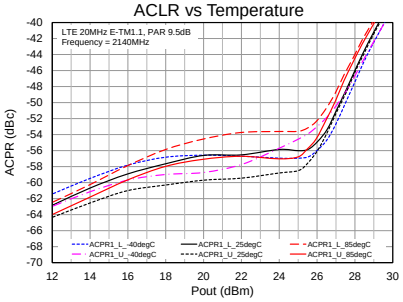
Return Loss vs. Frequency



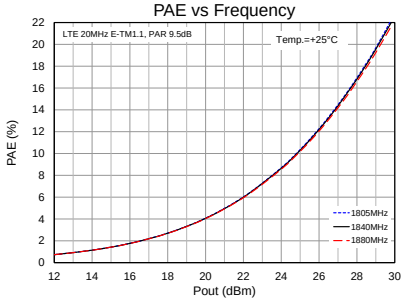
ACLR vs Frequency



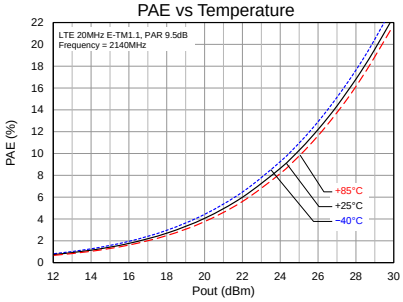
ACLR vs Temperature



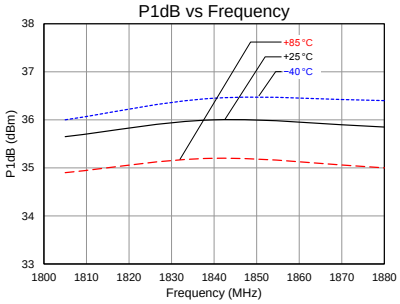
PAE vs Frequency



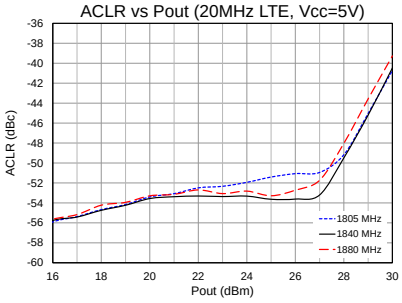
PAE vs Temperature



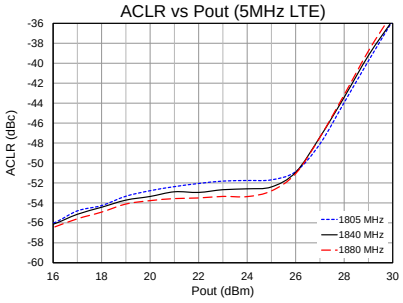
P1dB vs Frequency



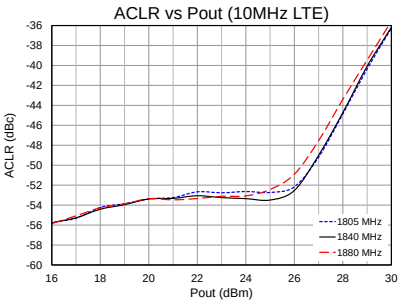
ACLR vs Pout (20MHz LTE, Vcc=5V)



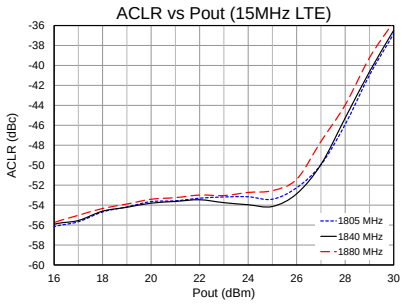
ACLR vs Pout (5MHz LTE)



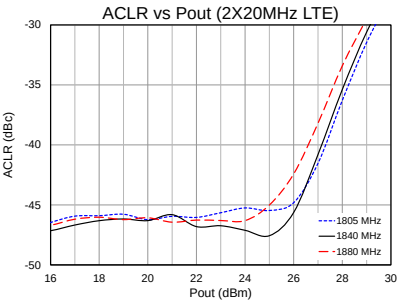
ACLR vs Pout (10MHz LTE)



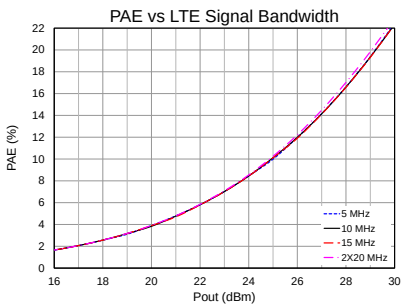
ACLR vs Pout (15MHz LTE)



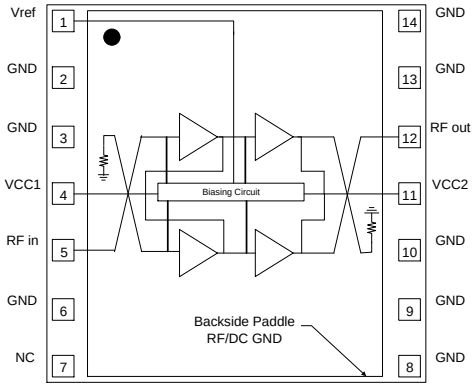
ACLR vs Pout (2X20MHz LTE)



PAE vs LTE Signal Bandwidth



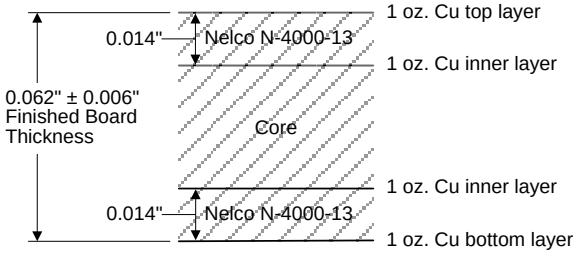
Pin Configuration and Description



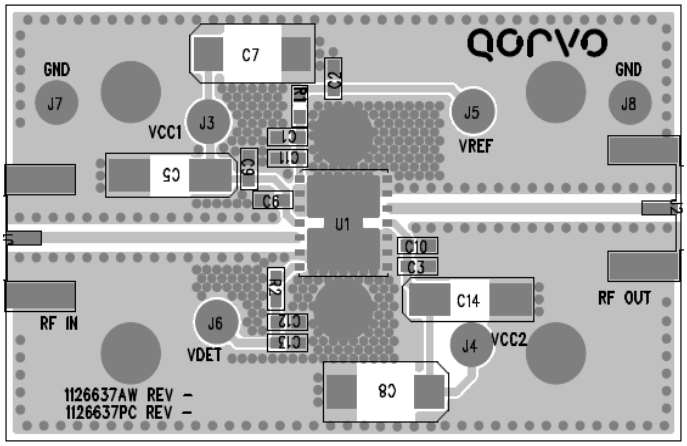
Pin No.	Label	Description
1	Vref	Provides reference voltage for internal active biasing circuit
2, 3, 6, 8, 9, 10, 13, 14	GND	RF and DC ground.
4	VCC1	Supply to first stage amplifier
5	RFin	RF input pin. The DC is internally blocked at this pin.
7	NC	No internal connection. Can be left open or grounded for mounting integrity.
11	VCC2	Supply to second stage amplifier.
12	RFout	RF output pin. The DC is internally blocked at this pin.
Backside Paddle	RF/DC GND	RF/DC ground. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 1126637 Material and Stack-up



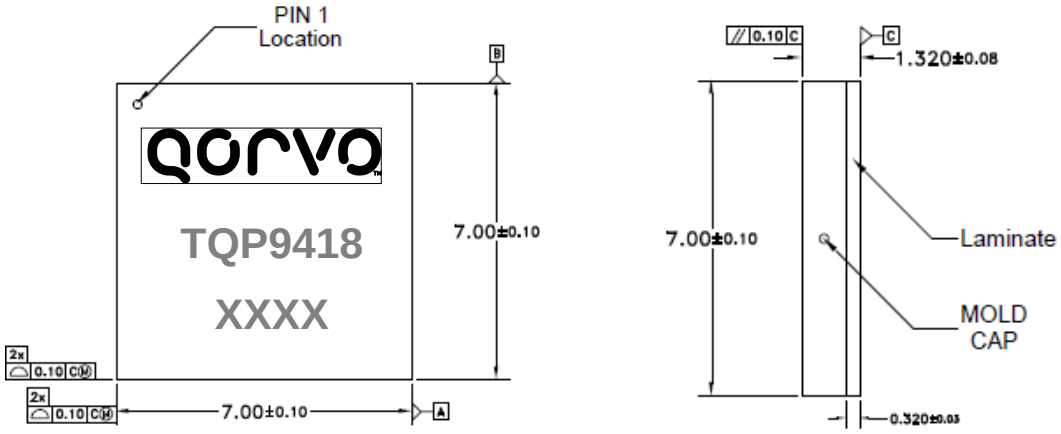
50 ohm line dimensions: width = .028”
spacing = .028”.

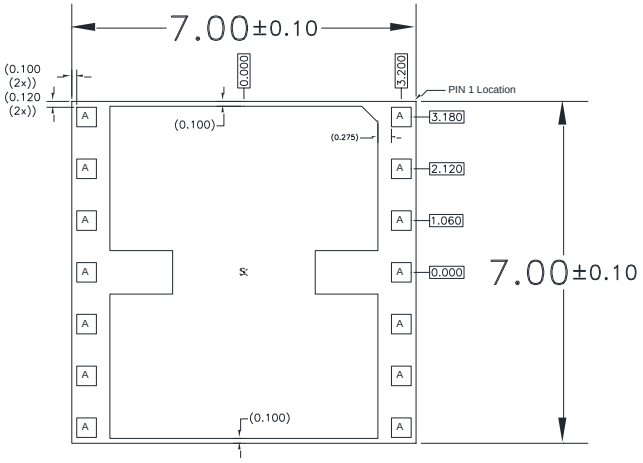


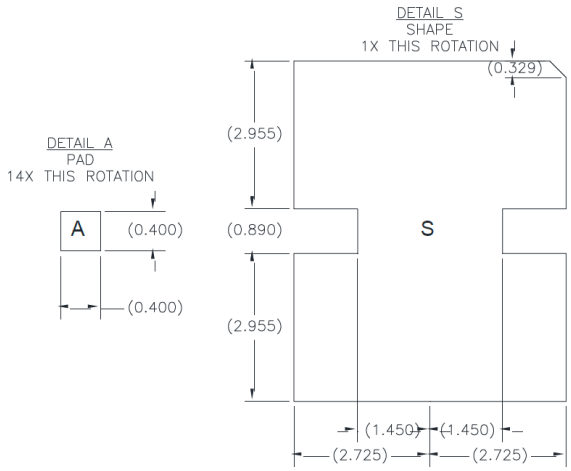
Mechanical Information

Package Marking and Dimensions

Marking: Part number – TQP9418
Trace code – XXXX





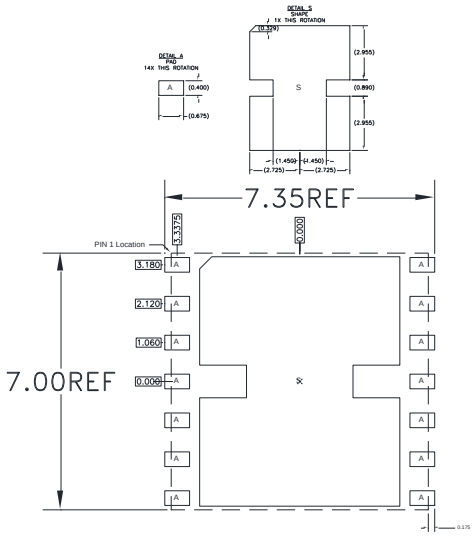


Notes:

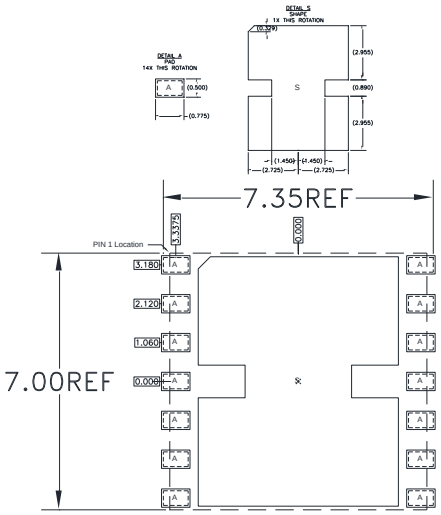
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern

Recommend PCB land-pad pattern metallization (Top View)



RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

Notes:

1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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