TR1001

FM Radio PLL IC

Data Sheet

AMENDMENT HISTORY

Version	Date	Description
V1.0	Feb, 2004	New release.
V1.1	Dec, 2011	Add Ordering Information table

CONTENTS

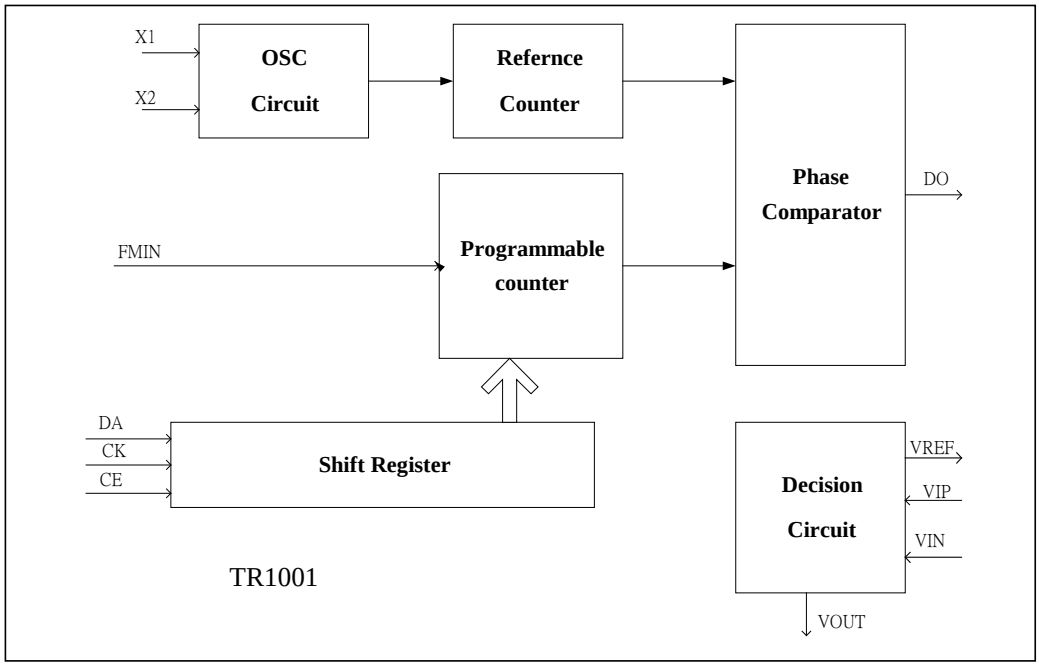
DESCRIPTION

The TR1001 is phase-locked loop (PLL) LSIs for digital tuning systems (DTS)
All functions are controlled through 3 serial bus lines. These LSIs are used to configure high-performance digital tuning system.

FEATURES

- Optimal for configuring digital tuning systems in high-fi tuners.
- Operate at input frequency ranging from 30~150 MHz during FMIN Input .
- All functions controlled through 3 serial bus lines.
- CMOS structure with operating power supply range of VDD=2.4~3.6V.
- 3.6MHz, 4.5MHz, 7.2MHz or 10.8MHz crystal oscillators can be used.

BLOCK DIAGRM



ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Characteristic	Symbol	Value	Unit
Supply Voltage	VCC	-0.3~6.0	V
Input Voltage	VIN	-0.3~VDD+0.3	V
Power Dissipation□	PD	300	MW
Operating Temperature	TOPR	-10~80	℃

ELECTRICAL CHARACTERISTICS (Ta=-10~80℃,VDD=2.4~3.6V.)

Characteristic	Symbol	Test Condition/Pin	Min	Typ.	Max	Unit
Operating Power Supply Voltage	VDD	PLL operation (normal operating)	2.4	3	3.6	V
Operating Power Supply Current	IDD	VDD=3.0V, XT=4MHz, FMIN=100MHz	--	2	4	mA

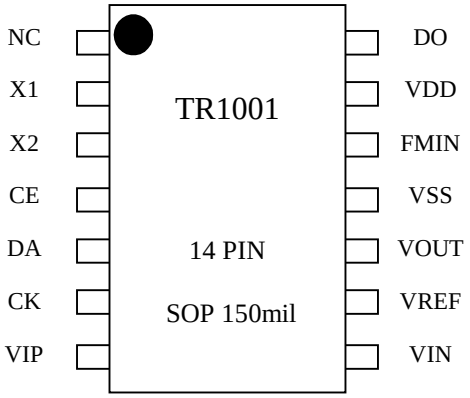
Operating frequency range

Crystal Oscillation Frequency		Connect crystal resonator to X1- X2 terminal		4		MHz
FMIN		VIN=0.2Vp-p	30	~	150	MHz

Operating input amplitude range

FMIN		30~150MHz	0.2	~	VDD-0.5	Vp-p

PIN DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Pin name	Description
2	X1	Crystal oscillator pins	These pins set the reference frequency of the reference counter.
3	X2		
4	CE	Shift register enable	These pins set the frequency of PLL.
5	DA	Shift register data input	
6	CK	Shift register clock input	
7	VIP		These pins decide the lock state of PLL.
8	VIN		
9	VREF		
10	VOUT	Decision circuit output pin	This pin informs the lock state of PLL.
12	FMIN	FM frequency input	These pins input FM band local oscillator signals by capacitor coupling. FMIN operate at low amplitude.
14	DO	Phase comparator Output	These pins are for phase comparator tri-state output.
11	VSS	Power supply pins	Applies 3.0V±10%
13	VDD		

FUNCTION DESCRIPTION

Serial I/O ports

The block diagram shows that the functions are controlled by setting data in the 16 bits registers. Each bit of data in these registers is transferred through the serial ports between the controller and the DA, CK and CE pins.

Serial transfer format

The serial transfer format consists of 16 data bits (Fig. 1).

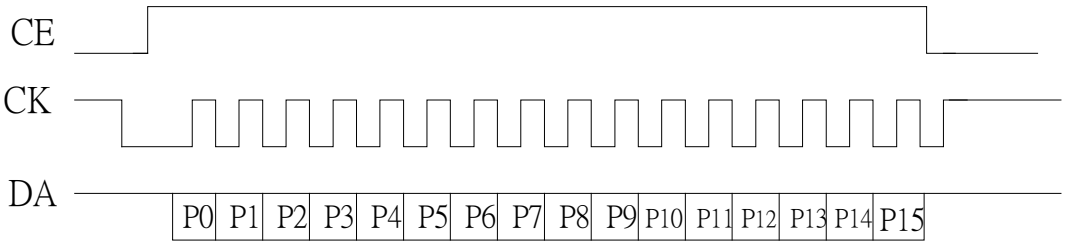


Fig.1

Serial data transfer

Serial data are transferred in sync with the clock signal. Data transfer ceases when the CE signal is set to “L” level. Since the receiving side receives the serial data as valid data when the clock signal rises, it is effective for the sending side to produce output in sync with the clock signal fall.

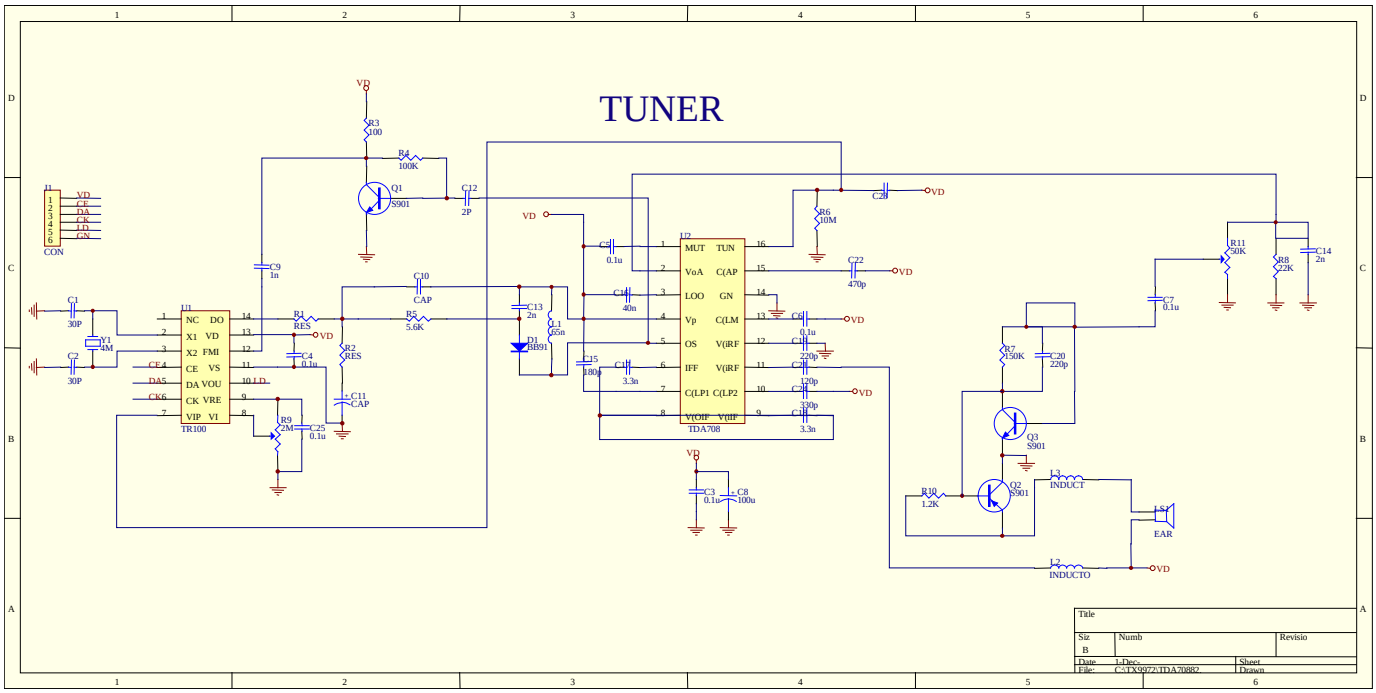
Programmable counter

The programmable counter section consists of 16bit programmable binary counter.

Setting programmable counter

The divisor for the programmable counter is set as binary data in bits P0~P15.(fig.1)
Divisor setting range n=640H~FF00H (1600~65280)

APPLICATION CIRCUIT



ORDERING INFORMATION

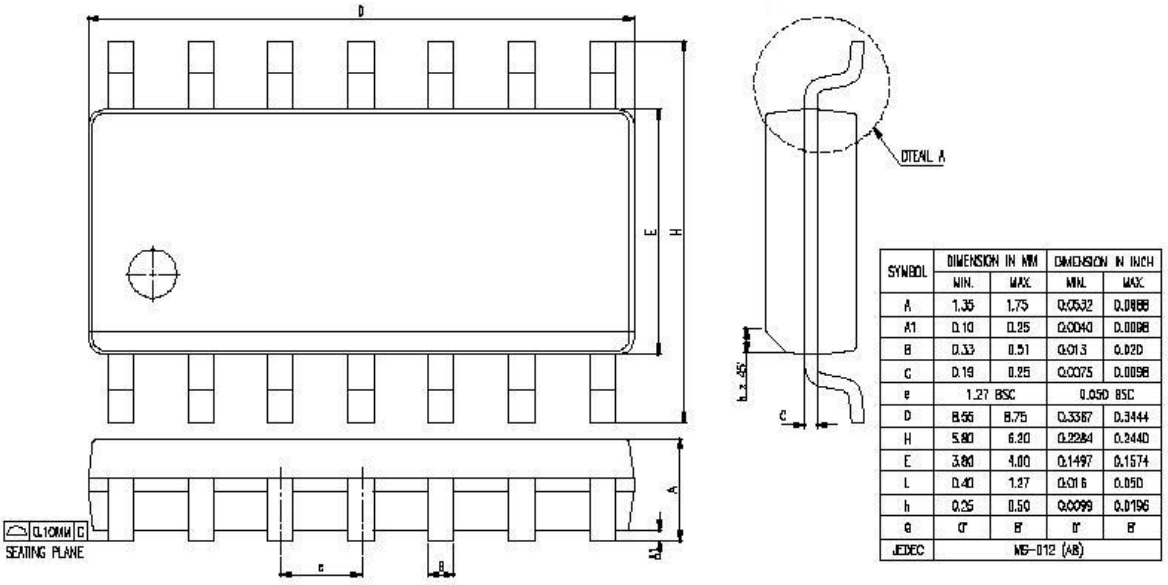
The ordering information:

Ordering number	Package
TR1001-000-15-X	SOP 14-pin (150 mil)

Note: "-X" represents the package material:

- Package material: Pb-free Code: W
- Package material: Green Package Code: G

PACKAGE OUTLINE (SOP14) 150mil



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
e	1.27 BSC		0.050 BSC	
D	8.56	8.75	0.3367	0.3444
H	5.80	6.20	0.2284	0.2440
E	3.80	4.00	0.1497	0.1574
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.0099	0.0196
θ	0°	8°	0°	8°
JEDEC	MS-012 (AB)			

NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH , PROTRUSIONS OR GATE BURRS.
MOLD FLASH , PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.