WESTERN DIGITAL
CORPORATION

TR1602/TR1402/TR1863/TR1865
Universal Asynchronous Receiver/Transmitter (UART)

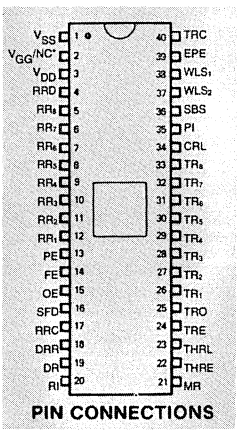
MARCH, 1981

FEATURES

- DUAL POWER SUPPLY TR1602/TR1402
- SINGLE POWER SUPPLY — +5VDC ON TR1863/5
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level for TR1602, TR1863/5)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS

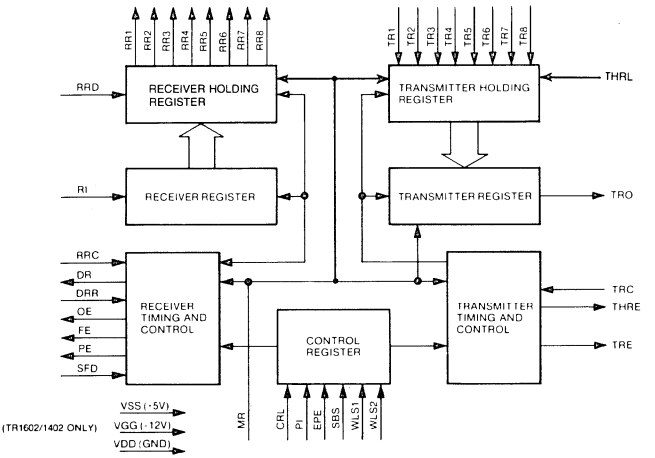
APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES



PIN CONNECTIONS

*TR 1402 & TR 1602-12V
TR 1863/5 NO CONNECTION



TR1602/TR1402/TR1863/TR1865 BLOCK DIAGRAM

GENERAL DESCRIPTION

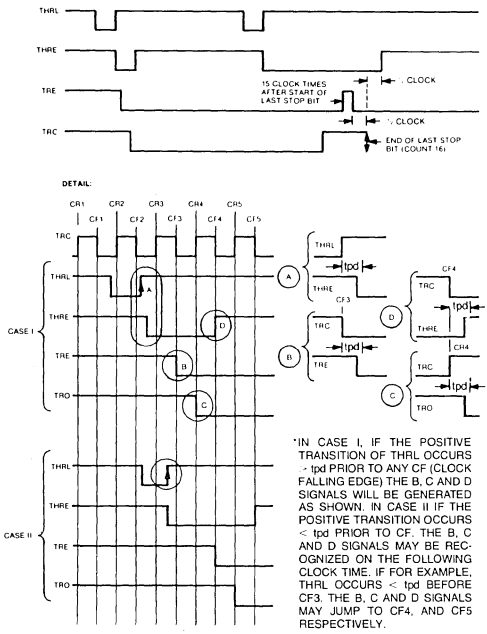
The ASYNCHRONOUS RECEIVER/TRANSMITTER is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start/stop bits, and optional parity. The receiver section converts a serial word with start, data, optional parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one-half when transmitting a 5 bit code. The TR1863/5 is pin- and function-compatible to the TR1402 and TR1602 except that it is +5V only and can operate up to 3.5 MHz (218.75K Baud). The standard TR1863/5 operates at 1.0 MHz (62.5K Baud).

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	VSS	+5 volts supply
2	V_{GG} — TR1602/TR1402 NC — TR1863/5	V_{GG} NC	-12 volts supply No Connection (open)
3	V_{DD} POWER SUPPLY	GND	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8- RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PARITY ERROR	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	OVERRUN ERROR	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.

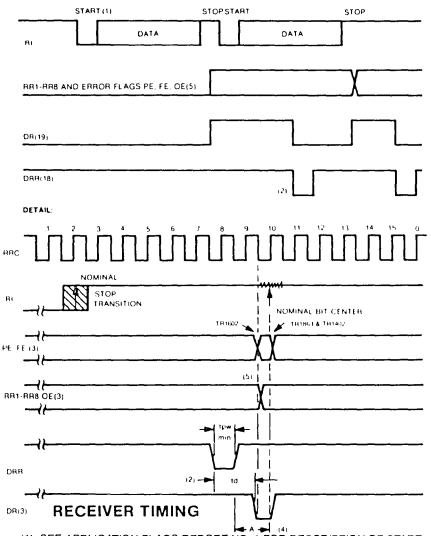
PIN NUMBER	NAME	SYMBOL	FUNCTION
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times times the desired receiver shift rate.
18	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the Transmitter and Receiver Holding Registers, the Transmitter Register, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a h igh-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage VOH, to a low-level output voltage, V_{OL}.
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_2 and WLS_1), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.

PIN NUMBER	NAME	SYMBOL	FUNCTION
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1602 and TR1863 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WORD LENGTH SELECT	WLS_2 -WLS_1	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.



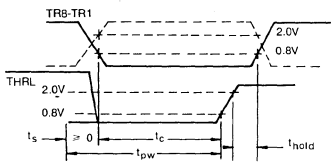
*IN CASE I, IF THE POSITIVE TRANSITION OF THRL OCCURS > tpd PRIOR TO ANY CF (CLOCK FALLING EDGE) THE B, C AND D SIGNALS WILL BE GENERATED AS SHOWN. IN CASE II IF THE POSITIVE TRANSITION OCCURS < tpd PRIOR TO CF. THE B, C AND D SIGNALS MAY BE RECOGNIZED ON THE FOLLOWING CLOCK TIME. IF FOR EXAMPLE, THRL OCCURS < tpd BEFORE CF3. THE B, C AND D SIGNALS MAY JUMP TO CF4, AND CF5 RESPECTIVELY.

TRANSMITTER TIMING

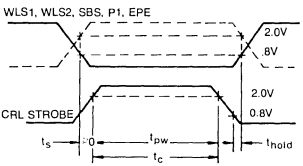


RECEIVER TIMING

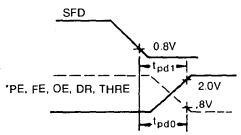
(1) SEE APPLICATION FLAGS REPORT NO. 1 FOR DESCRIPTION OF START BIT DETECTION
(2) THE DELAY BETWEEN DRR AND DR = tpd
(3) DR, ERROR FLAGS AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS tpd) PRIOR TO DR RISING EDGE
(5) DATA AND OE PRECEDES DR AND ERROR FLAGS BY ½ CLOCK
(6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.



DATA INPUT LOAD CYCLE

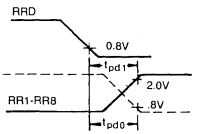


CONTROL REGISTER LOAD CYCLE



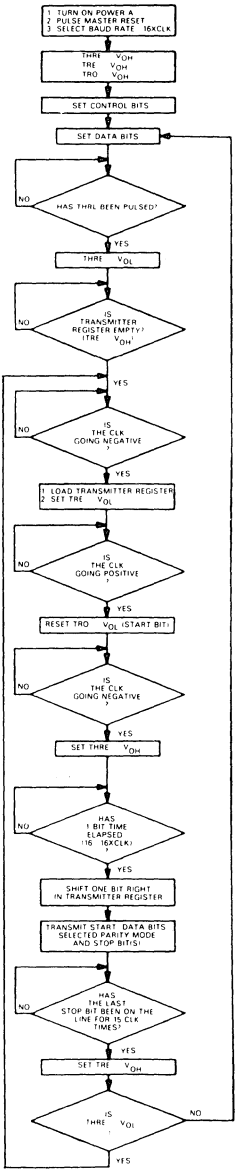
*OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM 0.8V TO 2.0V.

STATUS FLAG OUTPUT DELAYS

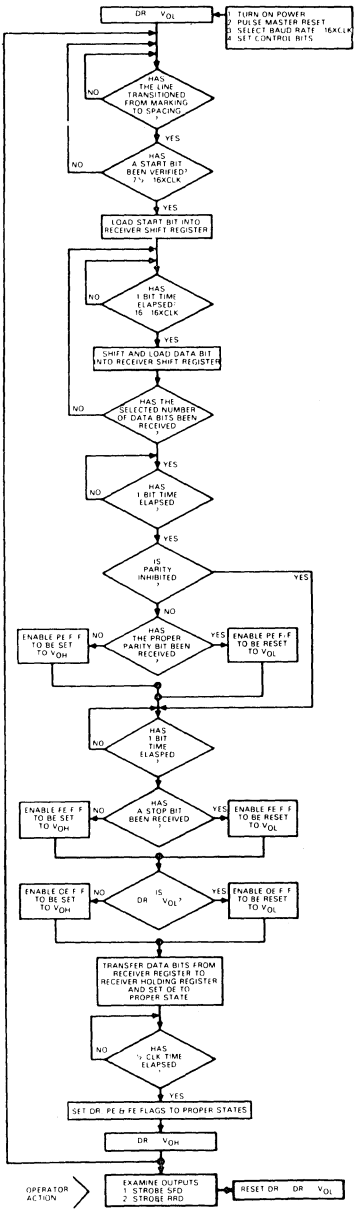


*RR, RR, ARE DISCONNECTED AT TRANSITION OF RRD FROM 0.8V TO 2.0V.

DATA OUTPUT DELAYS



TRANSMITTER FLOW CHART



RECEIVER FLOW CHART

ABSOLUTE MAXIMUM RATINGS NOTE: These voltages are measured with respect to GND

Storage Temperature -55°C to +125°C (Plastic) -65°C to +150°C (Ceramic)
V_{CC} Supply Voltage ..... -0.3V to +7.0V
Input Voltage at any pin ..... -0.3V to +7.0V
Operating Free-Air Temperature
T_A Range ..... 0°C to 70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS

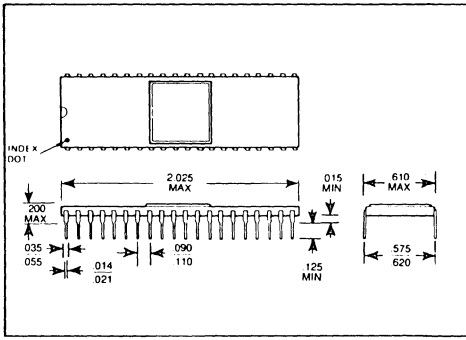
(V_{CC} = 5V ± 5%, V_{DD} = 0V, V_{GG} = - 12V ± 5%, TR1602/TR1402) (V_{CC} = 5V ± 5% TR 1863/5)

SYMBOL	PARAMETER	TR1602/TR1402		TR1863/5		
	OPERATING CURRENT	MIN	MAX	MIN	MAX	CONDITIONS
I_{CC}	Substrate Supply Current		60 ma		35 ma	V_{CC} = 5.25V
I_{GG}	Gate Supply Current		−10 ma			V_{GG} = −12.6V
	LOGIC LEVELS					
V_{IH}	Logic High	V_{SS} — 1.5V		2.4V		
V_{IL}	Logic Low		0.8V		0.6V	V_{CC} = 4.75V
	OUTPUT LOGIC LEVELS					
V_{OH}	Logic High	V_{SS} — 1.0V		2.4V		V_{SS} = 4.75V, I_{OH} = 100 µa
V_{OL}	Logic Low		0.4V		0.4V	V_{SS} = 5.25V, I_{OL} = 1.6 ma
I_{OC}	Output Leakage		10 µa		10ua	V_{OUT} = 0V, SFD = RRD = V_{IH}
I_{IL}	Low Level Input Current		-1.6 ma		*−1.6ma	V_{IN} =0.4V
I_{IH}	High level Input Current				10 µa	V_{IN} = 3.75V, TR1865 only

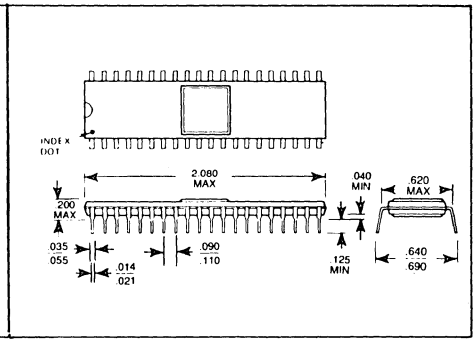
SWITCHING CHARACTERISTICS

(See "Switching Waveforms")

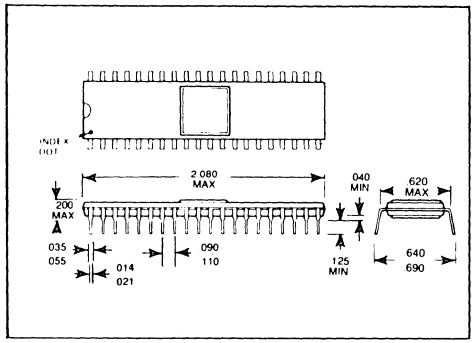
SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
f_{clock}	Clock Frequency			V_{CC} = 4.75V
	TR1402	DC	320 KHz	with internal pull-ups on all inputs
	TR1602	DC	320 KHz	with internal pull-ups on all inputs
	TR1863-00	DC	1.0 MHz	
	TR1863-02	DC	2.5 MHz	
	TR1863-04	DC	3.5 MHz	
	TR1865-00	DC	1.0 MHz	with internal pull-ups on all inputs
	TR1865-02	DC	2.5 MHz	with internal pull-ups on all inputs
	TR1865-04	DC	3.5 MHz	with internal pull-ups on all inputs
t_{pw}	Pulse Widths			
	CRL	200 ns		
	THRL	200 ns		
	DRR	200 ns		
	MR	500 ns		
t_C	Coincidence Time	200 ns		
t_{hold}	Hold Time	20 ns		
t_{set}	Set Time	0		
	OUTPUT PROPAGATION DELAYS			
t_{pd0}	To Low State 1602/1402		650 ns	
t_{pd1}	To High State 1602/1402		650 ns	C_L = 20 pf, plus one TTL load
t_{pd0}	To Low State 1863/1865		250 ns	
t_{pd1}	To High State 1863/1865		250 ns	C_L = 20 pf, plus one TTL load
	CAPACITANCE			
c_{in}	Inputs		20 pf	f = 1 MHz, V_{IN} = 5V
c_o	Outputs		20 pf	f = 1 MHz, V_{IN} = 5V



TR1602A, TR1402A, TR1863A, TR1865A
CERAMIC (HERMETIC) PACKAGE



TR1602B, TR1402B, TR1863B, TR1865B
PLASTIC PACKAGE



TR1602P, TR1402P, TR1863P,
TR1865P PLASTIC PACKAGE

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