TR16F096A(B)

Data Sheet

V1.6

96K Embedded Flash

Hi-Performance 16-bit Multimedia Processor

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TR16F096A(B) *16-bit Multimedia Processor*

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1. TR16F096A(B) General Description

The **TxP16E2**™ is a high performance 16-bit MCU, running up to 32MHz and provided with 96K FLASH and total 6K SRAM for high performance process of audio algorithm, power control and motor control. It is the new generation computational kernel for Flash DSP series2. It has initially aimed at the areas of controller and multimedia digital signal processing (DSP) application to demonstrate its profession. TxP16E2 furnish with fast **MAC** architecture, which allows multiplication+accumulation instructions to be issued with access memory simultaneously during one cycles. The TR16F096A(B) is equipped with TxP16E2 and integrating input/output ports, Audio PWM, Timer and Low Voltage Reset...etc on a chip. Built-in high-speed 12-bit ADC can apply to voice recording application easily.

Furthermore, TR16F096A(B) extend its external device connection capability such as Serial ROM/Flash. The internal memory capacity includes 96Kx16 program/data FLASH plus 6Kx16 working SRAM.

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2. TR16F096A(B) Features

- **Notice: TR16F096A(B) do not support ultra-deep sleep.**
- **Notice: PortC0 are forbidden to be connected with VCC or pull-up resistance.**
- **Notice: TR16F096B only supports SOP16-2 package. (PIN2 is PB3+PC0)**
- **Notice: TR16F096A(B) does not support buzzer and speaker wake up, so MISC2 bit5, MISC2 bit 6 and MISC3 bit3 should be set to 0.**
- **Notice: If Microphone is used, OPA1 and OPA2 need to be disable.**
- High-performance RISC TxP16E2 CPU
  - high working performance 32MIPS@SRAM PM
  - Max speed 24MIPS in no branch condition (Turbo-Speed ON) @Flash PM
  - Max speed 16MIPS (Turbo-Speed OFF) @Flash PM
  - wide working voltage 1.8Volt ~ 5.5Volt
  - Operation frequency is programmable by Software
  - Built-in 4096x16 SRAM + 2048 x16 SRAM
  - Embedded PC Stack Level 24
- Rich DSP function
  - Hardware Circular Buffer support
  - MAC Computation power : 32 MIPS (max.)
  - Multi-Function Support: In MAC calculation, simultaneously access two operands from memory in one cycle
  - Extend Dynamic Range: A 40-bit accumulator to ensure in 512 successive multiple+additions no overflows
- Embedded Flash 96Kx16
  - Typical 2,0000 erase/program cycles
  - Greater than 10 years Data Retention
- Software-based audio processing technical
  - Voice recognition, Subband , ADPCM , Melody
- Support 22+2(ICE PAD can be as I/O) general purpose I/O port.
- Stereo 16bit PWM and Mono 16bit DAC
- 15 IRQ & 1 FIRQ
  - FIRQ can interrupt IRQ immediately
  - 2 external interrupt
- SPI Master interface with 4 buffers
- SPI Slaver
- UART for IAP(In Application Programming)
- I2C interface
- Three timers: Timer1, Timer2, RTC timer
- Support Spread Spectrum clocking to reduce EMI.
- Watch dog timer (WDT)

- Low voltage reset (LVR)
- Low dropout regulator(LDO) supply 3.3V/2.4V/1.8V@20mA (voltage drop 0.1v)
- PB0, PB1, PB2, PB3 support two edge modes for wake-up function are rising and falling edge trigger.
- Three Comparators
- 12bit SAR ADC 12bit / 8 channel
- 16bit ∑-△ ADC
- Microphone with AGC(Auto Gain Control)
- Crystal 32768
- Low voltage detector
- Touch with BG Pre-Charge
- IR 38K
- 1402 interface
- PIR / CDS / OPA
- Four I/O pins support de-bounce input
- PortA5 support high sink current 60mA@3.3V
- **Notice: Special I/O PortC0 will cause LED flashing light when power on.**
- **Notice: PortC0 / PortC2 / PortC3 / PortC4 / PortC5 / PortC6 / PortC7 are forbidden to be directly connected to inductive components. For example, motors and coils, etc.**
- **Notice: VCC Decoupling Cap 10uF should be close to IC within 0.5cm in PCB layout.**
- **Notice: VCC Decoupling Cap 0.1uF should be close to IC within 0.5cm in PCB layout.**
- **Notice: The width of VCC and VSS power line should be greater than 30 mil in PCB layout.**
- **Notice: TR16F096A(B) does not support the function of deep sleep.**

3. TR16F096A(B) Application Field

- MCU Application
- Electronic Dictionary
- Handheld Games
- Electronic Learning Aid (ELA)
- Electronics storybook

4. TR16F096A(B) Block Diagram

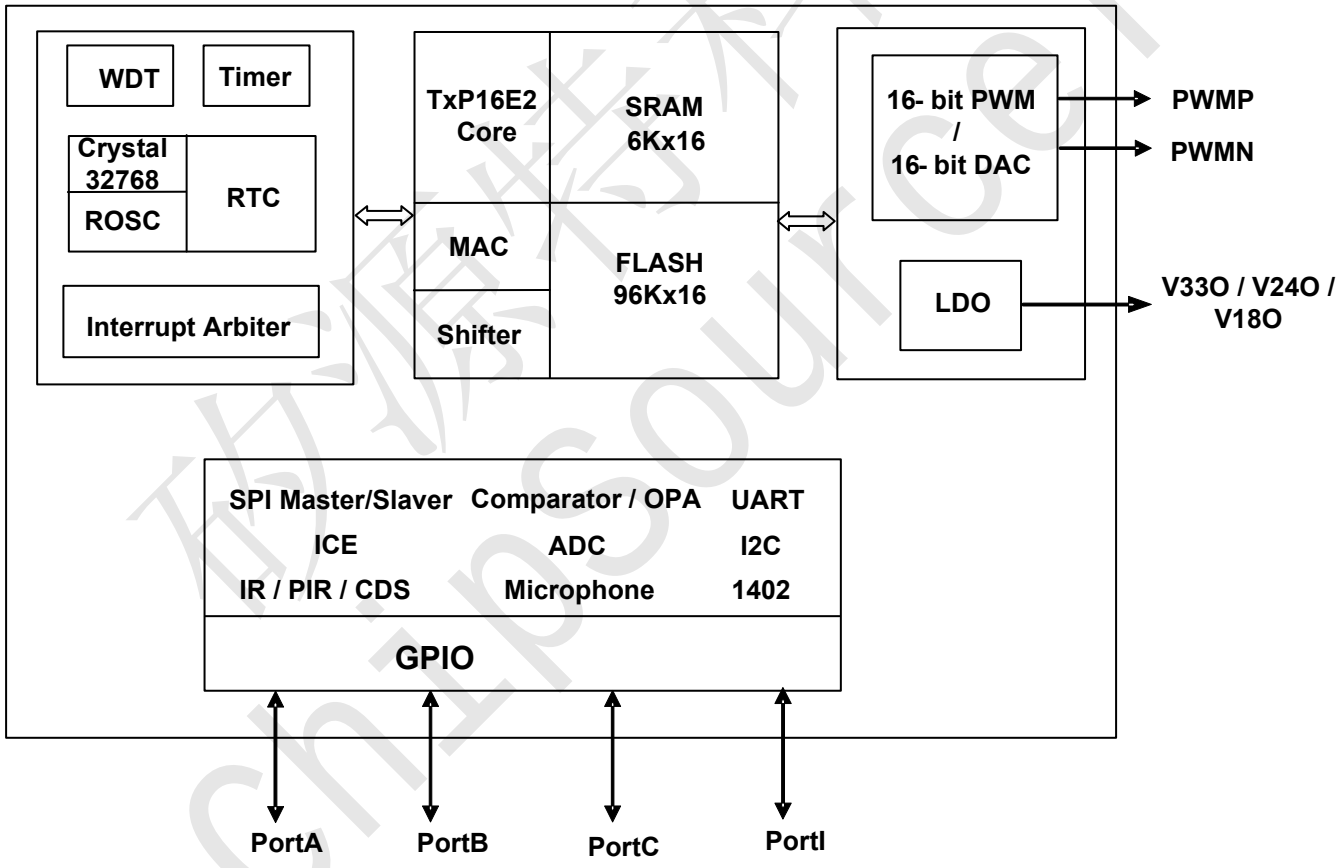

Figure 4.1

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4.1 Pin Assignments /Description

Pin Name	I/O	State after RESET	FUNCTIONS
Chip Power			
VCC	I	High	Chip Power Input
VSS	I	Low	Digital Ground
AVSS	I	Low	Analog Ground
VIO	I	High	PortA IO Power input
V33O	O	High	3.3V/2.4V/1.8V LDO Power Output
VPD	I	High	PWM IO PAD Power Input
VPS	I	Low	PWM IO PAD Ground
General Purpose I/O Port			
PortA[5:0]	I/O	Low	PortA is programmable Input/Output port
PortB[7:0]	I/O	Low	PortB is programmable Input/Output port
PortC[7:0]	I/O	Low	PortC is programmable Input/Output port PortC[0] is programmable Input/Output port when not connected to ICE ICE_VPP: PortC[0] is embedded ICE VPP pin when connected to ICE Probe.
PortI[1]/ ICE_SCLK	I/O	Low	PortI[1] is programmable Input/Output port when not connected to ICE Probe. Internal pull-down R (50K ohm) will be enable at ICE mode. ICE_SCLK: PortI[1] is embedded ICE clock pin when connected to ICE Probe.
PortI[0]/ ICE_SD	I/O	Low	PortI[0] is programmable Input/Output port when not connected to ICE Probe. Internal pull-down R (50K ohm) will be enable at ICE mode. ICE_SD: PortI[0] is embedded ICE data pin when connected to ICE Probe.
PWM Audio			
PWMP	O	Low	Digital PWM output(+) / Analog DAC output(+)
PWMN	O	Low	Digital PWM output(-) / Analog DAC output(-)

- **Notice: Special I/O PortC0 will cause LED flashing light when power on.**
- **Notice: PortC0 are forbidden to be connected with VCC or pull-up resistance.**

5. TR16F096A(B) Function Descriptions

5.1 TxP16E2

As shown in the block diagram in Figure 4.1, the TxP16E2 is a 16-bit data width processing capability and all instructions are operated in one cycle except parameter data ROM(PM) access. The TxP16E2 not only provides general arithmetic such as addition, subtraction, shifter, normalize, and other logical operations, but it also involves circular buffer operations for complexity digital signal processing.

5.2 TxP16E2 Registers

The TxP16E2 contains of register files are illustrated below:

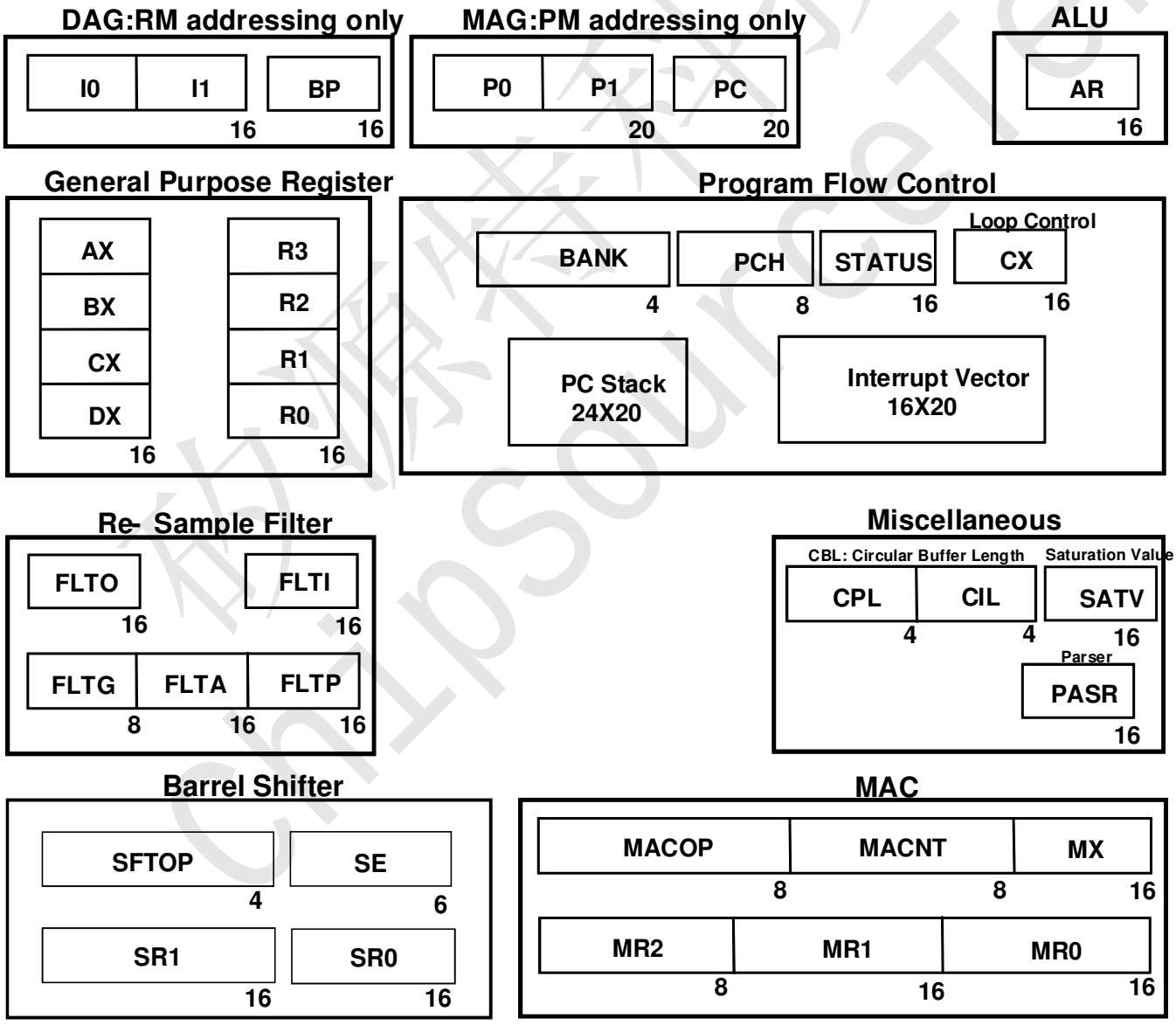

Figure 5.1 TxP16E2 Processor Core Registers

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■ REGISTER FILES DEFINE:

AR: Accumulator Register
I0: Index 0 Register
I1: Index 1 Register
BP: Base Pointer Register
P0: Pointer 0 Register
P1: Pointer 1 Register
MACOP: MAC Operation Register
MACNT: MAC Operation Loop Counter
MX: MUL/MAC Input X Register
MR0: MUL/MAC Result Register 0
MR1: MUL/MAC Result Register 1
SFTOP: Shifter Operation Register
SE: Shifter Exponent Register
MR2: MUL/MAC Result Register 2
AX: General AX Register
BX: General BX Register
CX: General CX Register
DX: General DX Register
R0: General R0 Register
R1: General R1 Register
R2: General R2 Register
R3: General R3 Register
CBL: Circular Buffer Length Register
PASR: Parser Register
SR1: Shifter Result Register 1
SR0: Shifter Result Register 0

5.2.1 Special Registers

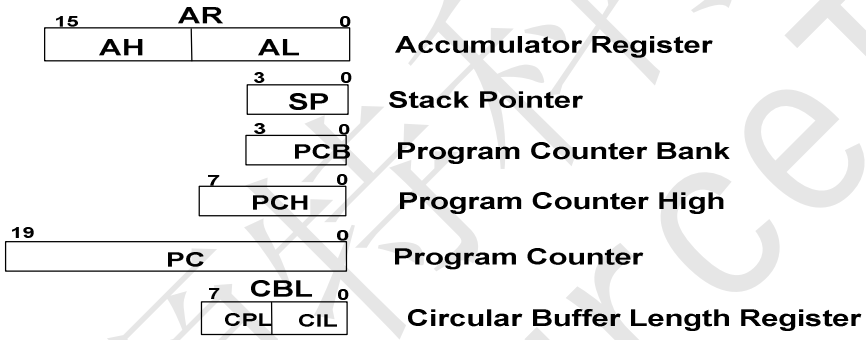

Figure 5.2 TxP16E2 Special Registers

- Accumulator Register

The AR is a general-purpose 16-bit register that stores the result of last arithmetic or logical operation. In addition, any data write to AR will affect the status flag.

- Stack Pointer

The SP is a 4-bit register that is for addressing Stack position. The SP will automatically increment / decrement cause by instruction “CALL” / “RETS”, and more detail revealed as the “PC Stack” section.

- Program Counter Bank

The program memory map is divided into 16 banks by PCB register (Program Counter Bank). From BANK8 to BANK14 are system reserved. From BANK0 to BANK7 are implemented as Flash memory. The BANK15 is implemented as static RAM.

- Program Counter High

The instruction “LJMP” and “LCALL” will refer PCH and PCB registers to compose of 20-bit pointer provides the 16x64K words PM addressing range.

- Program Counter

The 20-bit PC register provides 16x64K-word addressing capability. It is responsible for MCU fetch now executing instruction.

- Circular Buffer Length Register

Many algorithms such as convolution, correlation, and digital filter require the circular data buffers. The TxP16E2 supports circular buffer operating via the I0 vs. CIL and P0 vs. CPL. The modulus logic implements automatic modulus addressing for accessing RM/PM circular buffer data.

5.2.2 Common I/O Registers

The TxP16E2 involves 32 common I/O registers are shown in Table 5.1. There are defined the peripheral IO control and system register.

Symbol	Adr	Reset	RW	B15/b7	b14/b6	b13/b5	b12/b4	B11/b3	B10/b2	b9/b1	b8/b0	Description
STATUS.L	00H	00	R/W	INTEN	-	UART_EN	AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR	Bank15	-	-	SPIS_EN	SPIM_EN	
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Interrupt Enable
INTENA.H	01H	00	R/W	ENA15	ENA14	ENA13	ENA12	ENA11	ENA10	ENA9	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Interrupt Request
INTREQ.H	02H	00	R/W	Req15	Req14	Req13	Req12	Req11	Req10	Req9	Req8	
IntVect	03H	XX	R/W	IntVect[15:0]								Interrupt Vector access Window
IOC_PA	04H	00	R/W	IOC_PA[5:0]								"1"= out, "0" = in of related PA bit
IOC_PB	05H	00	R/W	IOC_PB[7:0]								"1"= out, "0" = in of related PB bit
IOC_PCI.L	06H	00	R/W	IOC_PC[7:0]								"1"= out, "0" = in of related PC bit
IOC_PCI.H	06H	00	R/W	IOC_PI[1:0]								1"= out, "0" = in of related PI bit
PortA	07H	XX	R/W	PortA[5:0]								Read: in port Write: out port
PortB	08H	XX	R/W	PortB[7:0]								Read: in port Write: out port
PortCI.L	09H	XX	R/W	PortC[7:0]								Read: in port Write: out port
PortCI.H	09H	XX	R/W	PortI[1:0]								Read: in port Write: out port
INTMASK.L	0AH	00	R/W	Mask7	Mask6	Mask5	Mask4	Mask3	Mask2	Mask1	Mask0	Interrupt Mask
INTMASK.H	0AH	00	R/W	Mask15	Mask14	Mask13	Mask12	Mask11	Mask10	Mask9	Mask8	
SPIS_CTL	0BH	XX	W	SPIS_CFG [15:0]								SPI Slaver Control
SPIS_DAT	0CH	XX	XX	SPIS_DAT [15:0]								SPI Slaver Data
SPIM_CTL	0DH	XX	R/W	SPIM_CFG [15:0]								SPI Master Control
SPIM_DAT	0EH	XX	R/W	SPIM_DAT [15:0]								SPI Master Data
Reserve	0FH	XX	XX									
Reserve	10H	XX	XX									
Reserve	11H	XX	XX									
UART_CTL	12H	XX	XX	UART_CTRL[15:0]								UART Signal
UART_DAT	13H	XX	XX	UART_DATA[15:0]								UART Signal
Reserve	14H	XX	XX									
MISC6.L	15H	00	R/W	DEB_ININV	DEB_INTEN	DEB_WKEN	DEB_EN	OPA2_EN	OPA1_EN	LDO24EN	PIR_EN	System Miscellanea register #6
MISC6.H	15H	00	R/W	DEB_OUT	PIR_CMPO	CDS_EN	DEB_INSEL			DEB_CLKSEL		
Audio-PWML / Audio-DAC	16H	XX	W	Audio-PWML / Audio-DAC[15:0]								Audio PWM L / DAC Channel
Audio-PWMR	17H	XX	W	Audio-PWMR [15:0]								Audio PWM R Channel
MISC5.L	18H	00	R/W	THO	LVDO	CMP2_TIMER2	CMP1_TIMER1	CMP2_INT_INV	CMP1_INT_INV	CMP2_INT_EN	CMP1_INT_EN	System Miscellanea register #5
MISC5.H	18H	00	R/W	InterPLY_FREQ_DIV								
MISC4.L	19H	00	R/W	TOUCH_REALT	TINT_EN	TIS		SVT	THEN	PREC	CMP3EN	System Miscellanea register #4
MISC4.H	19H	00	R/W	CY32K_STAB	DAC_OG			InterPLY_EN	Tone_Mode	InterPLY_FUN		
MISC3.L	1AH	00	R/W	D2ENB	LVDEN	SPIS_PIN_SEL	SPI_PIN_SEL	0	ENHC	CY32KEN	LP32KEN	System Miscellanea register #3
MISC3.H	1AH	00	R/W	CMPO3	CMPO2	CMPO1	LVD					
MISC2.L	1BH	00	R/W	PGAEN	0	0	GBB	CMP2EN	CMP1EN	-	LDO33EN	System Miscellanea register #2
MISC2.H	1BH	00	R/W	THR			AGCEN	GA				
MISC1.L	1CH	00	R/W	TCS	DAC_EN	PWM_MUTE	DAC_MUTEB	RC_RST	EXRST	LVR	WDT	System Miscellanea register #1
MISC1.H	1CH	00	R/W	CLR_RealT	DEB_WAKE	-	RTC_WAKE	IR_EN	IR_PIN_SEL	PWM_EN	MODX	
RealT	1DH	XX	R	RealT[15:0]								RealT register
ClrWDT	1DH	XX	W									Clear WDT
IOP_IX	1EH	XX	W	IOPIX[7:0]								Programming IO Port index
IOP_DAT	1FH	XX	W	IOPD[15:0]								Programming IO Port Data

Table 5.1 Common I/O registers

5.2.3 Basic System Registers

◆STATUS register

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
STATUS.L	00H	20	R/W	INTEN	-	UART_EN	AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR	Bank15	-	-	SPIS_EN	SPIM_EN	

The Status register provides two main functions, the first system flag holds the status information generated by the computational blocks of the TxP16E2, which used for program sequencer control. The second indicated that special function of hardware module is enable or not.

For program flow control:

System Flag	Definition
AZ	ALU or AR Result Zero
AN	ALU or AR Result Negative
AV	ALU Overflow
AC	ALU Carry
PA	Parser Queue available(Read only)
FA	Filter buffer available(Read only)

System hardware control:

System Flag	Definition
INTEN	System global interrupt control bit
IntVWR	Interrupt Vector Table access window control bit
UART_EN	UART enable bit
SPIM_EN	SPI master enable bit
SPIS_EN	SPI slaver enable bit
BNAK15	1 = Current program is run in BNAK15

◆ Address 01H, 02H and 0AH: Interrupt control registers, the detail are illustrated in Interrupt section.

◆ Address 04H~15H: GPIO registers, the detail are illustrated in GPIO section.

◆Address 16H~17H: Audio-PWM control registers, the detail are illustrated in AUDIO section.

◆System Miscellanea register #1

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC1.L	1CH	00	R/W	TCS	DAC_EN	PWM_MUTE	DAC_MUTEB	RC_RST	EXRST	LVR	WDT	System miscellanea register #1
MISC1.H	1CH	00	R/W	CLR_RealT	DEB_WAKE	-	RTC_WAKE	IR_EN	IR_PIN_SEL	PWM_EN	MODX	

Item	Description
Clr_RealT	Set high to clear 32-bit RealT timer. (this bit only for TCS=1)
DEB_WAKE	Debounce Wake Up Flag (Read Only)
RTC_WAKE	RTC Wake Up Flag (Read Only)
IR_EN	IR 38K Enable
IR_PIN_SEL	IR 38K PIN Select 0:PortA4 1:PortB4
PWM_EN	Audio PWM enable

MODX	MODX=0 is chosen narrowband sound-effect filter. MODX =1 is chosen wideband sound-effect filter. Actual bandwidth is dependent on source signal sample-rate.
TCS **(Note2*)**	Enable RealT Timer
DAC_EN	Audio DAC enable
PWM_MUTE	Audio PWM mute enable
DAC_MUTEB	Audio DAC mute enable
RC_RST **(Note1*)**	System Reset from internal RC reset
EXRST	System Reset from external reset pin
LVR	System Reset from low voltage reset
WDT	System Reset from watch dog reset

Note1: RC_RST, EXRST, LVR will clear WDT bits, except for WDT is set to 1. All of the reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device reset.

Note2: If programmer read the “RealT” register, it can get 32-bit timer based on 30.517ns(32.768MHz). An example is shown as follows. Address 1DH: RealT register.

```
io[RealT]   = ar          ; write to reset the state machine of 32-bit real timer.
ar          = io[RealT]   ; read low-word timer[15:0]
ar          = io[RealT]   ; read high-word timer[31:16]
```

◆System Miscellanea register #2

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC2.L	1BH	00	R/W	PGAEN	0	0	GBB	CMP2 EN	CMP1 EN	-	LDO33 EN	System miscellanea register #2
MISC2.H	1BH	00	R/W	THR			AGCEN	GA				

Item	Description
THR	Default:0 , Threshold voltage control
AGCEN	Default:0 , AGC enable
GA	Default:0 , PGA gain adjust, from 16db to 46db
PGAEN	Default:0 , Programmable Gain Amplifier
GBB	Default:0 , GBB=0 for PGA gain boost
CMP2EN	Default:0 , Comparator 2 Enable
CMP1EN	Default:0 , Comparator 1 Enable
LDO33EN	Default:0 , LDO 3.3V Output Enable

◆System Miscellanea register #3

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC3.L	1AH	00	R/W	D2ENB	LVDEN	SPIS_PIN_SEL	SPI_PIN_SEL	0	ENHC	CY32K EN	LP32K EN	System miscellanea register #3
MISC3.H	1AH	00	R/W	CMPO3	CMPO2	CMPO1	LVD					

Item	Description
CMPO3	Comparator 3 Output (Read Only)
CMPO2	Comparator 2 Output (Read Only)
CMPO1	Comparator 1 Output (Read Only)
LVD	Default:0 , LVD voltage 1.8~ 2.98V for D2ENB=0(each step~ 40mV), 2.7V~4.47V for D2ENB=1(each step~ 60mV)
D2ENB	Default:0 , VCC divide 2 for LVD input
LVDEN	Default:0 , LVD Enable
SPIS_PIN_SEL	SPI Slaver Pin Select 0:PortB[3:0] 1:PortA[3:0]
SPI_PIN_SEL	SPI Master Pin Select 0:PortA[3:0] 1:PortB[3:0]

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ENHC	Fast start mode for external capacitor
CY32KEN	Crystal 32768 enable, X32I / X32O (PortC7 / PortC6)
LP32KEN	Lower Power 32768 enable

◆System Miscellanea register #4

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC4.L	19H	00	R/W	TOUCH_REALT	TINT_EN	TIS		SVT	THEN	PREC	CMP3EN	System miscellanea register #4
MISC4.H	19H	00	R/W	CY32K_STAB	DAC_OG			InterPLY_EN	Tone_Mode	InterPLY_FUN		

Item	Description
CY32K_STAB	Crystal 32768 stable flag
DAC_OG	Default:0, DAC output gain = 1
InterPLY_EN	0:DAC Interpolation disable 1: DAC Interpolation enable
Tone_Mode	0:TONE disable 1:TONE enable
InterPLY_FUN	0:DAC Interpolation disable 1: DAC Interpolation 8 point 2:DAC Interpolation 16 point 3: DAC Interpolation 32 point
TOUCH_REALT	Touch with Real-T function 0:disable & clear real-T stop flag 1:enable
TINT_EN	Touch INT Enable
TIS	Touch I/O Port input select , 00: NA, 01:PortA, 10: NA, 11:PortC
SVT	Touch SVT , 0: 1/4*VCC, 1: 1/2*VCC
THEN	Touch Enable
PREC	Touch Pre-charge 1.5V
CMP3EN	Default:0 , Comparator 3 Enable

◆System Miscellanea register #5

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC5.L	18H	00	R/W	THO	LVDO	CMP2_TIMER2	CMP1_TIMER1	CMP2_INT_INV	CMP1_INT_INV	CMP2_INT_EN	CMP1_INT_EN	System Miscellanea register #5
MISC5.H	18H	00	R/W	InterPLY_FREQ_DIV								

Item	Description
InterPLY_FREQ_DIV	System Frequency Divisor for DAC interpolation, Default:0
THO	TOUCH Output (Read Only)
LVDO	LVD Output (Read Only)
CMP2_TIMER2	Comparator 2 with Timer2 function 0:disable & clear Timer2 stop flag 1:enable
CMP1_TIMER1	Comparator 1 with Timer1 function 0:disable & clear Timer1 stop flag 1:enable
CMP2_INT_INV	Comparator 2 INT Inverse
CMP1_INT_INV	Comparator 1 INT Inverse
CMP2_INT_EN	Comparator 2 INT Enable
CMP1_INT_EN	Comparator 1 INT Enable

◆System Miscellanea register #6

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC6.L	15H	00	R/W	DEB_ININV	DEB_INTEN	DEB_WKEN	DEB_EN	OPA2_EN	OPA1_EN	LDO24EN	PIR_EN	System Miscellanea register #6
MISC6.H	15H	00	R/W	DEB_OUT	PIR_CMPO	CDS_EN	DEB_INSEL			DEB_CLKSEL		

Item	Description
DEB_OUT	Debounce Output (Read Only)
PIR_CMPO	PIR Comparator Output (Read Only)
CDS_EN	Default:0 , CDS Function Enable
DEB_INSEL	Debounce Input Select
DEB_CLKSEL	Debounce Clock Select
DEB_ININV	Default:0 , Debounce Input Inverse
DEB_INTEN	Default:0 , Debounce Interrupt Enable
DEB_WKEN	Default:0 , Debounce Wake Up Enable
DEB_EN	Default:0 , Debounce Function Enable
OPA2_EN	Default:0 , OPA 2 Enable
OPA1_EN	Default:0 , OPA 1 Enable
LDO24EN	Default:0 , LDO 2.4V Output Enable
PIR_EN	Default:0 , PIR Function Enable

◆ Virtual Programming IO

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
VIO_IX	1EH	XX	W	-	-	-	IOPIX4	IOPIX3	IOPIX2	IOPIX1	IOPIX0	Programming IO Port index
VIO_DATA	1FH	XX	W	IOPD[15:0]								Programming IO Port Data

Table 5.2 Virtual Programming IO

The operation steps of these group register, first select virtual IO port index then write data to programming IO port.

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
Timer1	00H	00	W	Timer0								Timer1
Timer1	00H	00	R	Current Timer1 Value								
Timer2	01H	00	W	Timer1								Timer2
Timer2	01H	00	R	Current Timer2 Value								
RTCTimer	02H	00	RW	RTCTimer								RTC Timer
FetchCNT	03H	00	W	-	-	-	-	-	-	Fetch _Timer2	Fetch _Timer1	Fetch Timer1/2 Current Value
Reserve	04H	-	-									
PA_PDEN	05H	00	W	PA_PDEN[5:0]								PortA Pull Down Enable
PB_PDEN	06H	00	W	PB_PDEN[7:0]								PortB Pull Down Enable
PCI_PDEN.L	07H	00	W	PC_PDEN[7:0]								PortCI Pull Down Enable
PCI_PDEN.H	07H	C0	W	PI_PDEN[1:0]		-	-	-				PortCI Pull Down Enable ***(PortI default : Enable PD100K)***
PA_PUEN	08H	00	W	PA_PUEN[5:0]								PortA Pull Up Enable
PB_PUEN	09H	00	W	PB_PUEN[7:0]								PortB Pull Up Enable
PCI_PUEN.L	0AH	00	W	PC_PUEN[7:0]								PortCI Pull Up Enable
PCI_PUEN.H	0AH	00	W	PI_PUEN[1:0]		-	-	-				PortCI Pull Up Enable
PA_PDSEL	0BH	00	W	PA_PDSEL[5:0]								PortA Pull Down Select
PB_PDSEL	0CH	00	W	PB_PDSEL[7:0]								PortB Pull Down Select
PCI_PDSEL.L	0DH	00	W	PC_PDSEL[7:0]								PortCI Pull Down Select
PCI_PDSEL.H	0DH	00	W	PI_PDSEL[1:0]		-	-	-				PortCI Pull Down Select
PA_TOUCH	0EH	00	W	PA_TOUCH[5:0]								PortA Touch Enable
PB_TOUCH	0FH	00	W	PB_TOUCH[7:0]								PortB Touch Enable
PCI_ TOUCH.L	10H	00	W	PC_TOUCH[7:0]								PortCI Touch Enable
PCI_ TOUCH.H	10H	00	W	PI_TOUCH[1:0]		-	-	-				PortCI Touch Enable
PA_ODEN.L	11H	00	W	PA_ODEN[5:0]								PortA Open Drain Enable
PA_ODEN.H	11H	00	W			PA5_ HCEN						PortA5 High Current Enable
PB_ODEN	12H	00	W	PB_ODEN[7:0]								PortB Open Drain Enable
PCI_ ODEN.L	13H	00	W	PC_ODEN[7:0]								PortCI Open Drain Enable
PCI_ ODEN.H	13H	00	W	-		-	-	-				PortCI Open Drain Enable
WAKEN_PA	14H	00	W	PortA_WAKEN[5:0]								PortA WAKE UP Enable
WAKEN_PB	15H	00	W	PortB_WAKEN[7:0]								PortB WAKE UP Enable
WAKEN_PC	16H	00	W	PortC_WAKEN[7:0]								PortC WAKE UP Enable
WAKELV_PA	17H	00	W	PortA_WAKELV[5:0]								PortA WAKE UP Edge “1”= Pos-Edge, “0” = Neg-Edge of related PA bit
WAKELV_PB	18H	00	W	PortB_WAKELV[7:0]								PortB WAKE UP Edge “1”= Pos-Edge, “0” = Neg-Edge of related PB bit
WAKELV_PC	19H	00	W	PortC_WAKELV[7:0]								PortC WAKE UP Edge “1”= Pos-Edge, “0” = Neg-Edge of related PC bit
WAKEDLV_PB	1AH	00	W	PortB_WAKEDLV[3:0]								PortB Double-Edge WAKE UP Enable
Reserve	1BH	-	-	-								
Reserve	1CH	-	-	-								
Debounce_T1	1DH	00	W	Tdebounce[15:0]								Debounce Time Register
Debounce_T2.L	1EH	00	W	Tdelay[7:0]								Debounce Delay Time Register
Debounce_T2.H	1EH	00	W	Toff[7:0]								Debounce OFF Time Register

5.3 PC Stack

The PC STACK is TxP16E2 special embedded memory used to save (PC+1) value, which is composed with 24-level.

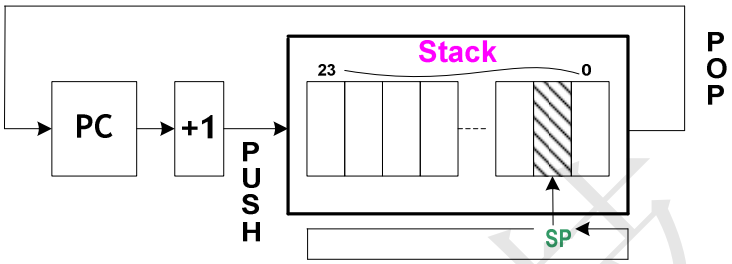

Figure 5.3 PC Stack Structure

Stack's top value is indexed by stack pointer (SP) register. When CALL instruction is executed, then the (PC+1) will PUSH onto stack addressing by SP and it will auto decrement. At the end of subroutine when RETS instruction is executed the SP will auto increment and stack content of pointer by SP will POP into PC.

The contents of STACK and SP are neither readable nor writeable by instruction. The SP is initialized to “0” after RESET.

5.4 Interrupt

5.4.1 Interrupt Vector Table

The Interrupt Vector Table is TxP16E2 special embedded memory, which is composed with 16-level of FIFO, used to store the index of interrupt service routine (ISR) address. User can access Interrupt Vector Table by read/write IntVect I/O register, which refers PCB register to compose of 20-bit address.

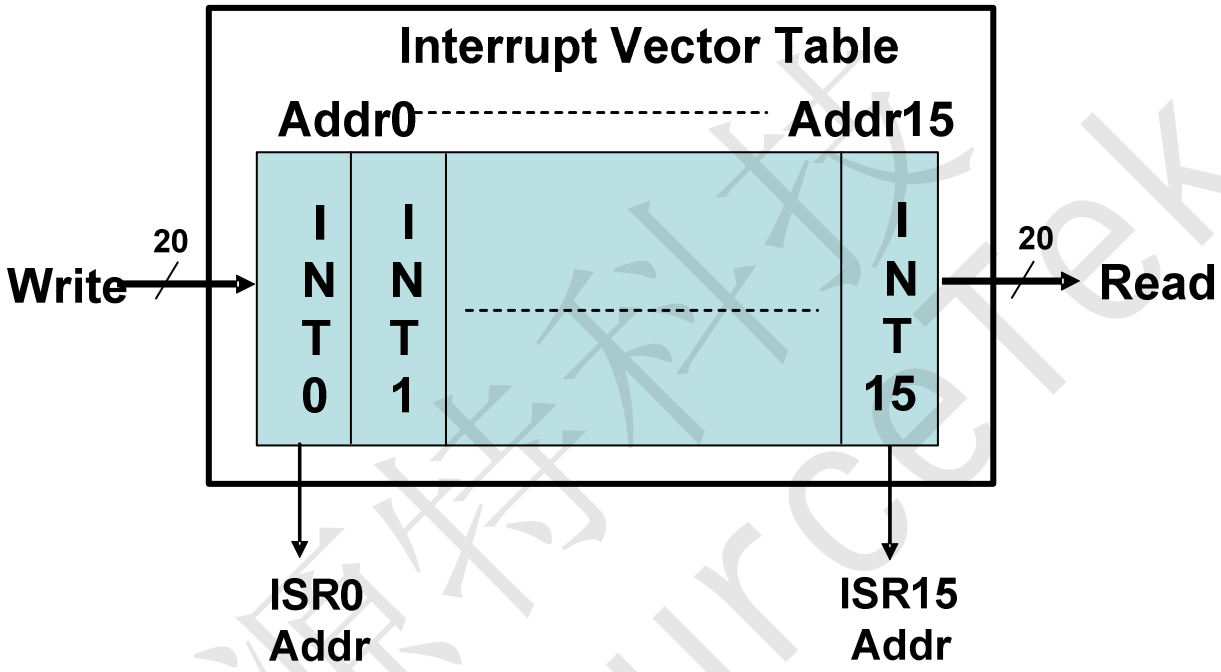

Figure 5.4 Interrupt Vector Structure

5.4.2 Interrupt Controller

Common I/O registers

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS.L	00H	00	R/W	INTEN	-	UART_EN	AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR	Bank15	-	-	SPIS_EN	SPIM_EN	
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Interrupt Enable
INTENA.H	01H	00	R/W	ENA15	ENA14	ENA13	ENA12	ENA11	ENA10	ENA9	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Interrupt Request
INTREQ.H	02H	00	R/W	Req15	Req14	Req13	Req12	Req11	Req10	Req9	Req8	
INTMASK.L	0AH	00	R/W	Mask7	Mask6	Mask5	Mask4	Mask3	Mask2	Mask1	Mask0	Interrupt Mask
INTMASK.H	0AH	00	R/W	Mask15	Mask14	Mask13	Mask12	Mask11	Mask10	Mask9	Mask8	

This chip provides several interrupt sources, including internal Audio PWM, T1, T2, RTC, I2C, UART, SPI master, SPI slaver, Flash ready, ADC, Touch and 2 external ExtINT0, ExtINT1 interrupts. More details control will describe as follows:

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Interrupt Source	Interrupt Vector	Priority(default)
Audio PWM Timer	0H	INT0_IRQ
Timer1	1H	INT1_IRQ
Timer2	2H	INT2_IRQ
RTC Timer	3H	INT3_IRQ
ExtINT0 / CMP1**(Note)**	4H	INT4_IRQ
ExtINT1 / CMP2**(Note)**	5H	INT5_IRQ
SPI Master	6H	INT6_IRQ
De-bounce	7H	INT7_IRQ
SPI Slaver	8H	INT8_IRQ
Flash Erase/Program Ready	9H	INT9_IRQ
12bit ADC	AH	INT10_IRQ
I2C	BH	INT11_IRQ
UART	CH	INT12_IRQ
TRA1402 / 16bit ADC	DH	INT13_IRQ
Touch	EH	INT14_IRQ(lowest)
Reserve	FH	INT15_IRQ(highest)

Table 5.3 Interrupt Sources

Note: Only one interrupt source can be selected for each interrupt vector.

(a) Global interrupt enable (INTEN)

The global interrupt INTEN controls the enable/disable of all interrupts. When INTEN is cleared to “0”, all interrupts are disabled. When INTEN is set to “1”, all interrupts are enabled (but still dependent on value of INTENA register). The INTEN is initialized to “”0” after power on.

(b) Interrupt enable (INTENA)

The interrupt enable from ENA15 to ENA0 are shown in above. An interrupt is allowed when these control bit are set to “1”, and interrupt is inhibit when these control bit are cleared to “0”. They are all initialized to “0” after power on.

(c) Interrupt request (INTREQ)

If an interrupt raising edge request is generated, the related interrupt request bit is set to “1” by hardware and waits for interrupt accept. INTREQ can be cleared to “0” by software. Hardware will not clear this bit. INTREQ are all initialized to “0” after power on.

(d) Interrupt mask (INTMASK)

The interrupt can be masked by setting bit15~ bit0 of interrupt mask register as above. Each interrupt source in the system can be masked individually.

(e) Interrupt Priority

INT15_IRQ (highest) > INT0_IRQ > INT1_IRQ > INT2_IRQ > INT3_IRQ > INT4_IRQ > INT5_IRQ > INT6_IRQ > INT7_IRQ > INT8_IRQ > INT9_IRQ > INT10_IRQ > INT11_IRQ > INT12_IRQ > INT13_IRQ > INT14_IRQ(lowest).

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5.4.3 Interrupt Processing

When any interrupt request(INTREQ) is generated, the acceptance of interrupt is decided by the interrupt enable(ENA) and global interrupt enable(INTEN). If the global interrupt enable(INTEN), related interrupt enable bit(ENA) are set to “1” and related mask bit(MASK) are cleared to 0, that interrupt will be accepted on the next clock. These following procedures will automatically be done in one clock cycle by hardware showing below:

(1) Program Counter(PC), PCB, PCH, AR and FLAG will be stored in special hardware registers.

(2) PC will be set to the corresponding interrupt entry address by refer to interrupt vector table.

(3) The global interrupt enable (INTEN) is cleared to “0”, which avoids the nest interrupt happened.

When interrupt service routine was finished, an RETI instruction will perform the procedures by hardware showing as follows:

(1) Restore the stored PC, PCB, PCH, AR and FLAG.

(2) The global interrupt enable (INTEN) is set to “1”, which allows to accept the subsequent interrupt.

Before executing RETI instruction, the corresponding interrupt request (INTREQ) bit must be cleared to “0” by software. If the request bit is not cleared, the same interrupt will be accepted again.

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5.5 MAC (16-bit X 16-bit Multiplier and Accumulator)

A 16 bit x 16 bit MAC is provided for digital signal processing. The core of MAC operation is multiply MX&MY with 2'S complement operand and accumulation previous 40-bit MF then rounding store result in the 40-bit MR register. The basic MAC architecture is shown as Figure 5.5.

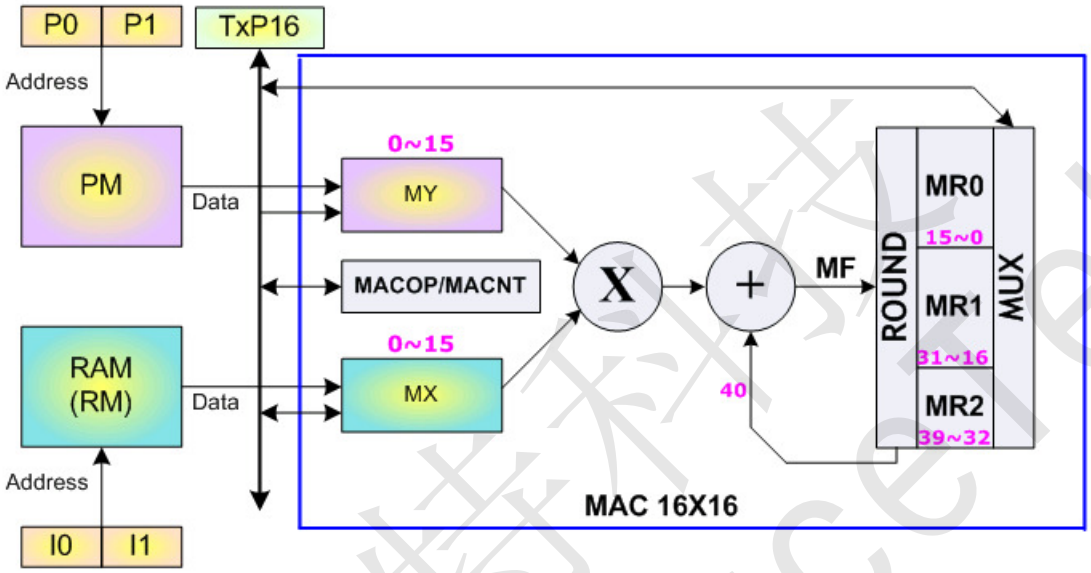

Figure 5.5 MAC Architecture

Define MAC module registers:

MX: MAC input 16-bit X register

MR: Multiplier or MAC result 40-bit register

MACOP: MAC operation define register

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
MACOP	00	R/W	RND1	RND0	P0/P1	POP:+/-	I0/I1	IOP:+/-	MY:SU(01)	MX:SU(01)	MAC Operation Setup

MACNT: MAC equation loop counter, max to 255

Basically, multiplier operates equation:

MR = MX*MY(SU) → MX: signed, MY: unsigned

Permission MY is AR or immediate value (-128~127), MX and MY are signed or unsigned assign by MACOP. So, actual multiplier instruction likes this:

MR = MX*AR or MR = MX*56

The operation of MAC equation is:

MR = MR + (MX*MY(SU))<<RND, MX=RM[I0++], MY=PM[P1--]

The means of equation is signed MX multiply unsigned MY the result value shift left RND bits and add previous MR then write back to MR.

Simultaneously, load new value to MX fixed from RM[index operation]

MY fixed from PM[pointer operation]

Therefore, MAC array operation like this:

```
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
                .
                .                                          Successive 64 times
                .
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
```

Actual just one line of instruction present in assembly coding like this:

MACNT = 63

This is very benefit for reducing code size. Of curse, we need setup MACOP register previous; at this example is like this;

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
MACOP	00	R/W	RND1	RND0	P0/P1	POP:+/-	I0/I1	IOP:+/-	MY:SU(01)	MX:SU(01)	MAC Operation Setup
			0	1	1	1	0	0	0	0	

Note: Successive MAC operation will cause MCU interrupt disable.

5.6 Barrel Shifter

The shifter accept a 16-bit input and can any place in a 32-bit output. The core of shifter include arithmetic shift, logic shift, exponent detector and normalization. The basic shifter architecture is shown as Figure 5.6.

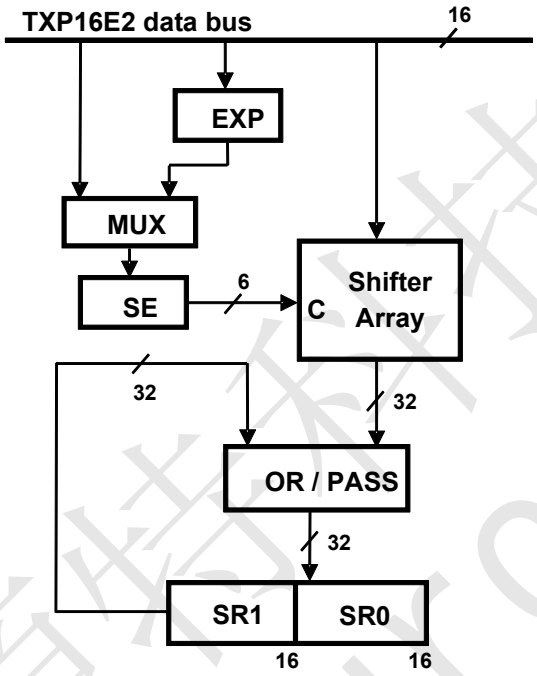

Figure 5.6 Barrel Shifter Architecture

Define Barrel Shifter module registers:

EXP: The EXP (Exponent Detector) register determines the number of leading sign bits and produces output number which indicates to eliminate redundant sign bits during the normalize operation.

SE: The shifting of input is determined by SE register. Positive SE value indicates a left shift and negative SE value indicate a right shift. SE register is set from TxP16E bus or EXP register.

SR1, SR0: barrel shifter result 32-bit register

SFTOP: shifter operation define register

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
SFTOP	00	W							Arith./Logic	PASS/OR	Shifter Operation Setup

SFTOP[1]: 0(arithmetic shifter, default), 1(logic shifter).

SFTOP[0]: 0(the shifter array output is passed through and load to SR register), 1(shifter array output may be OR logic with SR register, and then OR logic result is loaded into SR register).

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6. TR16F096A(B) Memory Configuration

6.1 Internal Program/Parameter Memory by DFFOFF / DFFON instruction

TxP16E2 consider both instruction and data ROM are the same as program ROM(PM), so it's very flexible and efficient for instruction and data memory allocation in PM. The total of logical PM space is 16 banks. Each bank has 64 K space. The 16 x 64K space is addressed by memory address generator unit (MAG). In TR16F096A(B), BANK0 is implemented as Flash memory. From BANK2 to BANK14 are system reserved. The BANK15 is implemented as static RAM. When TxP16E2 executed an **DFFON** instruction, the DFF register starts at the last location of BANK0 (0FFF0h~0FFFFH), and user can dynamically update PM data for MAC operation. When TxP16E2 executed an **DFFOFF** instruction, the DFF register will be cancelled. More details control will describe as follows:

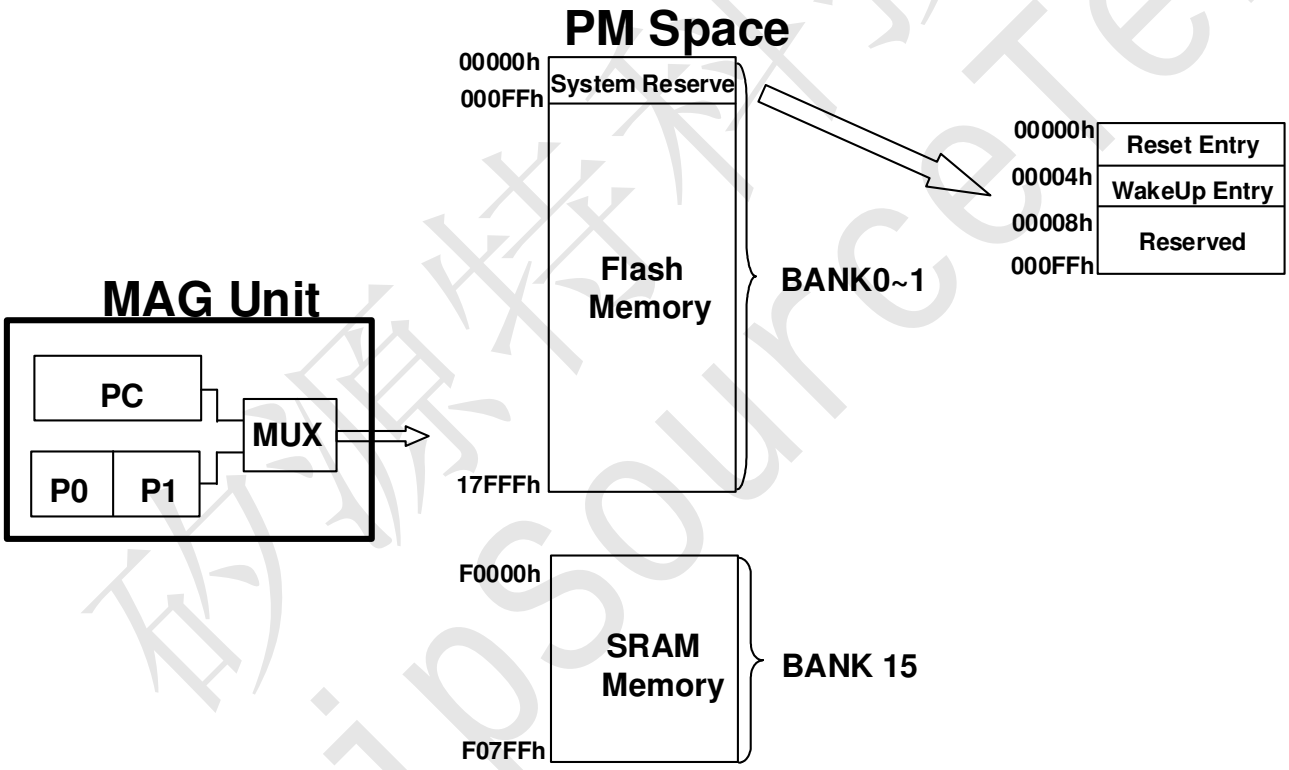


Figure 6.1 PM block diagram by DFFOFF instruction

When TxP16E2 executed an instruction, the PM address is generated from PC register. Similarity, when it access a word data, the PM address is composed with 20-bit from P0 or P1. System will auto adjust execute target space when program context switch between BANK0 and BANK15.

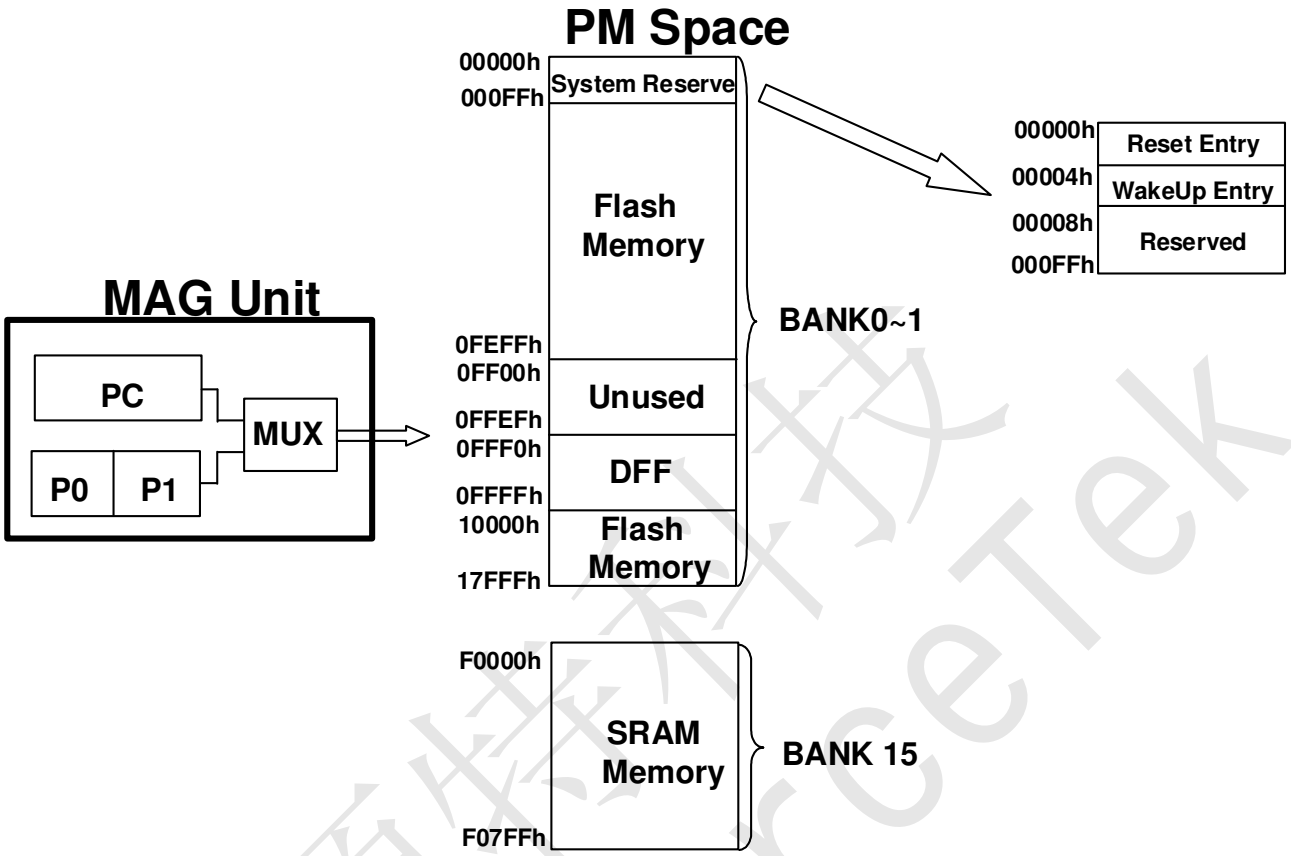


Figure 6.2 PM block diagram by DFFON instruction

6.2 Internal Data Working SRAM

The internal data working ram space is totally 6Kx16-bit that named as RM. Addressing ranged from 0x0000 through 0x17FF, which is generated by Data Address Generator Unit (DAG). Note: Index register (I0,I1,BP) are 16-bit width, but RM address line is only 12-bit width(0~4095); therefore, RM address will be warping when index value exceed 4095.

Note: Total SARM size is 6Kx16-bit. If PM(BANK15 / 2Kx16-bit) is used, RM will be 4Kx16-bit. If PM(BANK15) is no used, RM will be 6Kx16-bit. SARM configuration is set by option code.

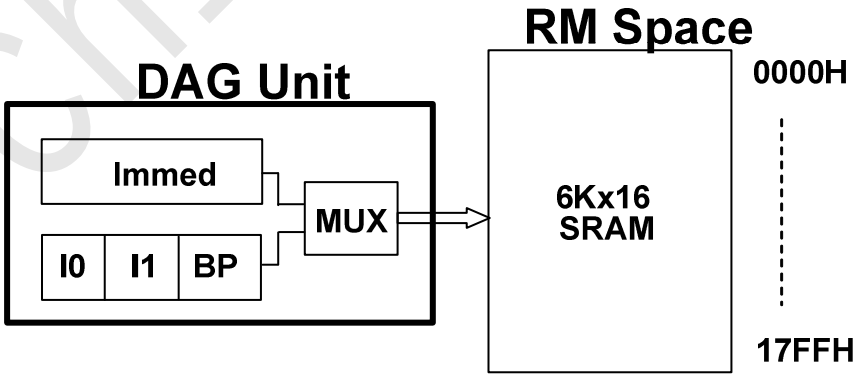


Figure 6.3 RM block diagram

6.3 Data Stack

A Last In First Out (LIFO) STACK is implementation for temporary data storage in RM memory. Generally, Data Stack is start-up at the bottom of RM, so BP is usually set to 0x17FF.

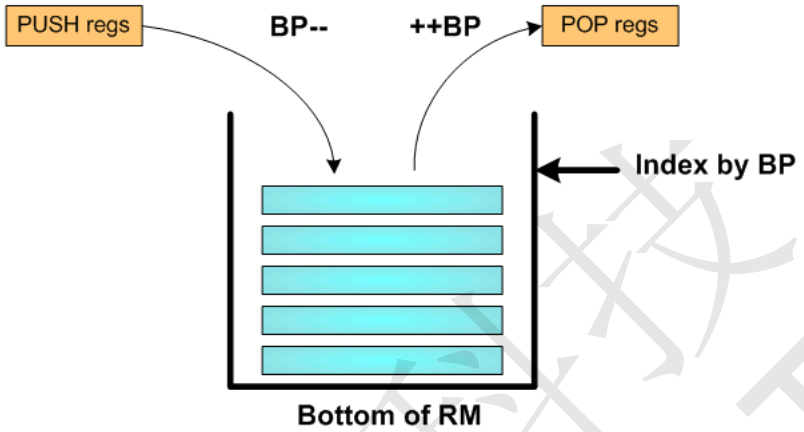


Figure 6.4 Data Stack Structure

Data Stack's top value is indexed by base pointer (BP) register. When PUSH instruction is executed, the “regs” will PUSH onto stack which address by BP and it will auto decrement. If POP instruction is performed, the BP will auto increment and stack content of pointed by BP will POP into “regs”.

7. TR16F096A(B) Peripherals

7.1 Programmable Timers

Common I/O registers

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS.L	00H	00	R/W	INTEN	-	UART_EN	AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR	Bank15	-	-	SPIS_EN	SPIM_EN	
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Interrupt Enable
INTENA.H	01H	00	R/W	ENA15	ENA14	ENA13	ENA12	ENA11	ENA10	ENA9	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Interrupt Request
INTREQ.H	02H	00	R/W	Req15	Req14	Req13	Req12	Req11	Req10	Req9	Req8	

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
Timer1	00H	00	W	Timer0								Timer1
Timer1	00H	00	R	Current Timer1 Value								
Timer2	01H	00	W	Timer1								Timer2
Timer2	01H	00	R	Current Timer2 Value								
RTCTimer	02H	00	RW	RTCTimer								RTC Timer
FetchCNT	03H	00	W	-	-	-	-	-	-	Fetch_Timer2	Fetch_Timer1	Fetch Timer1/2 Current Value

7.1.1 Audio PWM Timer

Audio PWM timer is fixed generate 32kHz interrupt request when INTENA0 bit is turned on, *If Auto FIFO_EN is setting the interrupt request rate = Ft / FIFO_Length.* ***Notice: It should be avoided that INTENA bit0 is turned on/off quickly. If need to turned on/off INTENA bit0 quickly, recommend to use INTMASK bit0.***

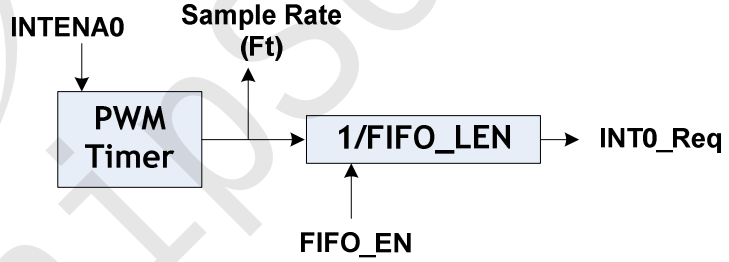
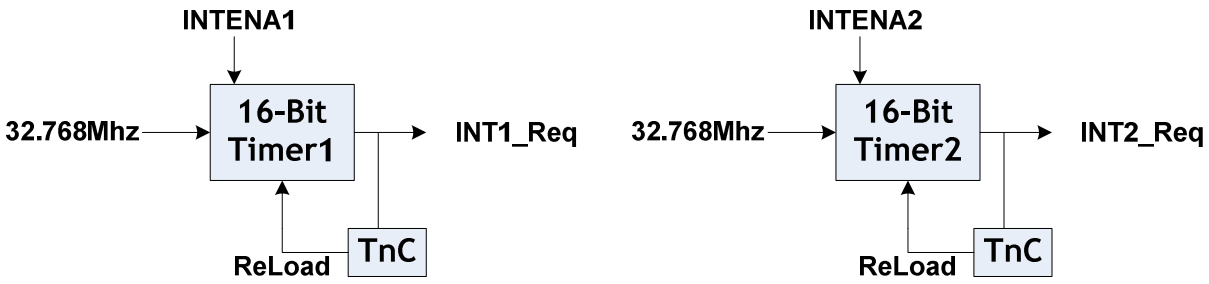


Figure 7.1 Audio PWM Timer Structure

7.1.2 Timer1 & Timer2

The clock source of Timer1 & Timer2 comes from fixed 32.768Mhz or External Clock Input, It contains 16-bit write-only counter register. If Timer enable correspond with the INTENA bit is turned on then counting to time out, an interrupt request will be generated. At the same time, TnC will be reloaded into Timer register and up-count again. If the global interrupt enable, an interrupt signal is generated at the next clock.



Int1_Req / Int2_Req = (32.768Mhz) / (TnC+1)

Figure 7.2 Timer1 & Timer2 Structure

7.1.3 RTC(Real Time Clock) Timer

The RTC Timer input frequency can select Crystal 32K (32768Hz) or Low power RC oscillator 32768Hz -10%@1.8V ~ +10%@5.5V (LP32K). It contains 16-bit counter register. RTC generates interrupt request or wake-up MCU when in halt mode or interrupt in normal mode. The wake-up function can be disabled by option.

The frequency of Int3_Req = 32768Hz / (RTC Timer TnC+1)

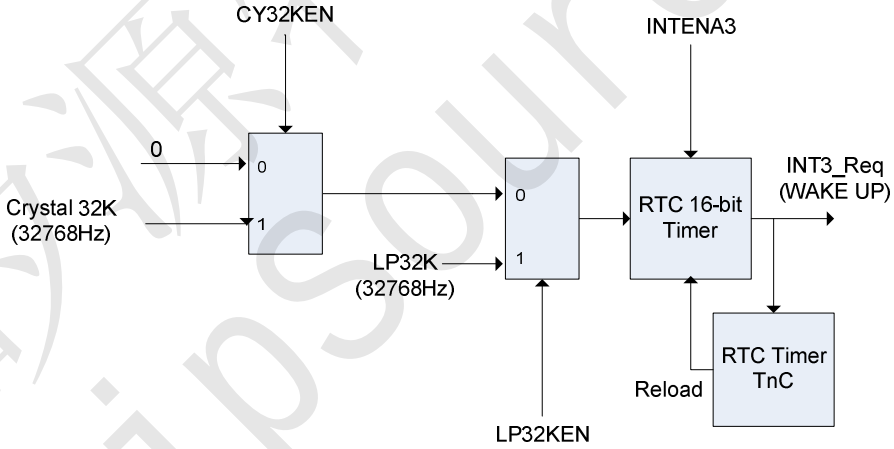


Figure 7.3 RTC Timer Structure

7.2 General Purpose I/O Ports

The TR16F096A(B) provides 4 I/O ports for user application. There are four I/O port, PA0~PA5, PB0~PB7, PC0~PC7 and PI0~PI1. The input/output bits programmable by IOC control register respectively. PA0~PA5, PB0~PB7, PC0~PC7 wake-up function enable or disable by user program. PortB3 / PortC0 and PortC3 / PortB1 are external interrupt pins. The pull-up 200K or The Pull-Down 100K or 200K or 500K resistor of each pin can be programmed by user program.

The basic I/O schematic is showed in Figure 7.4.

Common I/O registers

Symbol	Adr	Reset	RW	B15/b7	b14/b6	b13/b5	b12/b4	B11/b3	B10/b2	b9/b1	b8/b0	Description
IOC_PA	04H	00	R/W	IOC_PA[5:0]								"1"= out, "0" = in of related PA bit
IOC_PB	05H	00	R/W	IOC_PB[7:0]								"1"= out, "0" = in of related PB bit
IOC_PCI.L	06H	00	R/W	IOC_PC[7:0]								"1"= out, "0" = in of related PC bit
IOC_PCI.H	06H	00	R/W	IOC_PI[1:0]				-				1"= out, "0" = in of related PI bit
PortA	07H	XX	R/W	PortA[5:0]								Read: in port Write: out port
PortB	08H	XX	R/W	PortB[7:0]								Read: in port Write: out port
PortCI.L	09H	XX	R/W	PortC[7:0]								Read: in port Write: out port
PortCI.H	09H	XX	R/W	PortI[1:0]				-				Read: in port Write: out port

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
PA_PDEN	05H	00	W	PA_PDEN[5:0]								PortA Pull Down Enable
PB_PDEN	06H	00	W	PB_PDEN[7:0]								PortB Pull Down Enable
PCI_PDEN.L	07H	00	W	PC_PDEN[7:0]								PortCI Pull Down Enable
PCI_PDEN.H	07H	C0	W	PI_PDEN[1:0]		-	-	-				PortCI Pull Down Enable ***(PortI default : Enable PD100K)***
PA_PUEN	08H	00	W	PA_PUEN[5:0]								PortA Pull Up Enable
PB_PUEN	09H	00	W	PB_PUEN[7:0]								PortB Pull Up Enable
PCI_PUEN.L	0AH	00	W	PC_PUEN[7:0]								PortCI Pull Up Enable
PCI_PUEN.H	0AH	00	W	PI_PUEN[1:0]		-	-	-				PortCI Pull Up Enable
PA_PDSEL	0BH	00	W	PA_PDSEL[5:0]								PortA Pull Down Select
PB_PDSEL	0CH	00	W	PB_PDSEL[7:0]								PortB Pull Down Select
PCI_PDSEL.L	0DH	00	W	PC_PDSEL[7:0]								PortCI Pull Down Select
PCI_PDSEL.H	0DH	00	W	PI_PDSEL[1:0]		-	-	-				PortCI Pull Down Select
PA_TOUCH	0EH	00	W	PA_TOUCH[5:0]								PortA Touch Enable
PB_TOUCH	0FH	00	W	PB_TOUCH[7:0]								PortB Touch Enable
PCI_ TOUCH.L	10H	00	W	PC_TOUCH[7:0]								PortCI Touch Enable
PCI_ TOUCH.H	10H	00	W	PI_TOUCH[1:0]		-	-	-				PortCI Touch Enable
PA_ODEN.L	11H	00	W	PA_ODEN[5:0]								PortA Open Drain Enable
PA_ODEN.H	11H	00	W			PA5_ HCEN						PortA5 High Current Enable
PB_ODEN	12H	00	W	PB_ODEN[7:0]								PortB Open Drain Enable
PCI_ ODEN.L	13H	00	W	PC_ODEN[7:0]								PortCI Open Drain Enable
PCI_ ODEN.H	13H	00	W	-		-	-	-				PortCI Open Drain Enable
WAKEN_PA	14H	00	W	PortA_WAKEN[5:0]								PortA WAKE UP Enable
WAKEN_PB	15H	00	W	PortB_WAKEN[7:0]								PortB WAKE UP Enable
WAKEN_PC	16H	00	W	PortC_WAKEN[7:0]								PortC WAKE UP Enable
WAKELV_PA	17H	00	W	PortA_WAKELV[5:0]								PortA WAKE UP Edge "1"= Pos-Edge, "0" = Neg-Edge of related PA bit
WAKELV_PB	18H	00	W	PortB_WAKELV[7:0]								PortB WAKE UP Edge "1"= Pos-Edge, "0" = Neg-Edge of related PB bit
WAKELV_PC	19H	00	W	PortC_WAKELV[7:0]								PortC WAKE UP Edge "1"= Pos-Edge, "0" = Neg-Edge of related PC bit
WAKEDLV_PB	1AH	00	W	PortB_WAKEDLV[3:0]								PortB Double-Edge WAKE UP Enable

These totally 24 I/O pins work not only just a general input/output port function but also can be configured as UART, SPI master/slaver, ADC analog input, I2C master/slaver, Microphone, External Crystal, External interrupt etc. For more detail please refer to relative section.

The pull-down resistor and the pull-up resistor of each pin can be selected by program. If pull-down 100K resistor is enabled and input voltage is logical high, the pull-down 1M ohm resistor is selected; otherwise, the pull-down 100K ohm resistor is selected.

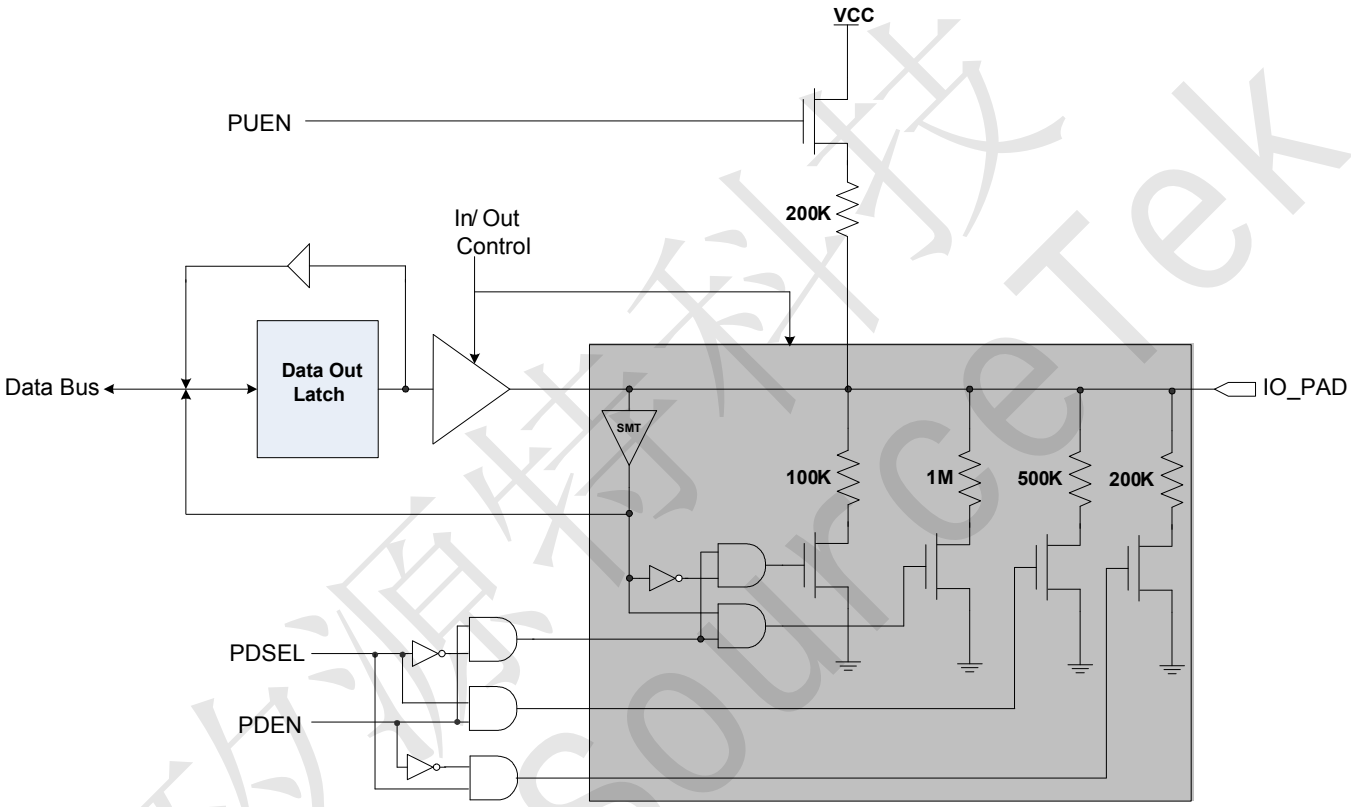


Figure 7.4 Basic I/O Configuration

PDEN = 0 and PDSEL = 0	**Disable Pull Down R**
PDEN = 0 and PDSEL = 1	**Pull Down POLY R 200K** **(Resistance value is not affected by high or low voltage)**
PDEN = 1 and PDSEL = 0	**Pull Down MOS R 100K** **(Resistance value is affected by high or low voltage)**
PDEN = 1 and PDSEL = 1	**Pull Down MOS R 500K** **(Resistance value is affected by high or low voltage)**

PUEN = 0	**Disable Pull Up R**
PUEN = 1	**Pull Up POLY R 200K** **(Resistance value is not affected by high or low voltage)**

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
WAKEDLV_PB	1AH	00	W	PortB_WAKEDLV[3:0]								PortB Double-Edge WAKE UP Enable

PB0, PB1, PB2 and PB3 support two edge mode which is rising and falling edge trigger for wake-up function. The rising and falling edge trigger is selected by user program.

The PortB0, PortB1, PortC0, PortC1, PortB4, PortB5 also provides 3 comparators configuration for user application that each comparator enable or disable by program. The output of comparator is bit13 and bit14 and bit15 of system miscellanea register #3.

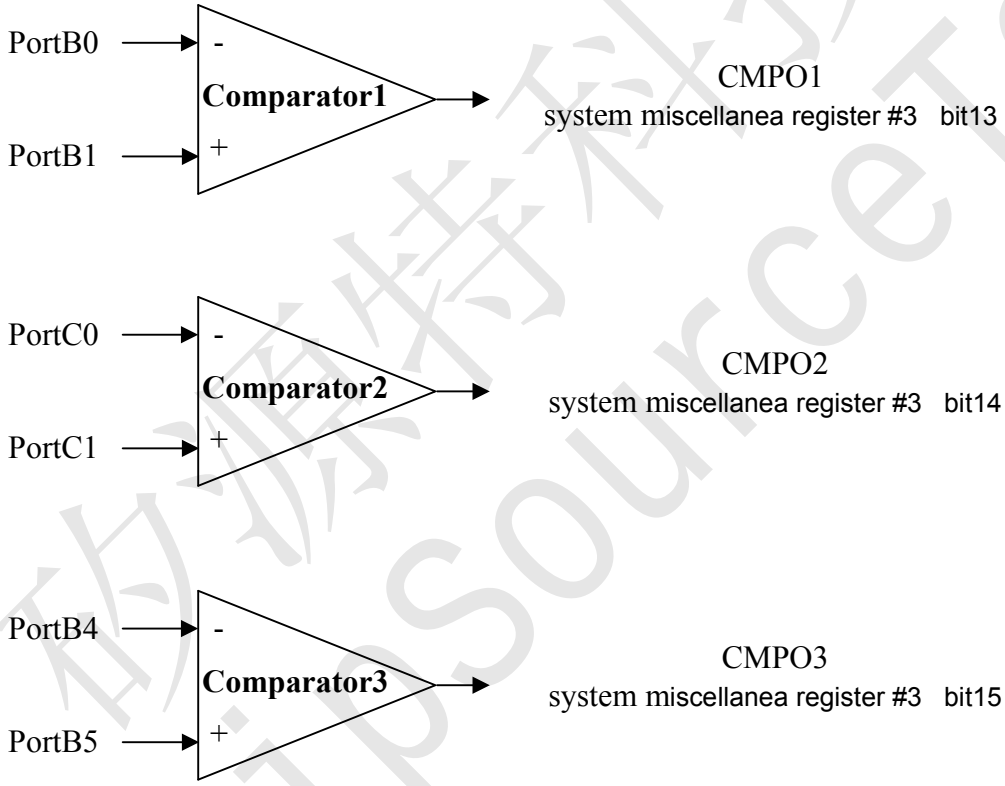


Figure 7.5 Comparator Configuration

7.3 Extension Device

TR16F096A(B) built-in special hardwires for external device connection capability are listed below:

7.3.1 SPI Master Controller

In order to enable SPI Master Controller interface, user should set STATUS.b8 = 1 before SPI Master Controller operation.

7.3.1.1 Features

- Serial clock rate: 16.384 MHz / 8.192 MHz / 4.096 MHz
- Support four standard SPI modes
- Built in 4x16 bits data buffer

I/O Port	SPI interface	Direction	Description
PortA.3 / PortB.3	SO	I	Serial Flash Data output
PortA.1 / PortB.1	SI	O	Serial Flash Data input
PortA.0 / PortB.0	SCK	O	Serial Clock
PortA.2 / PortB.2	CS	O	Chip Select(free assign by user)

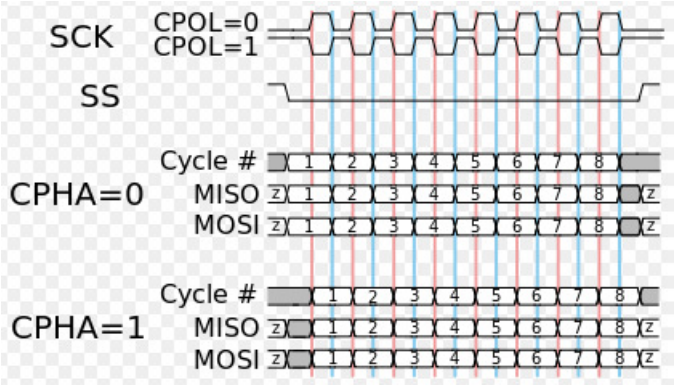
7.3.1.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	B14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.L	0DH	01	W	-	-	RCV	SEND	Total Send/Receive Byte				Write Control Register Low Byte
CTRL_W.H	0DH	00	W	CPOL	CPHA	CKSEL		ICS	-	-		Write Control Register High Byte
CTRL_R.L	0DH	01	R	DATOK	0	RCV	SEND	Total Send/Receive Byte				Read Control Register Low Byte
CTRL_R.H	0DH	00	R	CPOL	CPHA	CKSEL		ICS	-	-		Read Control Register High Byte

Item	Description
Total Send/Receive Byte	Default:1 , Total byte number of sending or receiving
SEND	Trigger sending data
RCV	Trigger receiving data.
ICS	Internal SPI command select enable
CKSEL	00: N/A , 01: 16.384MHz , 10: 8.192 MHz , 11: 4.096 MHz
CPHA	Clock Phase
CPOL	Clock Polarity
DATOK	Indicate transmit/receive data O.K

SPI Modes

SPI Mode	Conditions	Leading Edge	Trailing eDge
0	CPOL=0, CPHA=0	Sample (Rising)	Setup (Falling)
1	CPOL=0, CPHA=1	Setup (Rising)	Sample (Falling)
2	CPOL=1, CPHA=0	Sample (Falling)	Setup (Rising)
3	CPOL=1, CPHA=1	Setup (Falling)	Sample (Rising)



Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
DATA_W	0EH	XX	W	DATA[15:0]								Write Transmission Data Value
DATA_R	0EH	XX	R	DATA[15:0]								Read Received Data Value

DATA [15:0]: Transmit/Receive Data Value

7.3.2 SPI Slaver Controller

In order to enable SPI Slave Controller interface, user should set STATUS.b9 = 1 before SPI Slave Controller operation.

7.3.2.1 Features

- Support Input Serial clock rate (Max): 8.192 MHz
- Built in ping-pong data buffer to improve transfer efficiency

I/O Port	SPI interface	Direction	Description
PortB.3 / PortA.3	SO	O	Serial Data output
PortB.1 / PortA.1	SI	I	Serial Data input
PortB.0 / PortA.0	SCK	I	Serial Clock input
PortB.2 / PortA.2	CS	I	Chip Select

7.3.2.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	B14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.L	0BH	00	W	-	-	NEW_ MODE	-	-	Overrun Error Check Enable	MODE_SEL[1:0]		Write Control Register Low Byte
CTRL_R.L	0BH	00	R	-	-	NEW_ MODE	CS	Overrun Error -	Overrun Error Check Enable	MODE_SEL[1:0]		Read Control Register Low Byte

Item	Description
MODE_SEL[1:0]	Word/Byte Mode Select (10: Word Mode Enable , 01:Byte Mode Enable)
Overrun Error Check Enable	Enable Check RX buffer Overrun Error
Overrun Error	RX buffer Overrun Error happen
CS	user program can read CS status through this bit
NEW_ MODE	Default:0 , CS falling will reset TX / RX state machine.

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
DATA_W	0CH	XX	W	DATA[15:0]								Write Transmission Data Value
DATA_R	0CH	XX	R	DATA[15:0]								Read Received Data Value

DATA [15:0]: Transmit/Receive Data Value

7.3.3 High Speed 8 channel / 12 bits SAR ADC

7.3.3.1 Features

- 8 external I/O input Channels
- 12-bit SAR ADC
- Up to 200K samples per second (@ACQT = 2*TAD, ADC clock = 4Mhz)
- Programmable acquisition time
- ADC start conversion by S/W, Timer, RTC or External I/O pin

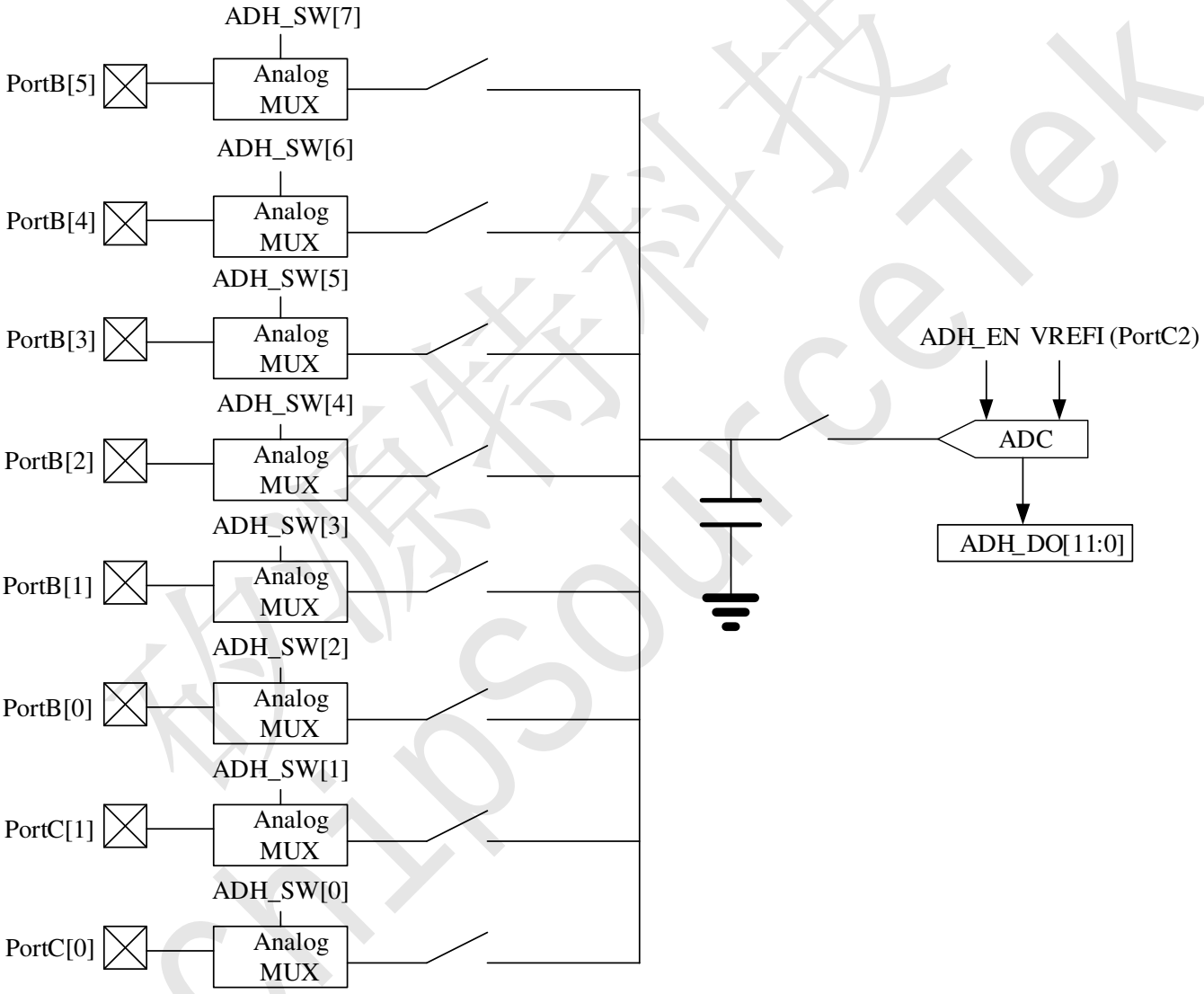


Figure 7.6 High speed 8-Channels / 12-bits ADC Structure Diagram

Note: If user need more precise ADC for application, user can set "ADC vref input" to enable VREFI at option. If ADC Verf input is enabled, PortC2 must be connected 20~100ohm resistor to VCC and 47uF capacitor to AVSS.

Note: Enable ADC verf input at option, PortC2 is as ADC voltage-reference input (VREFI), not as I/O pin.

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7.3.3.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_CFG0.L	40H	00	R/W	-	ACQT[2:0]			-	ADCS[2:0]			High Speed 12-bit ADC control0
ADH_CFG0.H	40H	00	R/W	ADH_EN	-	-	-	-	TRGSRC [2:0]			

Item	Description
ADH_EN	High speed 12-bit signed ADC enable bit ***Note: When ADC is used, ADH_EN must always be set. It can avoid PortC2 leakage current at halt mode.***
ADCS[2:0]	High speed ADC clock select bit 000 = 512K 001 = 1M 010 = 2M 011 = 4M others = N/A
TRGSRC[2:0]	Select trigger source 000 = software trigger 001 = PWM 010 = Timer1 011 = Timer2 100 = RTC Timer 101 = PortC[6] 110 = PortB[0]
ACQT[2:0]	A/D acquisition time select bits 000 = N/A 001 = 2 TAD 010 = 4 TAD(default) 011 = 8 TAD 100 = 16 TAD 101 = 32 TAD 110 = 64 TAD 111 = 128 TAD

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_CFG1.L	41H	00	R/W	ADH_SW[7:0]								High Speed 12-bit ADC control1
ADL_CFG1.H	41H	00	R/W	SWTRG	ADH_SW[14:8]							

SWTRG : Software Trigger

1 = Setting this bit starts the A/D conversion cycle.

This bit is automatically cleared by hardware when A/D conversion has completed.

0 = A/D conversion is completed

ADH_SW[14:0] : These PortC[0]、PortC[1] and PortB[5:0] pins associated with the 12-bit A/D Converter can individually be configured as an analog input or digital I/O using the ADH_SW[7:0] registers.

Item	Description
ADH_SW[14]	N/A
ADH_SW[13]	N/A
ADH_SW[12]	N/A
ADH_SW[11]	N/A
ADH_SW[10]	N/A
ADH_SW[9]	VBGO (Band Gap 0.8V)
ADH_SW[8]	Microphone channel
ADH_SW[7]	1 = PortB[5] is channel 7 analog input, 0 = PortB[5] is digital I/O
ADH_SW[6]	1 = PortB[4] is channel 6 analog input, 0 = PortB[4] is digital I/O
ADH_SW[5]	1 = PortB[3] is channel 5 analog input, 0 = PortB[3] is digital I/O
ADH_SW[4]	1 = PortB[2] is channel 4 analog input, 0 = PortB[2] is digital I/O
ADH_SW[3]	1 = PortB[1] is channel 3 analog input, 0 = PortB[1] is digital I/O
ADH_SW[2]	1 = PortB[0] is channel 2 analog input, 0 = PortB[0] is digital I/O
ADH_SW[1]	1 = PortC[1] is channel 1 analog input, 0 = PortC[1] is digital I/O
ADH_SW[0]	1 = PortC[0] is channel 0 analog input, 0 = PortC[0] is digital I/O

Note: If user need to enable more A/D channels than one, user should enable ADC interrupt in order to read A/D conversion data of more channels. When someone channel is converted completely, it will generate an interrupt to CPU. Every active channel is converted sequentially.

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Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_CFG2.L	42H	00	R/W	-	-	-	SIGN	SHIFT4	-	-	-	High Speed 12-bit ADC result
ADH_CFG2.H	42H	00	R/W	-					-			

Item	Description
SHIFT4	Shift ADC data 4 bits 0: ADH_DO[15:0] = {0000,ADC data[11:0]} 1: ADH_DO[15:0] = {ADC data[11:0],0000}
SIGN	Sign ADC data

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_DO.L	44H	00	R	ADH_DO[7:0]								ADC result
ADH_DO.H	44H	00	R	ADH_DO[15:8]								

ADH_DO (Only read): ADC Data Output

Item	Description
SHIFT4 = 0	ADH_DO[15:0] = {0000,12bit ADC data[11:0]}
SHIFT4 = 1	ADH_DO[15:0] = {12bit ADC data[11:0],0000}

7.3.4 UART Controller

In order to enable UART Controller interface, user should set STATUS.b5 = 1 for UART Controller before UART controller operation.

7.3.4.1 Features

- Baud Rate up to 921600
- Even, odd, or no-parity bit generation and detection
- 1-stop bit generation
- Built in TX 4x8 bits data buffer and RX 4x8 bits data buffer

UART I/O Port	UART interface	Direction	Description
PortA.4 / PortB.4	SIN(RX)	I	UART Data input. Which RX IO is selected by IDE option.
PortA.5 / PortB.5	SOUT(TX)	O	UART Data output. Which TX IO is selected by IDE option.

7.3.4.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.L	12H	XX	W	-	-	CLR_ TX_INT	Set_ Baud_ Rate	Parity_ SE	Parity_ EN	RXIRQ En	TXIRQ En	Control Register Low Byte
CTRL_W.H	12H	XX	W	-	-	-	-	-	CLR_Rx Overrun Err	CLR_ INT	-	Control Register High Byte
CTRL_R.L	12H	00	R	TX_INT	0	0	Set_ Baud_ Rate	Parity_ SE	Parity_ EN	RXIRQ En	TXIRQ En	Read Status Low Byte
CTRL_R.H	12H	00	R	Rx ERROR	TX_Buf Empty	RX_Dat aReady	RxParity Err	RxOverr unErr	0	0	RX_INT	Read Status High Byte

Item	Description
TXIRQEn	TX IRQ Enable
RXIRQEn	RX IRQ Enable
Parity_EN	Parity Enable
Parity_SE	0: Odd Parity, 1: Even Parity
Set_Baud_Rate	Set Baud Rate
TX_INT	If this bit is high, TX interrupt happen.
RX_INT	If this bit is high, RX interrupt happen.
RxOverrunErr	RX Overrun Error
RxParityErr	RX Parity Error
RX_DataReady	RX Data Ready Flag
TX_BufEmpty	TX Data Buffer Empty Flag
RxERROR	Receive Data(RX) miss STOP Bit
CLR_ TX_INT	Clear TX_INT Flag
CLR_ INT	Clear interrupt flag
CLR_RxOverrunErr	Clear RxOverrunErr Flag

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Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
DATA_W.L	13H	XX	W	Write_DATA_Buffer[7:0]								Write Data Buffer Low Byte
DATA_W.H	13H	XX	W	Write_DATA_Buffer[15:8]								Write Data Buffer High Byte
DATA_R.L	13H	00	R	RX_DATA[7:0]								Read Received Data Low Byte
DATA_R.H	13H	00	R	0	0	0	0	0	0	0	0	Read Received Data High Byte

OPTION	Write_DATA_Buffer[15:0]															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Set_Baud_Rate = 1	-	-	-	-	-	-	Divisor[9:0]									
Set_Baud_Rate = 0	-	-	-	-	-	-	-	-	TX_DATA[7:0]							

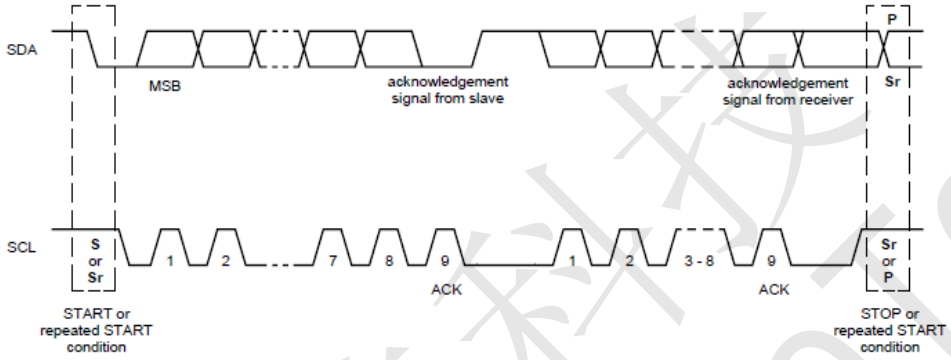
Item	**Description**
TX_DATA[7:0]	Transmit Data Value
RX_DATA[7:0]	Receive Data Value

Baud Rate Table:

Baud Rate	**Divisor (Decimal)**
1200	768
2400	384
4800	192
9600	96
19200	48
38400	24
57600	16
115200	8
230400	4
460800	2
921600	1

7.3.5 I2C Controller

The I2C controller provides master read/write transfer, slave read/write transfer and 7-bit address mode. The multi-master mode, 10-bit address and Hi-speed mode are not supported. Pull-up resistors are required on both SCL and SDA of I2C lines. Typically external 2k~10K Ohm resisters based on he capacitance load are used to pull the signals up to VCC. In order to enable I2C controller, user should set I2C_EN bit in the I2C_CTL register before I2C controller operation. The following diagram shows I2C bus read/write timing.



Data transfer on the I2C

Note:

1. In slaver mode, after I2C_DAT transmit/receive is completed, SCL line hold low until I2C_DAT start to transmit/receive data again.
2. S: A START condition immediately followed by a STOP condition is an illegal format.
3. P: The STOP condition is generated by master, which has previously sent a not-acknowledge(/A)

7.3.5.1 Features

- I2C master/slaver mode with changeable slave address
- Software programmable clock frequency
- Start/Stop/Repeated Start/Acknowledge generation
- Support 7-bit slave addressing mode

I/O Port	I2C interface	Direction	Description
PortB[3]/ PortA[5]	SCL	I/O	I2C serial clock input. Which SCL IO is selected by IDE option.
PortB[2]/ PortA[4]	SDA	I/O	I2C serial data input/output. Which SDA IO is selected by IDE option.

7.3.5.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
I2C_CTL.L	48H	00	W/R	PSCALE[0]	SADDR[6:0]							I2C control register
I2C_CTL.H	48H	00	W/R	I2C_EN	MODE	PSCALE[6:1]						

Item	Description
I2C_EN	I2C controller enable bit
MODE	1 : I2C master mode 0 : I2C slaver mode
PSCALE[6:0]	This register is used to pre-scale the SCL clock frequency(Freq). PSCALE = 64MHz/(10* Freq) -1 Example: desired SCL frequency = 100KHz -> PSCALE = 64MHz/(10*100KHz) – 1 = 63
SADDR[6:0]	In slave mode, Slave Address(SADDR) 7-bit is used to compare with the address that master sending out.

Symbol	Adr	Reset	RW	b7	b6	b5	b4	b3	b2	b1	b0	Description
I2C_DAT.L	49H	XX	W	TXR[7:0]								Transmit Data/Address register
I2C_DAT.H	49H	00	R	RXR[7:0]								Receiver Data/Address register

Item	Description
TXR[7:0]	Transmit Data/Address register
RXR[7:0]	Receiver Data/Address register

Symbol	Adr	Reset	RW	b7	b6	b5	b4	b3	b2	b1	b0	Description
I2C_CMD.L	4AH	XX	W				STA	STO	RD	WR	ACK	I2C command register

I2C_CMD Command register generates the related I2C control signal in the master mode only.

Item	Description
STA	generate (repeated) start condition timing
STO	generate stop condition timing
RD	read from slave device
WR	write to slave device
ACK	After master device receives the data of slave device, master will generate an ACK signal to slaver device. 1 = generate an NACK signal at 9th SCL. 0 = generate an ACK signal at 9th SCL.

Symbol	Adr	Reset	RW	b7	b6	b5	b4	b3	b2	b1	b0	Description
I2C_SR.L	4AH	00	R				RW	MATCH	TYPE	ACK	BUSY	I2C status register

Item	Description
RW	This R/W bit information is valid only from the address match to the next start bit or stop bit. 1 = Read status 0 = Write status
MATCH	Slave Address Match. 1 = match 0 = not match
TYPE	Data/Address type. 1 = indicate the last byte received or transmitted was ADDRESS. 0 = indicate the last byte received or transmitted was DATA.
ACK	In master mode, acknowledge is received from slave device. In slaver mode, acknowledge is received from master. 1 = No acknowledge received 0 = Acknowledge received
BUSY	Transfer in progress. 1 = transmit/receive in progress 0 = transmit/receive complete

7.3.6 IR 38KHz Modulation

I/O Port	IR	Direction	Description
PortB.4 / PortA.4	IR 38K	O	IR 38K Output. Which IR IO is selected by bit10 of system miscellanea register #1.

1. IR function is enabled by bit11 of system miscellanea register #1.
2. Which IR IO is selected by bit10 of system miscellanea register #1.
3. PortB4 combine 38 KHz modulator with register DATA_PB bit 4. PortB4 will output 38 KHz clock signal when PortB4 is configured as output port and DATA_PB bit4 = 1. In contrast, PortB4 output low when PortB4 is configured as output port and DATA_PB bit4 = 0. The PortB4 output pad will be forced to low state.
4. PortA4 combine 38 KHz modulator with register DATA_PA bit 4. PortA4 will output 38 KHz clock signal when PortA4 is configured as output port and DATA_PA bit4 = 1. In contrast, PortA4 output low when PortA4 is configured as output port and DATA_PA bit4 = 0. The PortA4 output pad will be forced to low state.

7.3.7 Touch Controller

7.3.7.1 Features

- Touch controller with one dedicated comparator
- Use Real-T counter to count the output pulse width of comparator
- Provides an interrupt for efficient programming.

7.3.7.2 Control Registers

◆System Miscellanea register #4

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC4.L	19H	00	R/W	TOUCH_REALT	TINT_EN	TIS		SVT	THEN	PREC	CMP3EN	System miscellanea register #4
MISC4.H	19H	00	R/W	CY32K_STAB	DAC_OG			InterPLY_EN	Tone_Mode	InterPLY_FUN		

Item	Description
TOUCH_REALT	Touch with Real-T function 0:disable & clear real-T stop flag 1:enable
TINT_EN	Touch INT Enable
TIS	Touch I/O Port input select , 00: NA, 01:PortA, 10:PortB, 11:PortC
SVT	Touch SVT , 0: 1/4*VCC, 1: 1/2*VCC
THEN	Touch Enable
PREC	Touch Pre-charge 1.5V

◆System Miscellanea register #5

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC5.L	18H	00	R/W	THO	LVDO	CMP2_TIMER2	CMP1_TIMER1	CMP2_INT_INV	CMP1_INT_INV	CMP2_INT_EN	CMP1_INT_EN	System Miscellanea register #5
MISC5.H	18H	00	R/W	InterPLY_FREQ_DIV								

Item	Description
THO	Touch Comparator Output (Read Only)

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
PA_TOUCH	0EH	00	RW	PA_TOUCH[5:0]								PortA touch enable bit
PB_TOUCH	0FH	00	RW	PB_TOUCH[7:0]								PortB touch enable bit
PCI_TOUCH	10H	00	RW	PC_TOUCH[7:0]								PortC0~ PortC7 touch enable bit

If THEN is set high, PA_TOUCH, PB_TOUCH and PCI_TOUCH registers are used to set the corresponding touch enable bit of PortA, PortB and PortC.

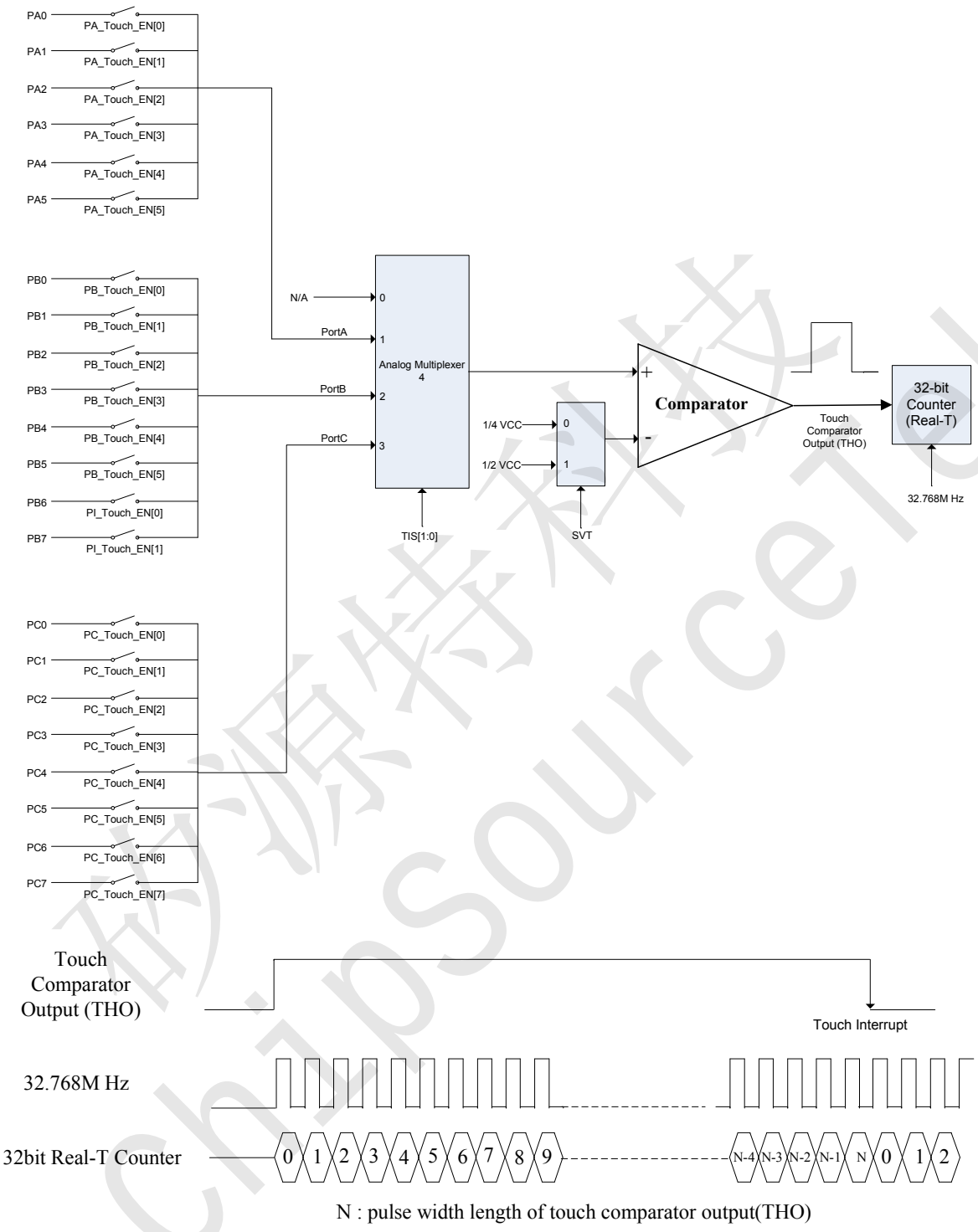


Figure 7.7 Touch Controller Structure

7.3.8 PIR / CDS / OPA

7.3.8.1 Features

- Built-in 2-stage Operational Amplifier
- Built-in Window Comparator for Two Independent Voltage Monitors
- Built-in Internal Reference Voltages for OP amps and Comparators
- Provide Adjustable Turn on Delay Timer and Stable Timer
- Support PIR motion sensor and CDS night sensor
- Support two OPAs mode
- Built-in de-bounce Circuit
- Can work in sleep mode and wake up

7.3.8.2 Control Registers

◆System Miscellanea register #6

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC6.L	15H	00	R/W	DEB_ ININV	DEB_ INTEN	DEB_ WKEN	DEB_ EN	OPA2_ EN	OPA1_ EN	LDO24 EN	PIR_EN	System Miscellanea register #6
MISC6.H	15H	00	R/W	DEB_ OUT	PIR_ CMPO	CDS_ EN	DEB_INSEL			DEB_CLKSEL		

Item	Description
DEB_OUT	Debounce Output (Read Only)
PIR_CMPO	PIR Comparator Output (Read Only)
CDS_EN	Default:0 , CDS Function Enable
DEB_INSEL	Debounce Input Select, See Figure7.8 Debounce Input Source
DEB_CLKSEL	Debounce Clock Select 00: LP1000Hz , 01: LP32768Hz, 10: System Clock , 11: 32.768 MHz
DEB_ININV	Default:0 , Debounce Input Inverse
DEB_INTEN	Default:0 , Debounce Interrupt Enable
DEB_WKEN	Default:0 , Debounce Wake Up Enable
DEB_EN	Default:0 , Debounce Function Enable
OPA2_EN	Default:0 , OPA 2 Enable
OPA1_EN	Default:0 , OPA 1 Enable
LDO24EN	Default:0 , LDO 2.4V Output Enable
PIR_EN	Default:0 , PIR Function Enable

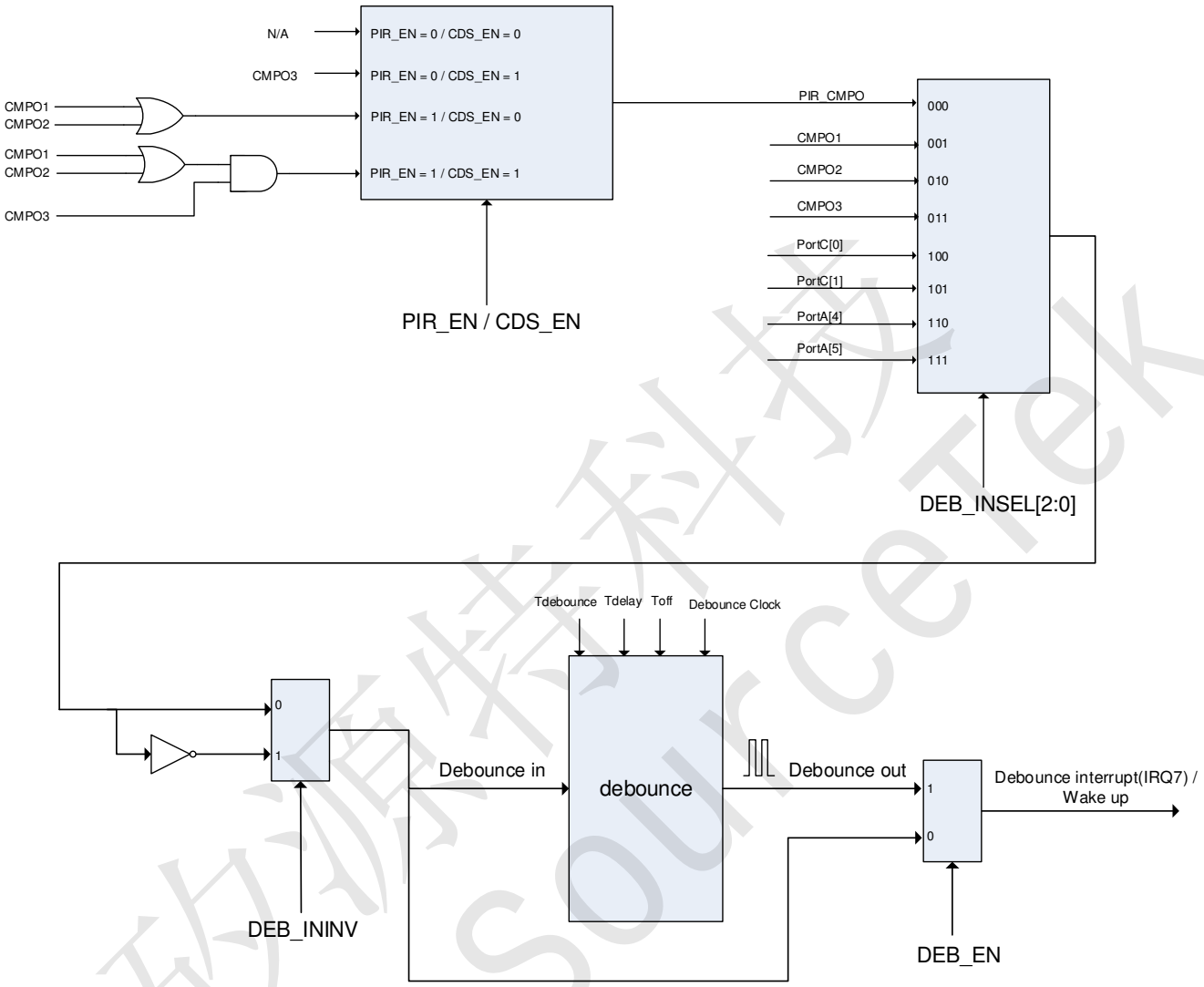


Figure 7.8 De-bounce Input Source

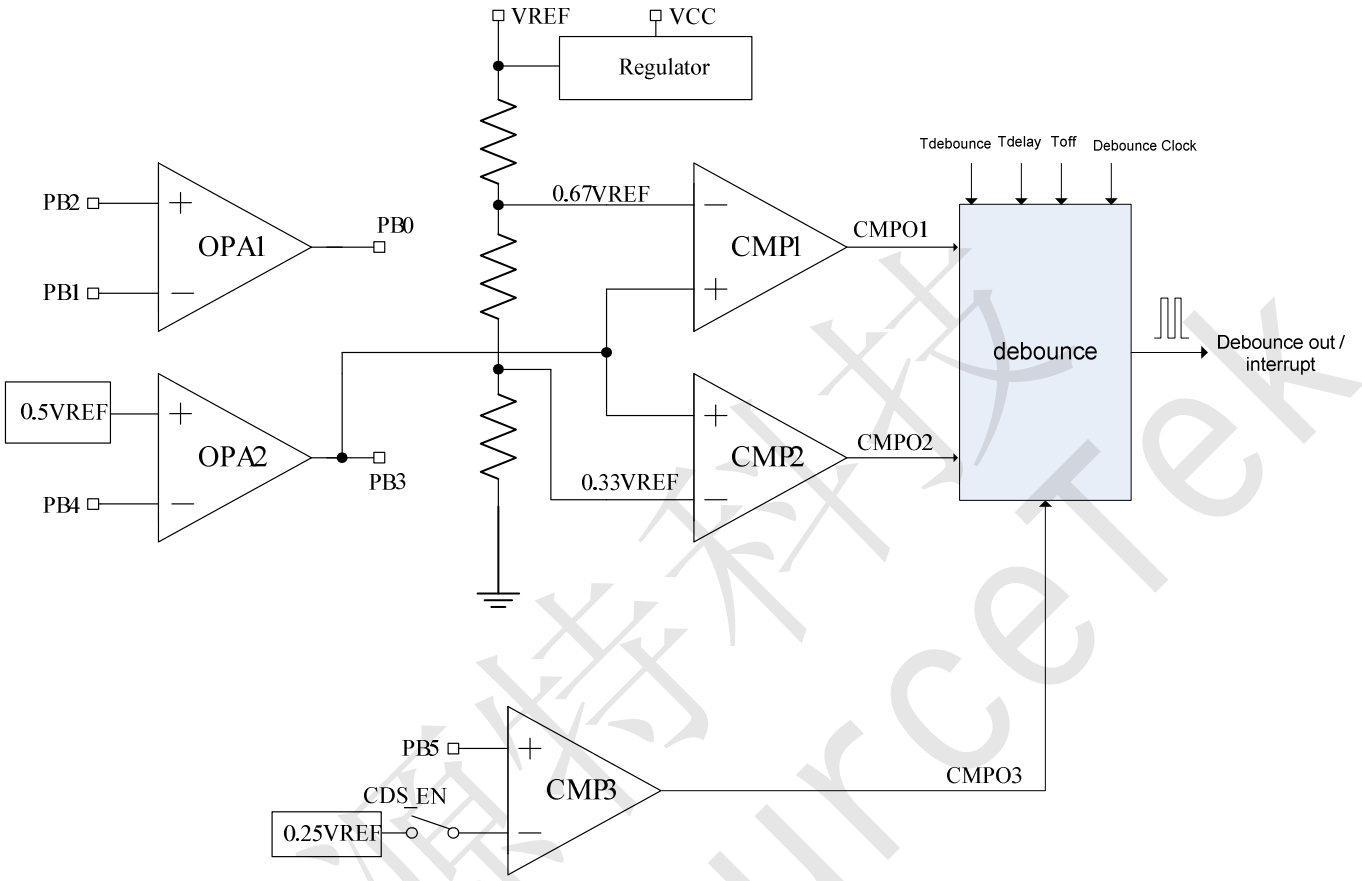


Figure 7.9 PIR / CDS Structure

Notice: OPA1 and OPA2 will be low power operation in PIR mode. So the external resistor of OPA should use high impedance resistor (above 1M ohm).

Notice: If PIR_EN (bit0 of MISC6) is enable, OPA1 and OPA2 will be enabled automatically.

Caution : OPA1_EN (bit2 of MISC6) and OPA2_EN (bit3 of MISC6) must be set to "0" in PIR MODE.

Conditions:

1. PIR mode without CDS: LDO33EN=1, OPA1_EN=0, OPA2_EN=0, PIR_EN=1, CDS_EN=0, CMP1EN=1, CMP2EN=1
2. PIR mode with CDS: LDO33EN=1, OPA1_EN=0, OPA2_EN=0, PIR_EN=1, CDS_EN=1, CMP1EN=1, CMP2EN=1, CMP3EN=1

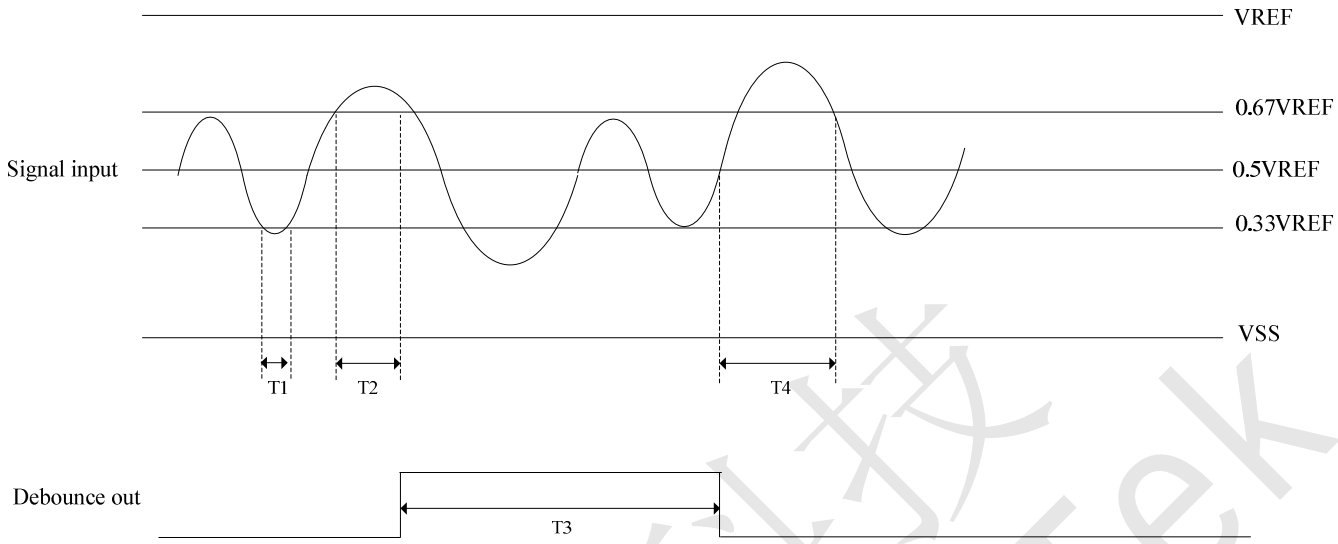


Figure 7.10 De-bounce for PIR Timing Diagram

T1: When the signal voltage is less than 0.33VREF or greater than 0.67VREF, if the length of time is less than Tdebounce, the system is unresponsive.

T2: When the signal voltage is less than 0.33VREF or greater than 0.67VREF, if the length of time is greater than Tdebounce, the system outputs high.

T3: The system outputs high during Tdelay time.

T4: When the system output is turned off, no input signals is accepted during Toff time

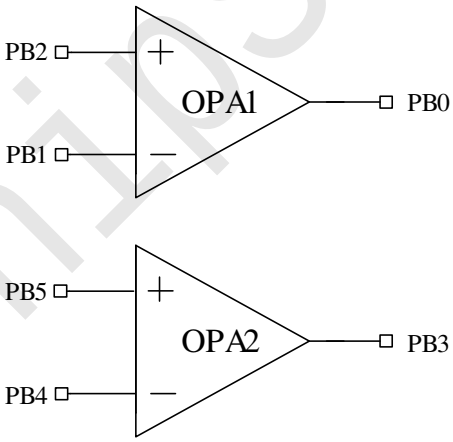


Figure 7.11 Two OPAs mode

Conditions: Two OPAs mode: OPA1_EN=1, OPA2_EN=1

Notice: OPA1 and OPA2 cannot be use alone.

7.3.9 High quality 16bit Σ-Δ ADC

7.3.9.1 Features

- High quality 16-bit Σ-Δ ADC
- Up to 32K samples per second
- Differential input for microphone channel

Note: PortB6(SDAVMID) must be connected 0.1uF capacitor to AVSS and as close as possible to the IC.

Note: AVCC must be connected 0.1uF capacitor to AVSS and as close as possible to the IC.

7.3.9.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH2_CFG0.L	4BH	00	R/W	-	-	-	-	UNSIGN	DSM_ SEL	ADH2_ IEN	ADH2_ EN	16-bit ADC control0
ADH2_CFG0.H	4BH	00	R/W	START	-	-	-	-	-	-	-	

Item	Description
ADH2_EN	16bit ADC enable bit
ADH2_IEN	16bit ADC interrupt enable bit (IRQ13)
DSM_SEL	Delta-Sigma module output select 0 : DSNO 1 : DSPO
UNSIGN	0:SIGN ADC data 1:UNSIGN ADC data
START	Setting this bit starts the ADC conversion cycle

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH2_CFG1.L	4CH	00	R/W	ADH2_SW[7:0]								16-bit ADC control1
ADH2_CFG1.H	4CH	00	R/W	-	-	-	-	-	-	-	ADH2_SW[8]	

Item	Description
ADH2_SW[8]	Microphone channel
ADH2_SW[7]	N/A
ADH2_SW[6]	N/A
ADH2_SW[5]	N/A
ADH2_SW[4]	N/A
ADH2_SW[3]	N/A
ADH2_SW[2]	N/A
ADH2_SW[1]	N/A
ADH2_SW[0]	N/A

Note: Only someone A/D channels can be select to convert. When someone channel is converted completely, it will generate an interrupt to CPU.

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH2_CFG2.L	4DH	00	R/W	ADH2_FREQ_DIV								16-bit ADC control2
ADH2_CFG2.H	4DH	00	R/W	-	-	-	-	-	-	-	-	

Item	Description
ADH2_FREQ_DIV	16bit ADC Frequency Divisor. Minimum value 15 (0xF)

16bit ADC clock frequency = 65536K Hz / (ADC_FREQ_DIV + 1)

ADC interrupt frequency = 16bit ADC clock frequency / 128

Example: ADC_FREQ_DIV = 15 (0x0F)

16bit ADC clock frequency = 65536K Hz / (15 + 1) = 4096 K Hz

ADC interrupt frequency = 4096 K Hz / 128 = 32 K Hz

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH2_DO.L	4FH	00	R	ADH2_DO[7:0]								16-bit ADC result
ADH2_DO.H	4FH	00	R	ADH2_DO[15:8]								

ADH2_DO (Only read): 16bit ADC Data Output

7.3.10 TRA1402 Interface

In order to enable Tritan TRA1402 Audio Recording interface, user should set TRA_EN bit in the TRA_CFG register before TRA1402 controller operation.

7.3.10.1 Features

- SCLK pin can set as floating status by setting CKF bit in the TRA_CFG register
- The bit number of parallel-to-serial / serial-to-parallel converter is up to 16 for the TRA1402 write/read data.

I/O Port	TRA1402 interface	Direction	Description
PortB[2]	SYNC	O	TRA1402 32K(32000Hz) SYNC output
PortB[1]	DIO	I/O	TRA1402 data input and output
PortB[0]	SCLK	I	TRA1402 clock input

7.3.10.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
TRA_CFG.L	46H	00	W/R	SYNC_EN	CKSEL	CKF	BitNum[4:0]					TRA1402 control register
TRA_CFG.H	46H	00	W/R	TRA_EN			TRA_INT_EN	FIFO_MODE	Auto_Polling	RCV	SEND	
TRA_DAT.L	47H	00	W/R	TRA_DAT[7:0]								TRA1402 data register
TRA_DAT.H	47H	00	W/R	TRA_DAT[15:8]								

TRA_EN: TRA1402 interface enable bit

TRA_INT_EN: TRA1402 interrupt enable

SYNC_EN: TRA1402 interface 32K(32000Hz) SYNC output enable bit

RCV:

1 = Setting this bit starts to receive data. This bit is automatically cleared by hardware when receiving data has completed.

0 = receiving data is completed

SEND:

1 = Setting this bit starts to send data. This bit is automatically cleared by hardware when sending data has completed.

0 = sending data is completed

Note: Both SEND and RCV are simultaneously set to one which is prohibited.

CKSEL: Select SCLK clock speed

0 = 8M clock speed (default)

1 = 16M clock speed

CKF:

0: the output of SCLK pin is controlled by hardware.

1: the output of SCLK pin is floating.

BitNum: bit number of sending or receiving, range from 1 to 16

TRA_DAT:

W: write transmission Left-Justified data TRA_DAT[15:0] to TRA1402.

R: Read received Left-Justified data TRA_DAT[15:0] from TRA1402

Auto_Polling: Enable Auto-Polling mode. (See Figure 7.13)

Continuously polling tra1402 status bit **FEPT/DRDYEN** by hardware and generate interrupt when reading tra1402 status bit **FEPT/DRDYEN** is high**.**

FIFO_MODE:

1: Auto Polling tra1402 status bit **FEPT** on tra1402 FIFO mode.

0: Auto Polling tra1402 status bit **DRDYEN** on tra1402 Non-FIFO mode.

Auto_Polling	FIFO_MODE	Function Description
0	X	Disable Auto-Polling mode
1	0	Auto Polling tra1402 status bit **DRDYEN** on tra1402 Non-FIFO mode
1	1	Auto Polling tra1402 status bit **FEPT** on tra1402 FIFO mode

Note: It not necessary for generating interrupt at Auto-Polling mode that TRA_INT_EN is set to high .

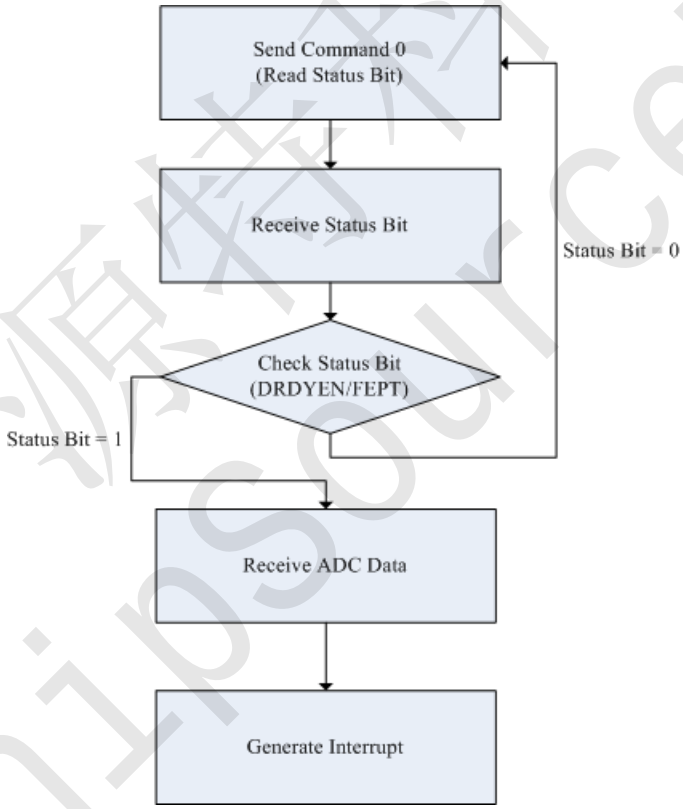


Figure 7.12 Auto-Polling Mode

7.4 Audio Output

7.4.1 Stereo 16-bit PWM Output

One 16-bit of audio PWM is built-in TR16F096A(B) for audio application. Audio output pin PWMP and PWMN are connected to speaker directly. This amplifier can be used to direct drive 8 ohm speaker without any external circuit.

Common I/O registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	B13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
Audio-PWML	16H	XX	W	Audio-PWML [15:0]								Audio-PWM Audio L Channel
Audio-PWMR	17H	XX	W	Audio-PWMR [15:0]								Audio-PWM Audio R Channel

7.4.2 Mono 16-bit DAC Output

One 16-bit of digital-to-analog converter (DAC) is built-in TR16F096A(B) for mono audio application. In order to get more output power driving, which require external amplifier is need.

Common I/O registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	B13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
Audio-DAC	16H	XX	W	Audio-DAC [15:0]								16-bit DAC Audio Channel

◆System Miscellanea register #4

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC4.L	19H	00	R/W	TOUCH_REALT	TINT_EN	TIS		SVT	THEN	PREC	CMP3EN	System miscellanea register #4
MISC4.H	19H	00	R/W	CY32K_STAB	DAC_OG			InterPLY_EN	Tone_Mode	InterPLY_FUN		

Item	Description
DAC_OG	Default:0, DAC output gain = 1

7.4.3 DAC Interpolation Control

One DAC interpolation control unit is built-in TR16F096A(B), in order to reduce quantization noise and improve sound quality at DAC audio output.

◆System Miscellanea register #4

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC4.L	19H	00	R/W	TOUCH_REALT	TINT_EN	TIS		SVT	THEN	PREC	CMP3EN	System miscellanea register #4
MISC4.H	19H	00	R/W	CY32K_STAB	DAC_OG			InterPLY_EN	Tone_Mode	InterPLY_FUN		

Item	Description
InterPLY_EN	0:DAC Interpolation disable 1: DAC Interpolation enable
Tone_Mode	0:TONE disable 1:TONE enable(Sin wave output)
InterPLY_FUN	0:DAC Interpolation disable 1: DAC Interpolation 8 point 2:DAC Interpolation 16 point 3: DAC Interpolation 32 point

◆System Miscellanea register #5

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC5.L	18H	00	R/W	THO	LVDO	CMP2_TIMER2	CMP1_TIMER1	CMP2_INT_INV	CMP1_INT_INV	CMP2_INT_EN	CMP1_INT_EN	System Miscellanea register #5
MISC5.H	18H	00	R/W	InterPLY_FREQ_DIV								

Item	Description
InterPLY_FREQ_DIV	System Frequency Divisor for DAC interpolation, Default:0

Setting this value defines how many System Clocks will produce a smooth interpolated value that will be output directly to the DAC. If the system generates a 32-point interpolation operation, and the DAC value is updated every 32 points. Sampling Rate is set by IDE option.

Example1:

Sampling Rate = 32k Hz, 16-point interpolation

D[7:0](InterPLY_FREQ_DIV) = 65536k Hz / (16 x 32k) = 128(Dec.) / 0x80(Hex.)

Example2:

Sampling Rate = 64k Hz, 32-point interpolation

D[7:0](InterPLY_FREQ_DIV) = 65536k Hz / (32 x 64k) = 32(Dec.) / 0x20(Hex.)

7.5 Auto-FIFO

The Auto-FIFO allows user transfer base on 4-level of data to Audio-PWM. In some case of frame base applications that data transfer is more efficient than sample base. It is advantageous to decrease number of context switch between main program and interrupt service routine (ISR). The FIFO structure reveal as below:

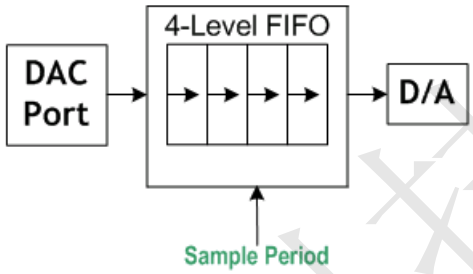


Figure 7.13 Auto FIFO Structure

An interrupt is generated when an entire 4-level FIFO is transfer completed (D\A FIFO buffer is empty), then interrupt service routine should re-load 4-level data to FIFO at ones during 32K or 64K sample period. The FIFO will automatically shift-out data to Audio-PWM at each sample period.

Note: Auto-FIFO is enable/disable by option setup.

8. TR16F096A(B) Flash Control

8.1 Flash Structure

TR16F096A(B) is built in 64Kx16 program/data FLASH memory. This Flash is offered with sector endurance of more than 1,000 cycles, Data retention is rated at greater than 10 years. It is suited for convenient and economical updating of program, configuration, or data memory.

The sector architecture is based on sector size of 256 words/512 bytes. The sector erase operation allows the system to erase the device on a sector. The sector architecture is shown as Figure 8.1.

Sector Select(255 sectors)								Word Select(256 words)							
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Figure 8.1 The sector architecture

8.2 Flash Sector Erase

The Sector Erase instruction needs to assign erasing sector number to AR register. When “PE = AR” instruction is executed, select of sector will be erased.

Example: Erase 16th sector (0x1000 – 0x10FF)

```
AR  = 0x0010   // assign erasing sector number
PE  = AR       // sector erasing
```

Note: Erasing time of one sector is 2.6ms.

8.3 Flash Word Programming

TR16F096A(B) provide one word programming instruction. The Word Programming instruction needs to assign programming data to AR register and assign programming address to P0/P1 register. When “PM[P0/P1] = AR” instruction is executed, select of flash address will be programmed.

Example: Program 16th word address (0x0010)

```
P0.hh = 0x0000
P0 = 0x0010        // assign programming address
AR  = 0x5678       // assign programming data
PM[P0] = AR        // word programming
```

Note: Programming time of one word is 41us.

8.4 Flash Word Read

TR16F096A(B) provide word read instruction. The Word Read instruction needs to assign reading address to P0/P1 register. When “AR = PM[P0/P1] ” instruction is executed, select of word will be read out to AR register.

Example: Read 16th word address (0x0010)

```
P0.hh = 0x0000
P0 = 0x0010          // assign reading address
AR = PM[P0]          // read word data
```

Note: Readng time of one word is two cycles of System Clock.

8.5 Flash unlock/lock for Programming/Erase instruction

Flash unlock instruction need to be executed before flash programming/erase instruction will be executed. This flash unlock instruction is to ensure the safety of the flash operation in order to prevent flash data from being modified by mistake. After the Flash program/erase instruction is executed, the Flash lock instruction needs to be executed to ensure the flash security.

Example1: Flash unlock

```
ENC_DAT    EQU   54H

           ar = 0xdb3f
           io[ENC_DAT] = ar

           ar = 0x8a17
           io[ENC_DAT] = ar
```

Example2: Flash lock

```
ENC_DAT    EQU   54H

           ar = 0x1234
           io[ENC_DAT] = ar

           ar = 0x5678
           io[ENC_DAT] = ar
```

9. TR16F096A(B) Others

9.1 Dynamic System Clock

Operation frequency can be adjusted by software dynamically. User can adjust operation frequency in order to reduce power consumption.

Write Data	CPU Operation frequency
3	8 MHz
4	11 MHz
5	13 MHz
6	14 MHz
7	16 MHz

Example: Change CPU Operation frequency to 13 MHz.

```
SPEED    EQU   67H

         ar = 0x0005;
         io[SPEED]   = ar;
```

9.2 Low Voltage Detector

The voltage detect range of LVD is 1.8V ~ 2.98V for D2ENB = 0 or 2.7V~4.47V for D2ENB=1. When VCC/2 or VCC/3 < VBGI, LVDO=1, otherwise LVDO=0.

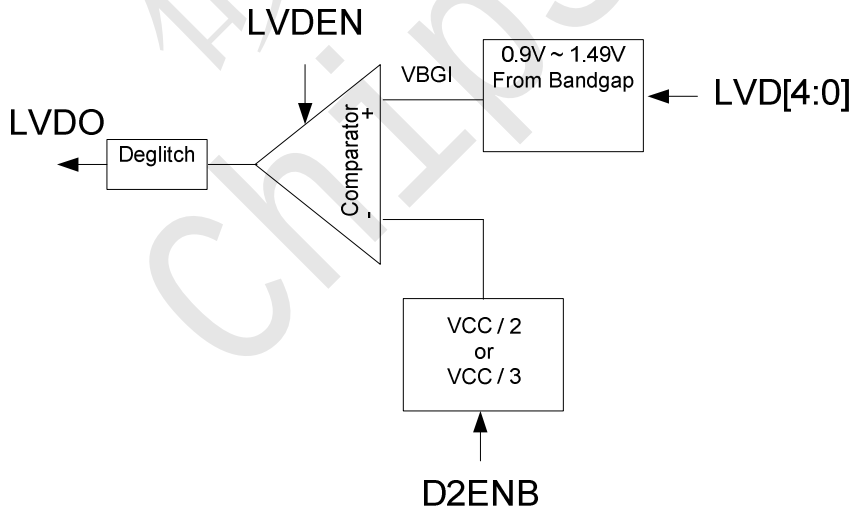


Fig 9.1 Function diagram of LVD

Register	MISC3.b6	MISC3.b7	MISC3.b8~12	MISC5.b6
Control signal	LVDEN	D2ENB	LVD[4:0]	LVDO

LVD [4:0]	D2ENB=0		D2ENB=1		LVD [4:0]	D2ENB=0		D2ENB=1	
	Ideal	Real	Ideal	Real		Ideal	Real	Ideal	Real
0x00	1.80	**1.79**	2.70	**2.68**	0x10	2.44	**2.40**	3.66	**3.59**
0x01	1.84	**1.83**	2.76	**2.74**	0x11	2.48	**2.44**	3.72	**3.65**
0x02	1.88	**1.87**	2.82	**2.79**	0x12	2.52	**2.48**	3.78	**3.70**
0x03	1.92	**1.91**	2.88	**2.85**	0x13	2.56	**2.52**	3.84	**3.76**
0x04	1.96	**1.95**	2.94	**2.91**	0x14	2.60	**2.56**	3.90	**3.82**
0x05	2.00	**1.98**	3.00	**2.96**	0x15	2.64	**2.59**	3.96	**3.87**
0x06	2.04	**2.02**	3.06	**3.02**	0x16	2.68	**2.63**	4.02	**3.93**
0x07	2.08	**2.06**	3.12	**3.08**	0x17	2.72	**2.67**	4.08	**3.99**
0x08	2.12	**2.10**	3.18	**3.13**	0x18	2.76	**2.71**	4.14	**4.05**
0x09	2.16	**2.14**	3.24	**3.19**	0x19	2.80	**2.75**	4.20	**4.10**
0x0A	2.20	**2.18**	3.30	**3.25**	0x1A	2.84	**2.79**	4.26	**4.16**
0x0B	2.24	**2.21**	3.36	**3.30**	0x1B	2.88	**2.82**	4.32	**4.22**
0x0C	2.28	**2.25**	3.42	**3.36**	0x1C	2.92	**2.86**	4.38	**4.27**
0x0D	2.32	**2.29**	3.48	**3.42**	0x1D	2.96	**2.90**	4.44	**4.33**
0x0E	2.36	**2.33**	3.54	**3.48**	0x1E	3.00	**2.94**	4.50	**4.39**
0x0F	2.40	**2.37**	3.60	**3.53**	0x1F	3.04	**2.98**	4.56	**4.44**

It's a COB test result for reference only.

9.3 AGC (Auto Gain Control)

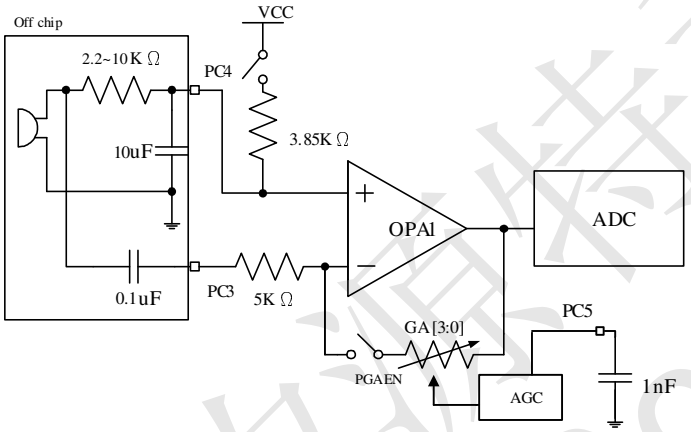
Register	MISC6.b2	MISC2.b7	MISC2.b12
Control signal	OPA1_EN	PGAEN	AGCEN
Mic-pre-amp_PGA	0	1	1

GBB (MISC2.b4)	1	0
PGA GAIN RANGE	17dB~47dB	23dB~53dB

Threshold voltage, detect OPA_OUT voltage level > (VDD-VTH) or < (VSS+VTH)

THR[2:0] (MISC2.b15~b13)	000	001	010	011	100	101	110	111
VTH	0.3V	0.4V	0.45V	0.5V	0.6V	0.7V	0.8V	0.9V

**Mic-preamplifier PGA



AGC function can work on PGA mode only.

Conditions: OPA1_EN=0, PAGEN=1, AGCEN=1, PC5 with capacitor 1nF.

or OPA1_EN=0, PAGEN=1, AGCEN=0, Change GA[3:0] (MISC2.b11~b8) to adjust gain.

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9.4 Microphone

Notice: If Microphone is used, OPA1 and OPA2 need to be disable.

Note: PC3 is microphone pre-amplifier input

Note: PC4 is the bias (VMID) for microphone pre-amplifier

Note: User must use AVCC as power input of 16bit ADC for microphone application.

Note: User must use PC2 (Enable the option of ADC VREF input) as power input of 12bit ADC for microphone application.

Note: Port Cx(Any IO portC pin) must be set to low at sleep mode in order to save power in Fig 9.2.

The standard version (Fig 9.2) is used in the design.

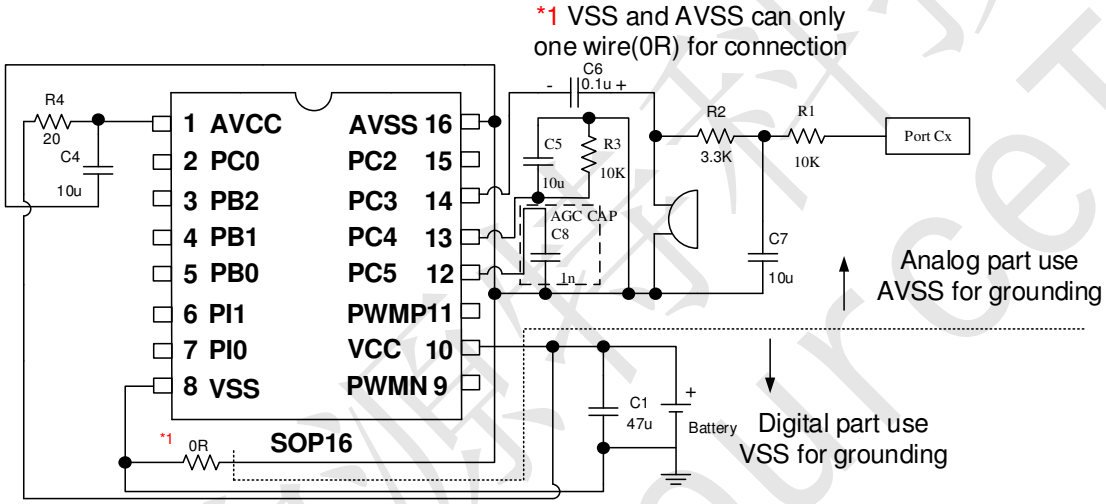

Fig 9.2.1 Microphone recorder application circuit (Standard version with 16bit ADC)

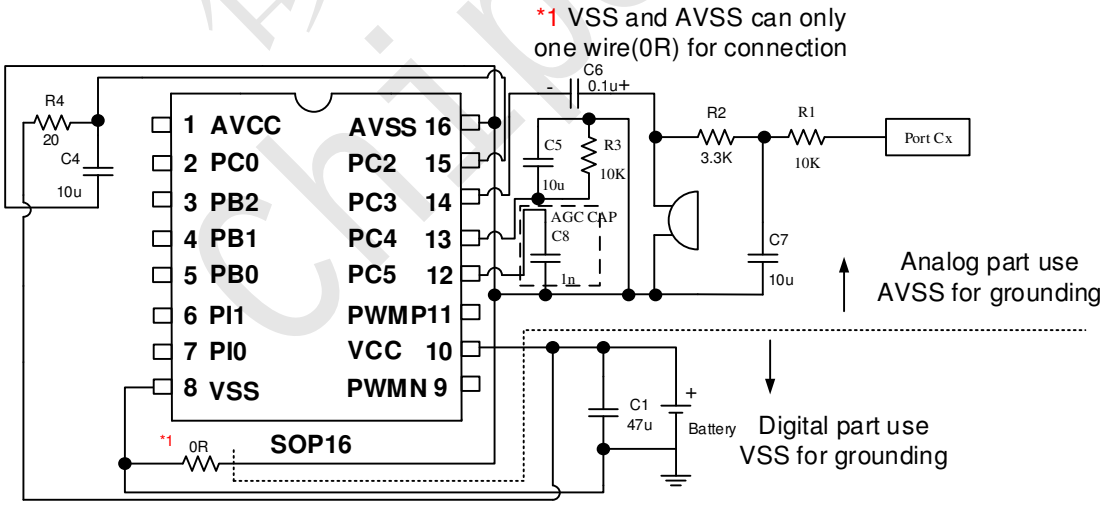

Fig 9.2.2 Microphone recorder application circuit (Standard version with 12bit ADC)

The optimum version (Fig 9.3) is used in the design. The voltage of PC4 must be checked for different microphone impedance, it must be below (1/2 VCC-0.1V) at highest operating voltage that can adjust by R2 (2.2K ~ 10K).

R-option (parallel with microphone) can help to adjust PC4 voltage below (1/2 VCC-0.1V), when R2 adjustment can't do it.

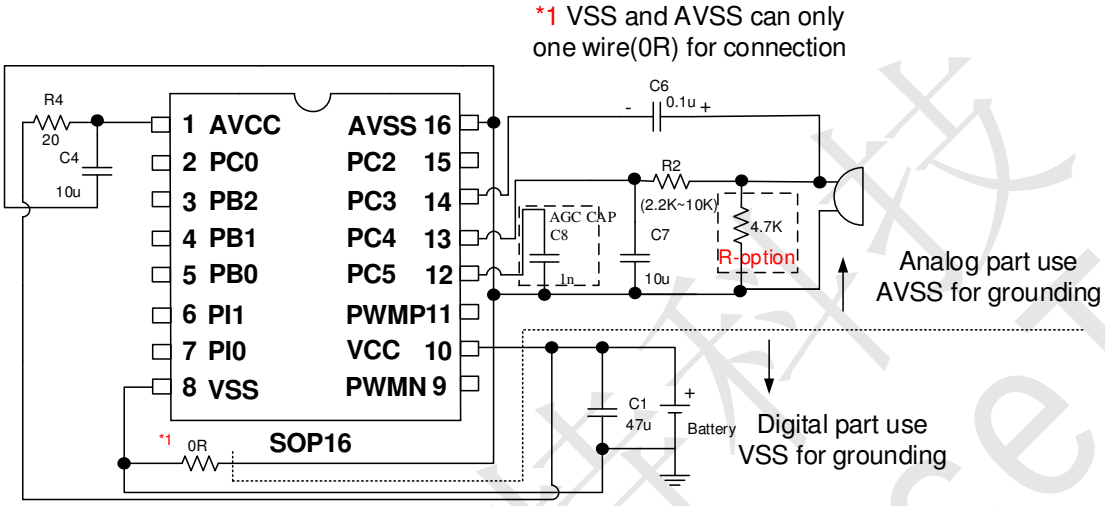

Fig 9.3.1 Microphone recorder application circuit (Optimum version with 16bit ADC)

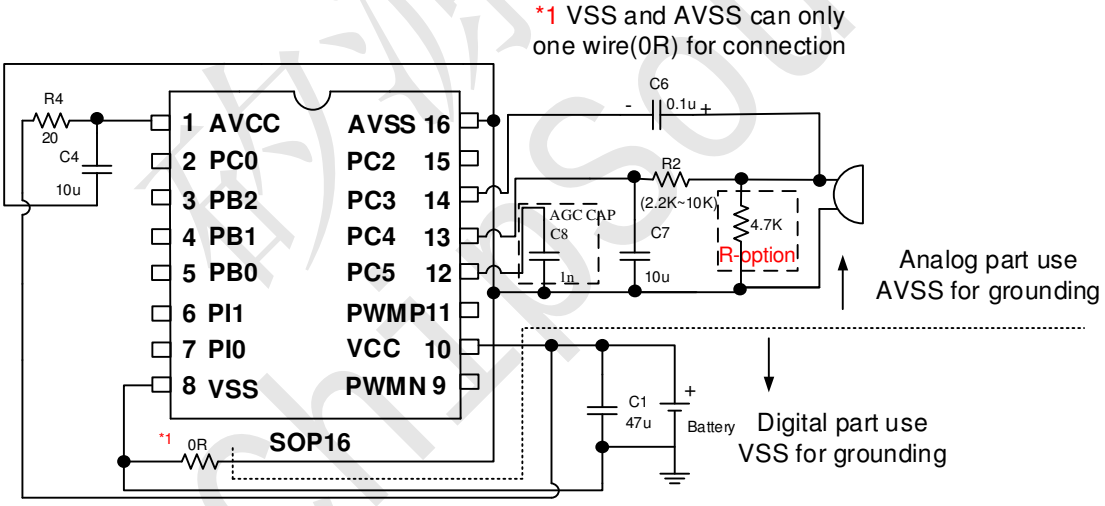

Fig 9.3.2 Microphone recorder application circuit (Optimum version with 12bit ADC)

10. TR16F096A(B) System Control

10.1 Halt Mode & Wake up

TR16F096A(B) is changed into HALT mode (system clock stop, RTC stop by Option setup) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The RTC timer, PA0~PA5, PB0~PB5 and PC0~PC7 are supporting the wake-up MCU function when related I/O port raising/falling edge which selects by program. The program counter will be 04H when HALT instruction executed immediately; in addition, when wake up condition is occurred, MCU will release HALT state and program counter go-to next address after difference stable clock is delayed by option. During the Halt mode period, the SRAM will keep their previous data without changing.

10.2 Watch Dog Timer Reset (WDT)

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
ClrWDT	1DH	XX	W									Clear WDT

The watch dog timer (WDT) is used to reset whole chip when detect unexpected execution sequence of instructions caused by accident condition, avoiding dead lock of MCU program. Software shall run an "clear watch dog timer"(CLRWDT) instruction before this timer time out. It will generate a reset signal to reset whole system when WDT overflow.

WDT will be reset when wake-up from halt or after power on or software clear. In test mode, watch dog timer will be disabled no matter watch-dog-timer is time-out or not.

The reset watch dog timer code syntax is strongly recommended as: "**CLRWDT = AR**".

10.3 Low Voltage Reset

When VCC power is applied to the chip, the low voltage reset is initially enabled by default, it will be disabled when in halt mode. The internal system reset will be generated if VCC power below the voltage of LVR(option setup). The normal operation of LVR is always enable expect disable in HALT mode.

10.4 Reset System

TR16F096A(B) reset is come from four signals which are power on reset, low voltage reset(LVR), external IO PB5 or PC7 pin (by option) and WDT overflow reset, as shown in Figure 10.1. A dedicated external resetb input pin (by option) is provided to reset this chip, which has 30K ohm pull up resistor. The operation frequency of MCU will go back to BANK0 mode when reset occurred.

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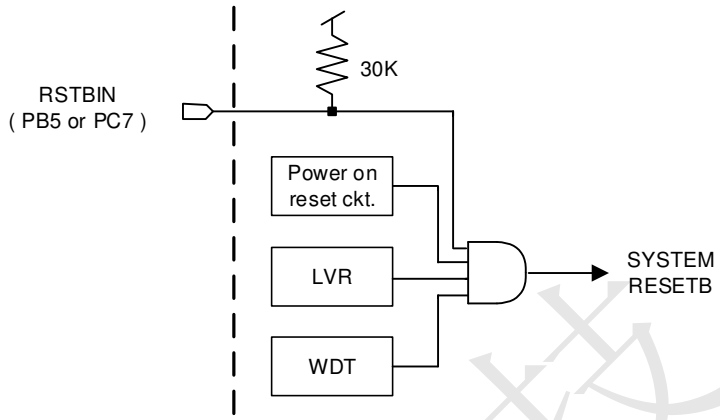

Figure 10.1 Reset system block diagram

10.5 Clock System Architecture

TR16F096A(B) clcok system supports internal ROSC(65.536MHz) for System Clock, and Low power RC oscillator(32768Hz -10%@1.8V ~ +10%@5.5V) for RTC function.

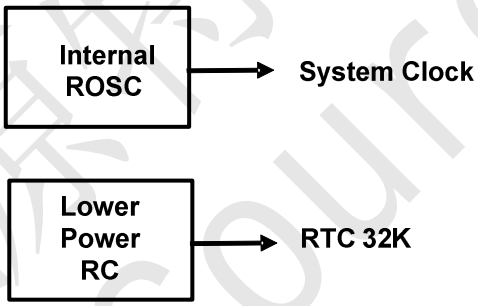

Figure 10.2 Clock System Diagram

11. TR16F096A(B) Electrical Characteristics

11.1 Absolute Maximum Rating

Parameters	Symbol	Value	Unit
DC Supply Voltage	VCC	<5.5	V
Input Voltage	Vin	-0.5 to VCC+0.5	V
Operating Temperature Range	Ta	-20 to 75	℃
Storage Temperature Range	Tstg	-50 to 150	℃

11.2 DC/AC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted

Parameters	Symbol	Minimum	Typical	Maximum	Test Condition
Operating voltage	VCC	1.8 V	-	5.5 V	
Operating frequency (BANK0)	BANK0	8.192MHz ±3%		16.384MHz ±3%	
Operating frequency (BANK15)	BANK15		32.768MHz ±3%		
RC oscillator frequency	Frc1		65.536MHz ±3%		
Low power RC oscillator frequency	Frc2	32768Hz -10%		32768Hz +10%	
Normal Sleep Halt Current	Ihalt1		5uA	9uA	All function off
Operating Current	Iop		5mA		no load
input high voltage (PortA, PortB, PortC)	VIH	0.6 VCC			Without schmitt trigger
input low voltage (PortA, PortB, PortC)	VIL			0.5 VCC	Without schmitt trigger
input high voltage (PortI)	VIH	0.7 VCC			With schmitt trigger
input low voltage (PortI)	VIL			0.3 VCC	With schmitt trigger
output high voltage	Voh	0.95 VCC			no load
output low voltage	Vol			0.05 V	no load
output high current	Ioh		16 mA		Vout=VCC-0.4V, PortA, B, C, I select strength driving option
output low current	Iol		-16 mA		Vout=0.4V PortA, B, C, I select strength driving option
pull-down resistance	Rpd		100K/200 /500K ohm		pins with pull-down, Port A,B,C, I
pull-up resistance	Rpu		200K ohm		pins with pull-up, Port A,B,C, I

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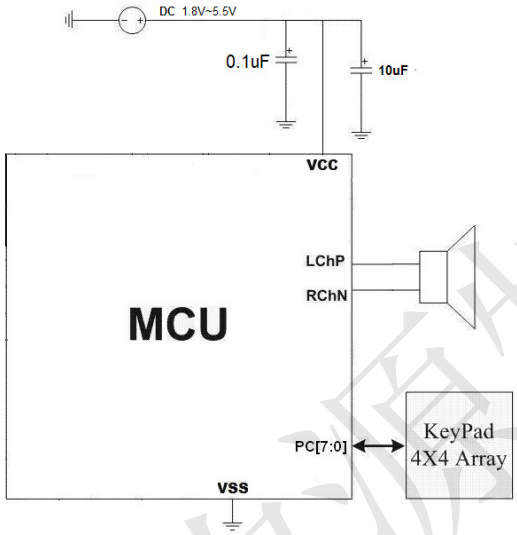
12. TR16F096A(B) Application Circuit

Application Circuit: Mono16-bit PWM output

Notice:

1. ***VCC Decoupling Cap 10uF should be close to IC within 0.5cm in PCB layout.***
2. ***VCC Decoupling Cap 0.1uF should be close to IC within 0.5cm in PCB layout.***
3. ***The width of VCC and VSS power line should be greater than 30 mil in PCB layout.***
4. ***VSS and AVSS are as close as possible.***



13. TR16F096A(B) Appendix:

Appendix 1: PORT A PIN MAP RELATE TO FUNCTION

	PORT A[5:0] (I/O Power : VIO)					
	5	4	3	2	1	0
8 CH ADC						
8 CH ADC2						
3 CH Comparator						
SPI (Master)			SO(0) <-	CS(0) ->	SI(0) ->	CLK(0) ->
SPI (Slaver)			SO(1) ->	CS(1) <-	SI(1) <-	CLK(1) <-
ICE						
Crystal						
I2C	SCL(1)	SDA(1)				
UART	TX(0)	RX(0)				
TRA1402						
IR 38K		IR_38KO(0)				
EXT-RESETB						
EXTINT0						
EXTINT1						
Microphone						
AUDIO PWM						
BUZZER						
PIR						
CDS						
OPA						
Debounce	Debounce(4)	Debounce(3)				
High-Current	High-Current					

Appendix 2: PORT B PIN MAP RELATE TO FUNCTION

	PORT B[7:0] (I/O Power : VCC)							
	7	6	5	4	3	2	1	0
8 CH ADC			ADC Ch7	ADC Ch6	ADC Ch5	ADC Ch4	ADC Ch3	ADC Ch2
8 CH ADC2		SDAVMID	ADC Ch7	ADC Ch6	ADC Ch5	ADC Ch4	ADC Ch3	ADC Ch2
3 CH Comparator			CAP3+	CAP3-			CAP1+	CAP1-
SPI (Master)					SO(1) <-	CS(1) ->	SI(1) ->	CLK(1) ->
SPI (Slaver)					SO(0) ->	CS(0) <-	SI(0) <-	CLK(0) <-
ICE								
Crystal								
I2C					SCL(0)	SDA(0)		
UART			TX(1)	RX(1)				
TRA1402						SYNC	DIO	SCLK
IR 38K				IR_38KO(1)				
EXT-RESETB			EXT-RSTB(0)					
EXTINT0					Trigger(0)			
EXTINT1							Trigger(1)	
Microphone								
AUDIO PWM			PWM_B5 (TYPE 1)	PWM_B4 (TYPE 1)				
BUZZER								BUZZER(0)
PIR				VINN2	OPOUT2	VINP1	VINN1	OPOUT1
CDS			CAP3+					
OPA			VINP2	VINN2	OPOUT2	VINP1	VINN1	OPOUT1
Debounce								
High-Current								

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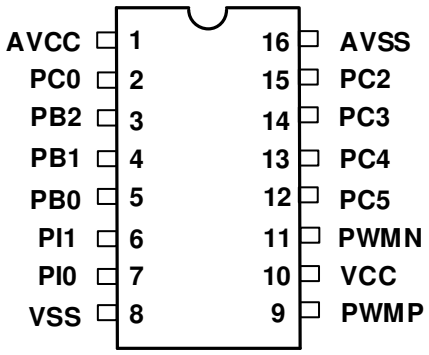
Appendix 3: PORT C PIN MAP RELATE TO FUNCTION

	PORT C[7:0] (I/O Power : VCC)							
	7	6	5	4	3	2	1	0
8 CH ADC						VREFI	ADC Ch1	ADC Ch0
8 CH ADC2							ADC Ch1	ADC Ch0
3 CH Comparator							CAP2+	CAP2-
SPI (Master)								
SPI (Slaver)								
ICE								
Crystal	X32KI	X32KO						
I2C								
UART								
TRA1402								
IR 38K								
EXT-RESETB	EXT-RSTB(1)							
EXTINT0								Trigger(1)
EXTINT1					Trigger(0)			
Microphone			AGC	VMID	MIC			
AUDIO PWM			PWM_C5 (TYPE 2)	PWM_C4 (TYPE 2)				
BUZZER							BUZZER(1)	
PIR								
CDS								
OPA								
Debounce							Debounce(2)	Debounce(1)
High-Current								

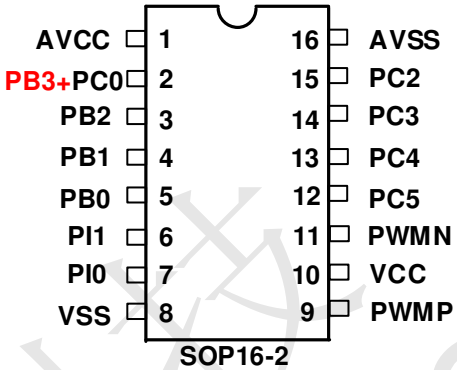
Appendix 4: PORT I PIN MAP RELATE TO FUNCTION

	PORT I[1:0] (I/O Power : VCC)	
	1	0
8 CH ADC		
8 CH ADC2		
3 CH Comparator		
SPI (Master)		
SPI (Slaver)		
ICE	ICE_SCLK(I)	ICE_SD(I/O)
Crystal		
I2C		
UART		
TRA1402		
IR 38K		
EXT-RESETB		
EXT-INT		
Microphone		
AUDIO PWM		
BUZZER		
PIR		
CDS		
OPA		
Debounce		
High-Current		

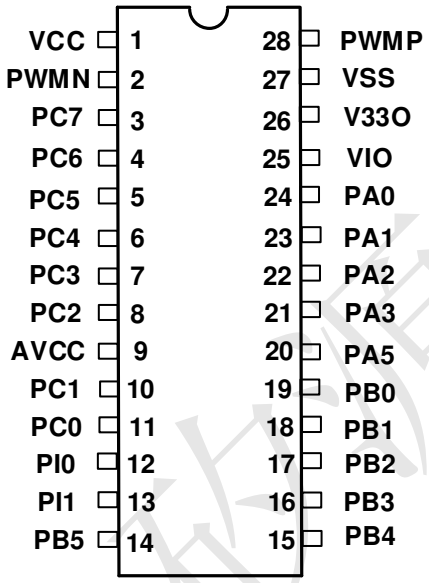
14. TR16F096A(B) Package: SOP16 / SOP16-2 / SSOP24 / SSOP28



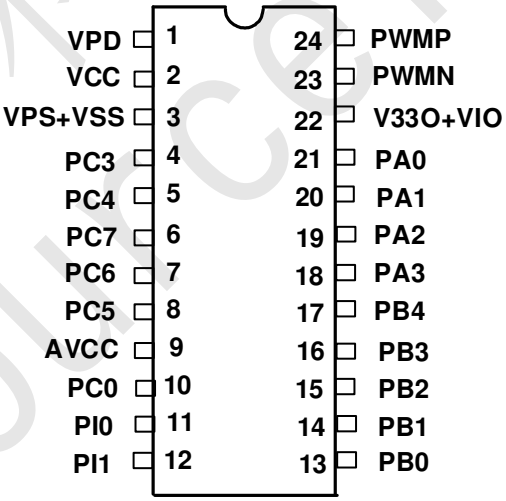
SOP16
(TR16F096A)



SOP16-2
(TR16F096B)



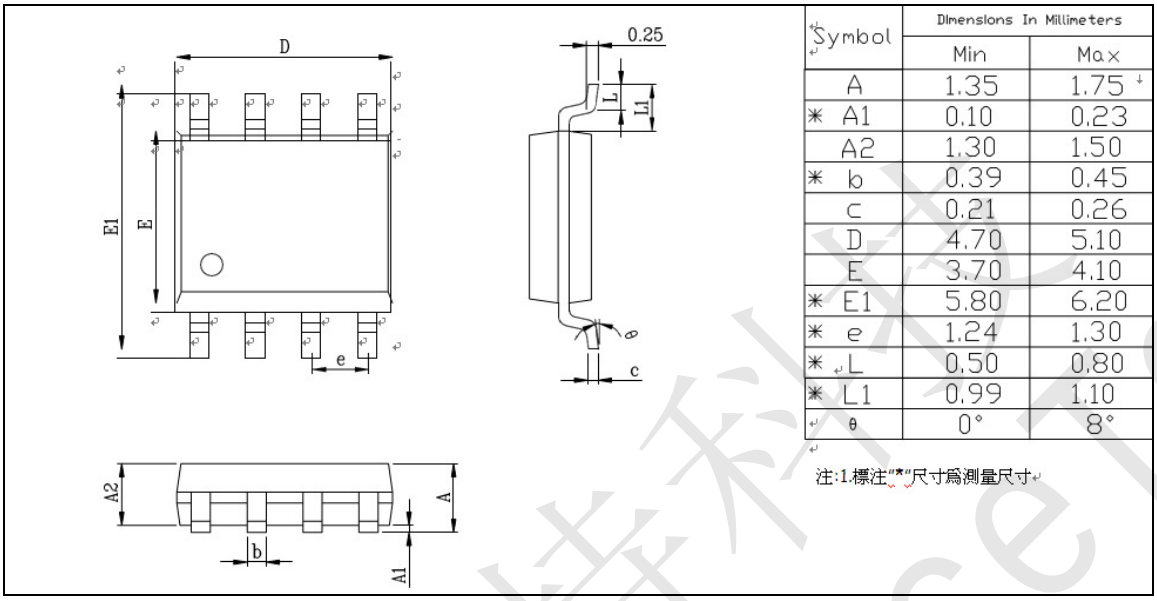
SSOP28 (TR16F096A)



SSOP24
(TR16F096A)

TR16F096A(B) PACKAGE INFORMATION

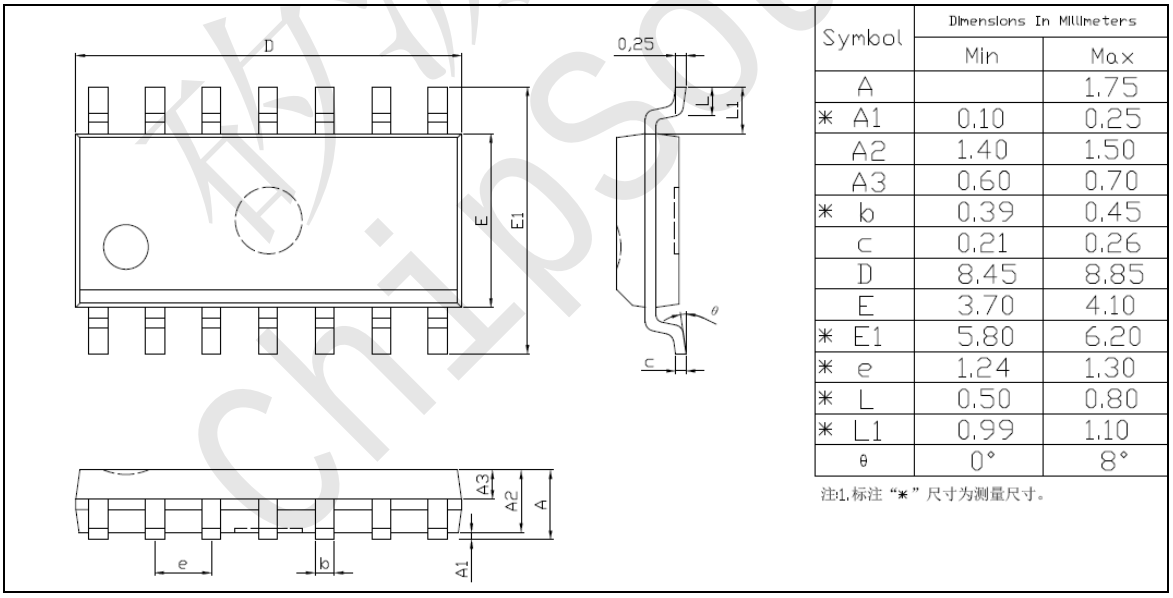
SOP08



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
* A1	0.10	0.23
A2	1.30	1.50
* b	0.39	0.45
c	0.21	0.26
D	4.70	5.10
E	3.70	4.10
* E1	5.80	6.20
* e	1.24	1.30
* L	0.50	0.80
* L1	0.99	1.10
θ	0°	8°

注:1.標注"*"尺寸爲測量尺寸。

SOP14



Symbol	Dimensions In Millimeters	
	Min	Max
A		1.75
* A1	0.10	0.25
A2	1.40	1.50
A3	0.60	0.70
* b	0.39	0.45
c	0.21	0.26
D	8.45	8.85
E	3.70	4.10
* E1	5.80	6.20
* e	1.24	1.30
* L	0.50	0.80
* L1	0.99	1.10
θ	0°	8°

注1,标注“*”尺寸为测量尺寸。

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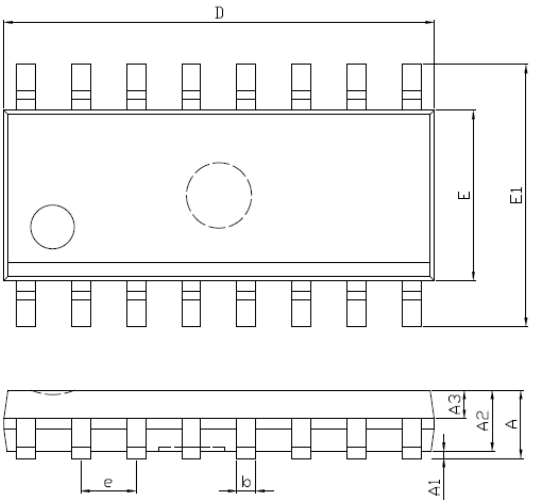
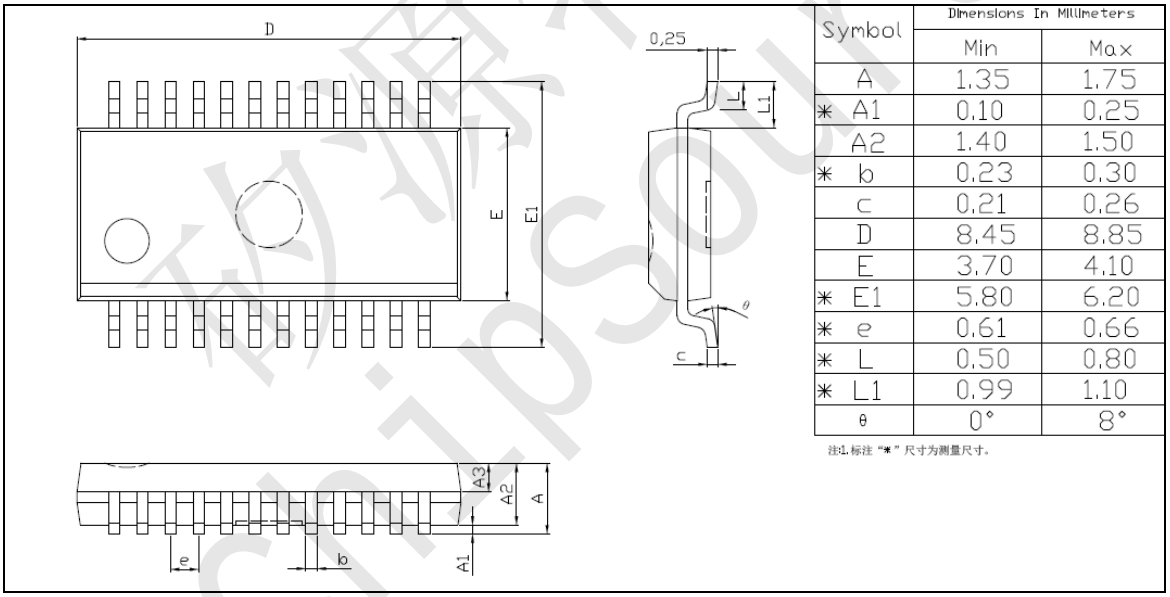
SOP16



Symbol	Dimensions In Millimeters	
	Min	Max
A		1.75
* A1	0.10	0.25
A2	1.40	1.50
A3	0.61	0.71
* b	0.39	0.45
c	0.21	0.26
D	9.70	10.10
E	3.70	4.10
* E1	5.80	6.20
* e	1.24	1.30
* L	0.60	0.80
* L1	0.99	1.10
θ	0°	8°

注1.标注“*”尺寸为测量尺寸。

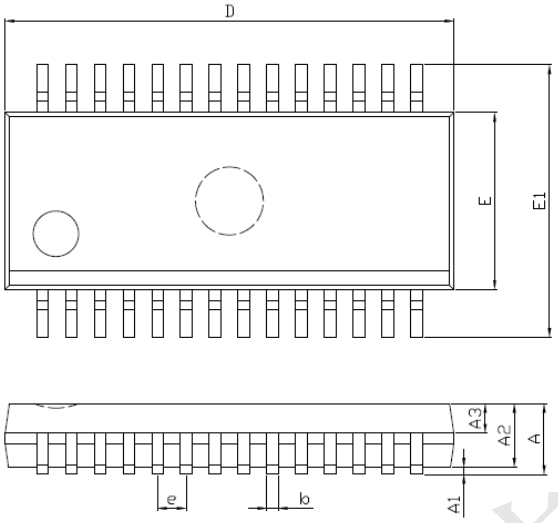
SSOP24



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
* A1	0.10	0.25
A2	1.40	1.50
* b	0.23	0.30
c	0.21	0.26
D	8.45	8.85
E	3.70	4.10
* E1	5.80	6.20
* e	0.61	0.66
* L	0.50	0.80
* L1	0.99	1.10
θ	0°	8°

注1.标注“*”尺寸为测量尺寸。

SSOP28



Symbol	Dimensions In Millmeters	
	Min	Max
A		1.75
* A1	0.08	0.225
A2	1.35	1.50
A3	0.60	0.70
* b	0.23	0.31
c	0.20	0.24
D	9.80	10.00
E	3.80	4.00
* E1	5.80	6.20
* e	0.58	0.69
* L	0.50	0.80
* L1	0.99	1.10
θ	0°	8°

注1.标注“*”尺寸为测量尺寸。
2. e=0.635mm

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15. TR16F096A(B) SPI Operation Sequence

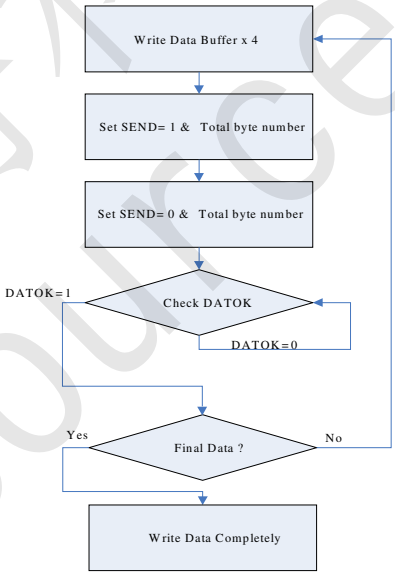
A1.0 Initial Process

```
set io[IOC_PA].b2          // set output port
set io[STATUS].b8          // Enable SPI Control
set io[PortA].b2           // CS=1
set io[SPI_CTRL].b11       // set ICS = 1
```

A1.1 Sending Data Process

```
clr io[PortA].b2                // CS =0
clr io[SPI_CTRL].b11            // ICS=0
// page write 256 bytes
cx = 0x1f;
i0      = Data_Buf.n0
i0.h    = Data_Buf.n1
SPI_write_data_loop:
io[SPI_DATA] = rm[i0++];
io[SPI_DATA] = rm[i0++];
io[SPI_DATA] = rm[i0++];
io[SPI_DATA] = rm[i0++];
push ar;
// set total byte number & send data
ar = 0x18;
ah = 0x00;                      // speed
io[SPI_CTRL] = ar;              //set SEND = 1;
clr io[SPI_CTRL].b4             // set SEND = 0;
call   Check_Tran_OK
loop   SPI_write_data_loop
set io[PortA].b2                // CS =1
set io[SPI_CTRL].b11            // ICS=1

Check_Tran_OK:
test io[SPI_CTRL].b7
if eq jmp Check_Tran_OK
Check_Tran_OK_End:
rets
```

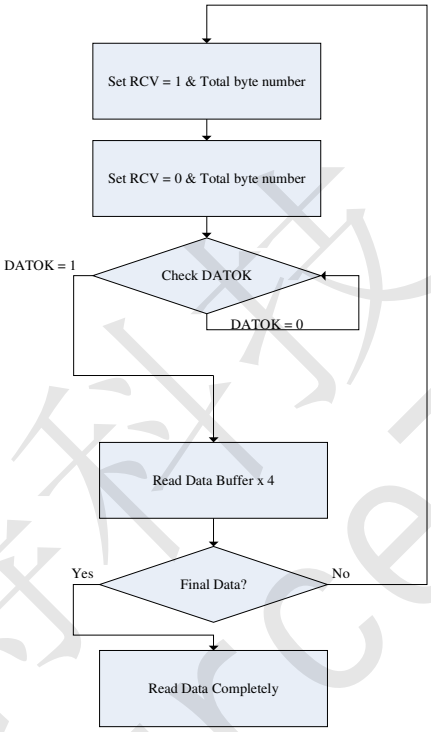


A1.2 Receiving Data Process

```
            clr io[PortA].b2                // CS =0
             clr io[SPI_CTRL].b11           // ICS=0


             i0      = Data_Buf.n0
             i0.h    = Data_Buf.n1
            // receive data(256 bytes)
            cx = 0x1f;
SPI_read_data_loop:
             ar = 0x28;
             ah = 0x00;                     // speed
             io[SPI_CTRL] = ar;             // Set RCV = 1;
             clr io[SPI_CTRL].b5            // Set RCV = 0;
            call    Check_Tran_OK
            rm[i0++] = io[SPI_DATA];
             rm[i0++] = io[SPI_DATA];
             rm[i0++] = io[SPI_DATA];
             rm[i0++] = io[SPI_DATA];
            loop    SPI_read_data_loop
             set io[PortA].b2               // CS =1
             set io[SPI_CTRL].b11           // ICS=1


Check_Tran_OK:
             test io[SPI_CTRL].b7
            if eq jmp Check_Tran_OK
Check_Tran_OK_End:
            rets
```



16. TR16F096A(B) Revision history

REVISION	DESCRIPTION	PAGE	DATE
V1.0	New establish		2022/1/27
V1.1	Add TR16F096B(only one package : SOP16-2)	68	2022/5/11
	the capacitance value of C6 is changed to 0.1uF in Fig9.2 and Fig9.3	60	
V1.2	TR16F096A(B) do not support ultra-deep sleep	3	2022/11/8
	PortC0 are forbidden to be connected with pull-up resistance	3, 6	
	Low power RC modify to 32768Hz +/- 10%	27, 63, 64	
	Modify two OPAs mode	47	
	Modify SOP16, SOP16-2 package, change PWMP to pin 9, change PWMN to pin 11	68	
V1.3	Remove Buzzer and speaker wake up. (MISC2 bit5, MISC2 bit 6 and MISC3 bit3 should be set to 0.)	10, 11, 12	2022/12/28
V1.4	Add TR16F096A comment to package chapter	67	2023/1/16
V1.5	Add SSOP24 to package chapter	67	2023/3/2
V1.6	PortC0 are forbidden to be connected with VCC or pull-up resistance.	3, 6	2023/4/17
	Address 1DH: RealT register	10, 12	
	Add the description of these signals of CLR_TX_INT, CLR_INT and CLR_RxOverrunErr	37	
	If Microphone is used, OPA1 and OPA2 need to be disable.	3, 60	
	Add microphone channel 8 of 12-bit SAR ADC	35, 60, 61	

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