WESTERN DIGITAL

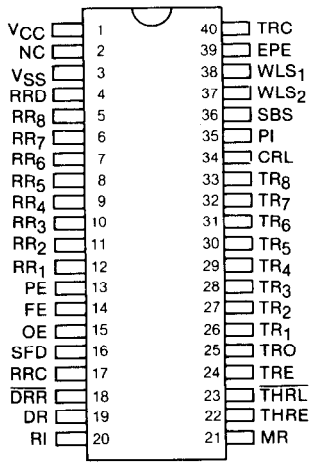
CORPORATION

TR1863/TR1865

Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

- SINGLE POWER SUPPLY — +5VDC
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS



PIN DESIGNATION

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES

DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UART) is a general purpose, programmable or hardwired MOS/LSI device. The UART is used to convert parallel data to a serial data format on the transmit side, and converts a serial data format to parallel data on the receive side.

The serial format in order of transmission and reception is a start bit, followed by five to eight data bits, a parity bit (if selected) and one, one and one-half, or two stop bits.

Three types of error conditions are available on each received character: parity error, framing error (no valid stop bit) and overrun error.

The transmitter and receiver operate on external 16X clocks, where 16 clock times are equal to one bit time. The receiver clock is also used to sample in the center of the serial data bits to allow for line distortion.

Both transmitter and receiver are double buffered allowing a one character time maximum between a data read or write. Independent handshake lines for receiver and transmitter are also included. All inputs and outputs are TTL compatible with three-state outputs available on the receiver, and error flags for bussing multiple devices.

PIN DESCRIPTION

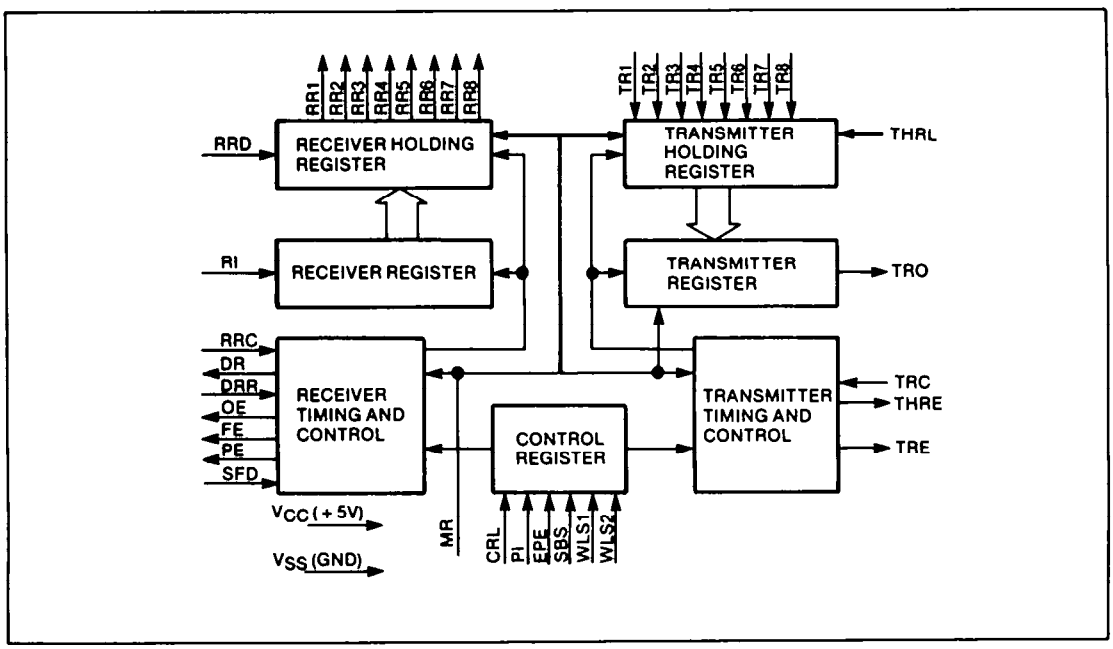
PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
1	V_{CC}	POWER SUPPLY	+5 volts supply
2	NC	NC	No Internal Connection
3	V_{SS}	GROUND	Ground = 0V
4	RRD	RECEIVER REGISTER DISCONNECT	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RR_8-RR_1	RECEIVER HOLDING REGISTER DATA	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PE	PARITY ERROR	A high level output voltage, V_{OH}, on this line indicates that the received parity differ from that which is programmed by the EVEN PARITY ENABLE (pin 39) and the PARITY INHIBIT (pin 35) control lines. This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FE	FRAMING ERROR	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	OE	OVERRUN ERROR	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	SFD	STATUS FLAGS DISCONNECT	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	RRC	RECEIVER REGISTER CLOCK	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	$\overline{DRR}$	$\overline{\text{DATA RECEIVED RESET}}$	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DR	DATA RECEIVED	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.

PIN DESCRIPTION

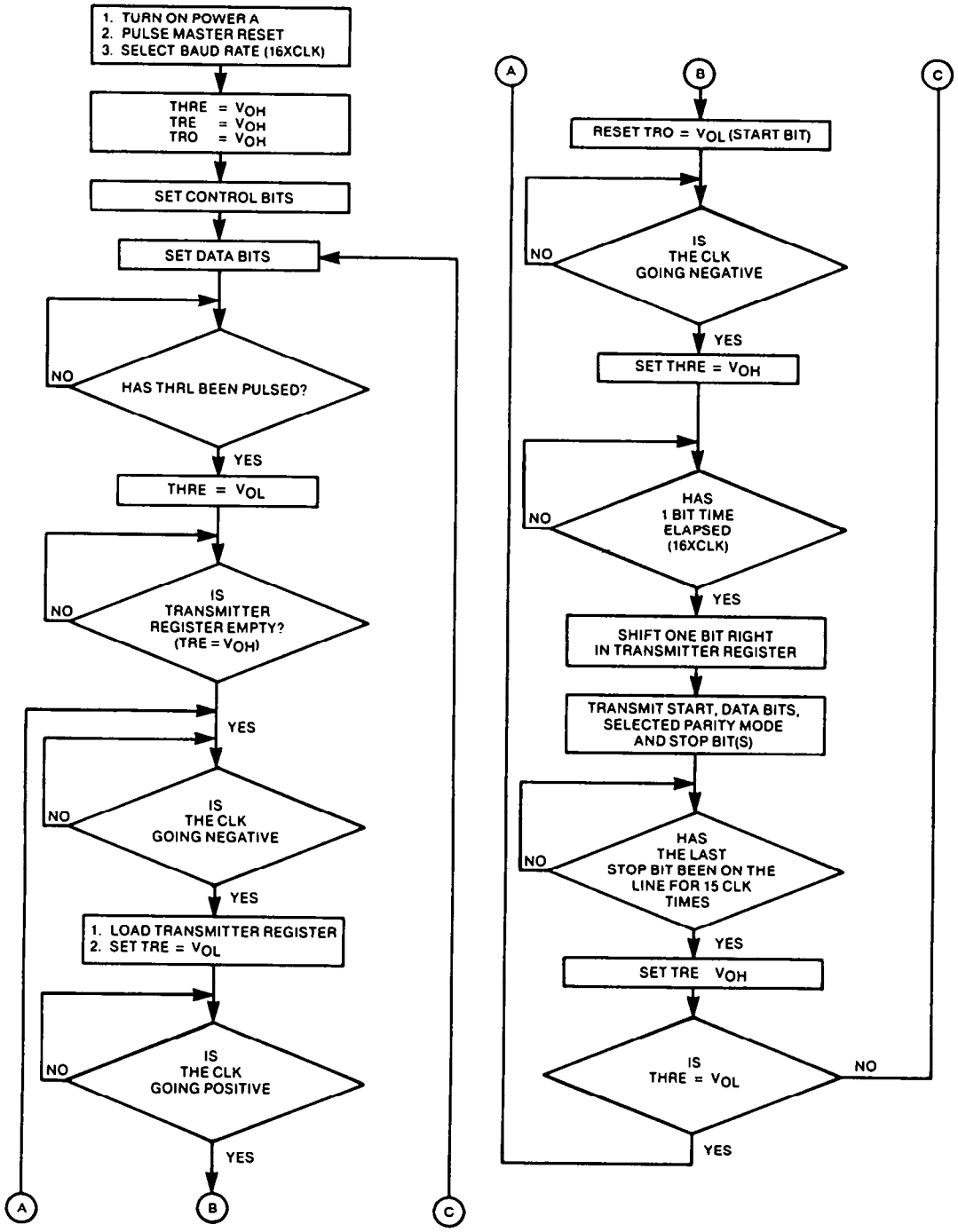
PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
20	RI	RECEIVER INPUT	Serial input data. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MR	MASTER RESET	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the TRANSMITTER and RECEIVER HOLDING REGISTERS, the TRANSMITTER REGISTER, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	THRE	TRANSMITTER HOLDING REGISTER EMPTY	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	$\overline{\text{THRL}}$	$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRE	TRANSMITTER REGISTER EMPTY	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRO	TRANSMITTER REGISTER OUTPUT	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage V_{OH}, to a low-level output voltage V_{OL}.
26-33	TR_1-TR_8	TRANSMITTER REGISTER DATA INPUTS	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, TR_1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CRL	CONTROL REGISTER LOAD	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.

PIN DESCRIPTION

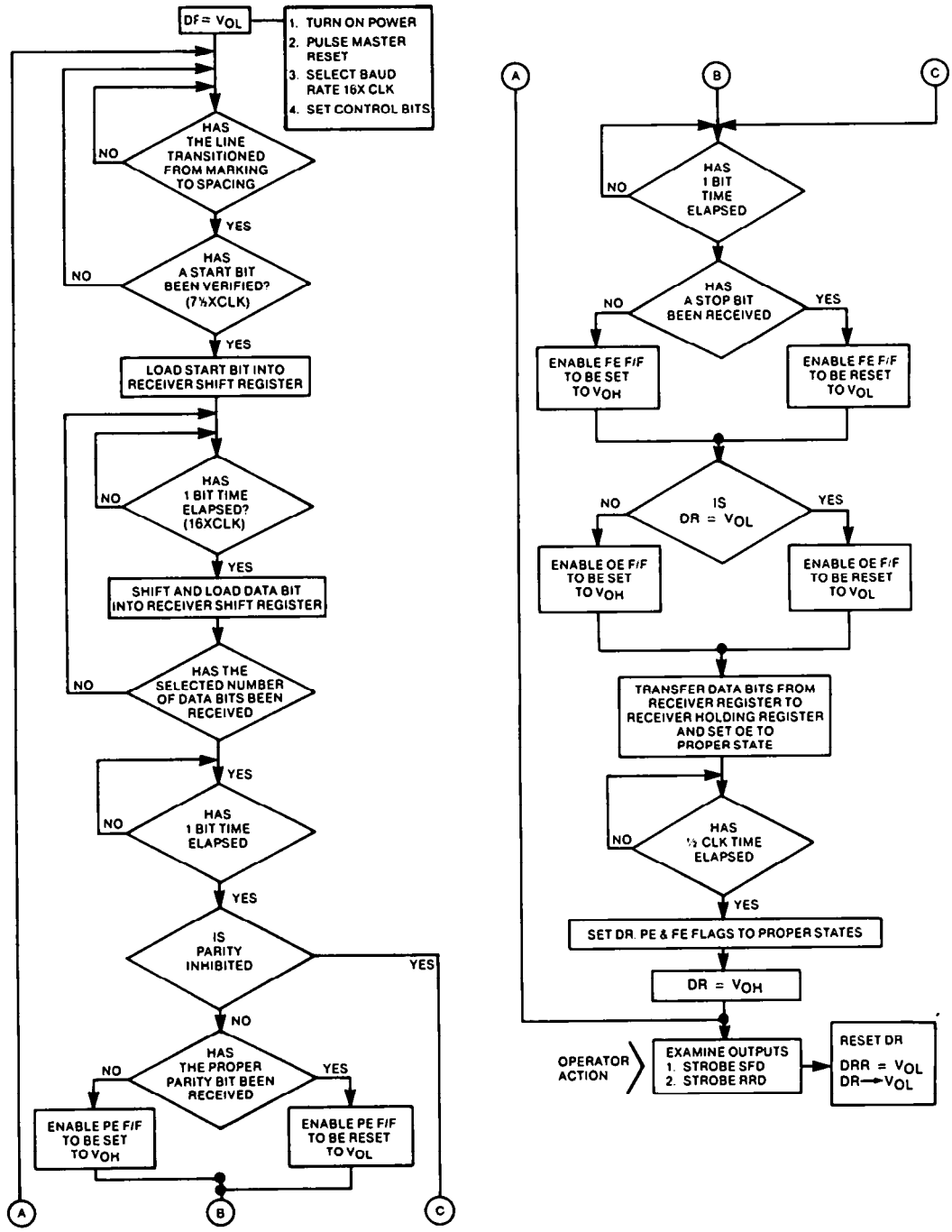
PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
35	PI	PARITY INHIBIT	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	SBS	STOP BIT(S) SELECT	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1863 and TR1865 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WLS_2-WLS_1	WORD LENGTH SELECT	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EPE	EVEN PARITY ENABLE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRC	TRANSMITTER REGISTER	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.



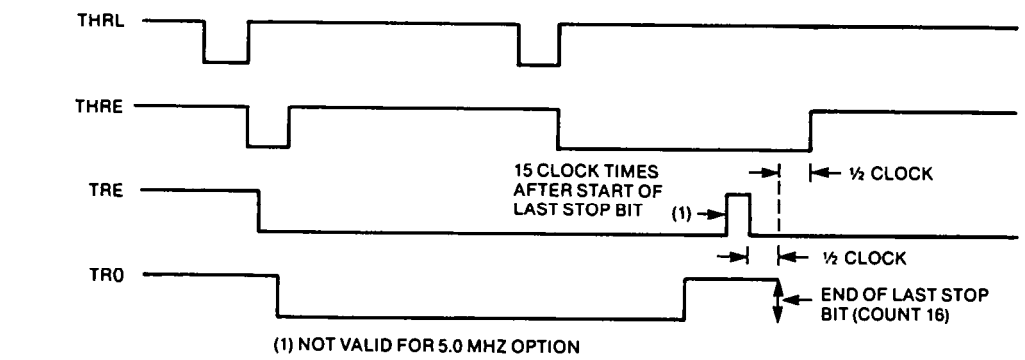
TR1863/TR1865 BLOCK DIAGRAM

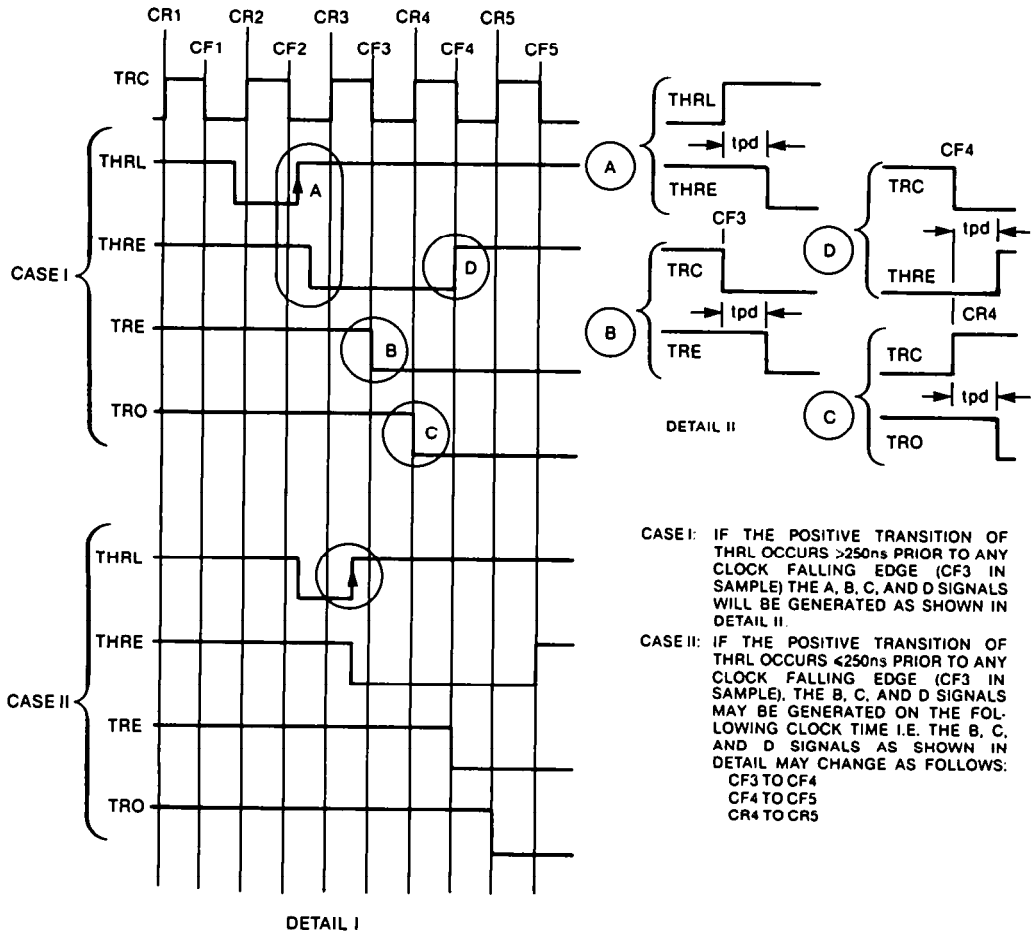


TRANSMITTER FLOW CHART



RECEIVER FLOW CHART

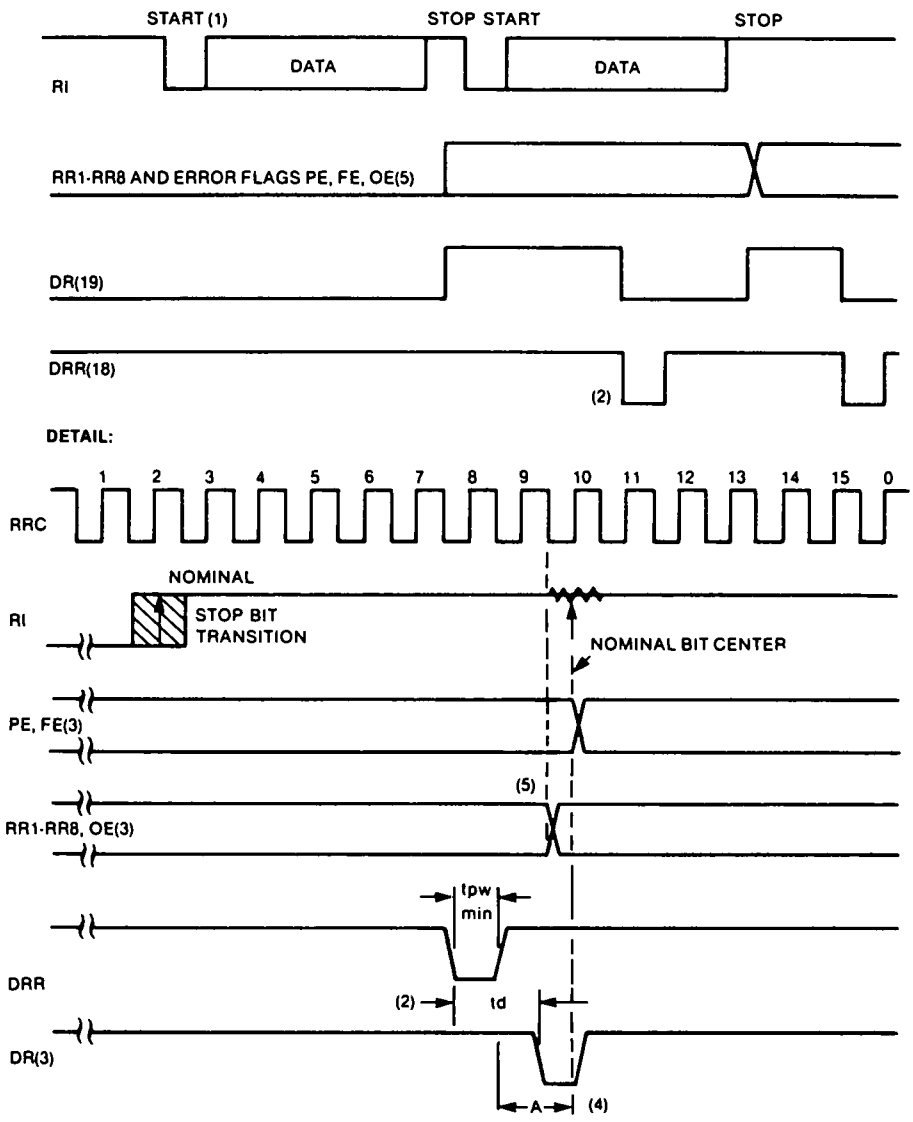




TRANSMITTER TIMING

CASE I: IF THE POSITIVE TRANSITION OF THRL OCCURS >250ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE) THE A, B, C, AND D SIGNALS WILL BE GENERATED AS SHOWN IN DETAIL II.

CASE II: IF THE POSITIVE TRANSITION OF THRL OCCURS <250ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE), THE B, C, AND D SIGNALS MAY BE GENERATED ON THE FOLLOWING CLOCK TIME I.E. THE B, C, AND D SIGNALS AS SHOWN IN DETAIL MAY CHANGE AS FOLLOWS:
- CF3 TO CF4
- CF4 TO CF5
- CR4 TO CR5



(1) SEE APPLICATION FLAGS REPORT NO. 1 FOR DESCRIPTION OF START BIT DETECTION
(2) THE DELAY BETWEEN DRR AND DR = td = 500 NS
(3) DR. ERROR FLAGS, AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS tpd) PRIOR TO THE RISING EDGE OF DR
(5) DATA AND OE PRECEDES DR, PE, AND FE FLAGS BY ½ CLOCK
(6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.

FIGURE 1. RECEIVER TIMING

ABSOLUTE MAXIMUM RATINGS

NOTE: These voltages are measured with respect to GND

Storage Temperature
- Plastic ..... −55°C to +125°C
- Ceramic ..... −65°C to +150°C

V_{CC} Supply Voltage ..... −0.3V to +7.0V
Input Voltage at any pin ..... −0.3V to +7.0V
Operating Free-Air Temperature
- T_A Range ..... 0°C to 70°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 5%, V_{SS} = 0V)

SYMBOL	PARAMETER	TR1863/5		
	OPERATING CURRENT	MIN	MAX	CONDITIONS
I_{CC}	Supply Current		35ma	V_{CC} = 5.25V
	LOGIC LEVELS			
V_{IH}	Logic High	2.4V		
V_{IL}	Logic Low		0.6V	V_{CC} = 4.75V
	OUTPUT LOGIC LEVELS			
V_{OH}	Logic High	2.4V		V_{CC} = 4.75V, I_{OH} = 100μa
V_{OL}	Logic Low		0.4V	V_{CC} = 5.25V, I_{OL} = 1.6 ma
I_{OC}	Output Leakage (High Impedance State)		± 10μa	V_{OUT} = 0V, V_{OUT} = 5V SFD = RRD = V_1H
I_{IL}	Low Level Input Current	100μa	1.6ma	V_{IN} = 0.4V TR 1865 only
			10μa	V_{IN} = V_{IL}, TR 1863 only
I_{IH}	High Level Input Current		− 10μa	V_{IN} = V_{IH}, TR 1863 only

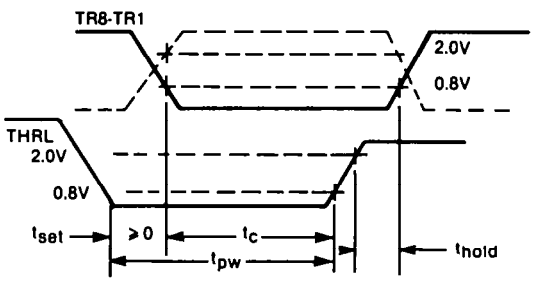


FIGURE 2. DATA INPUT LOAD CYCLE

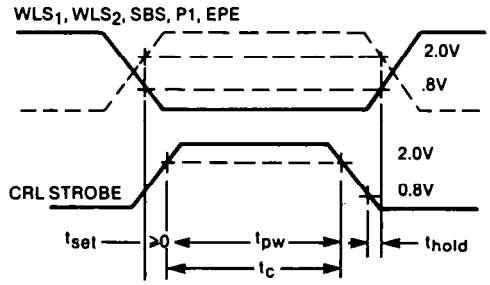
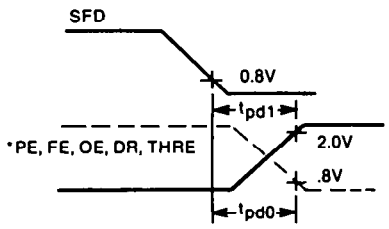
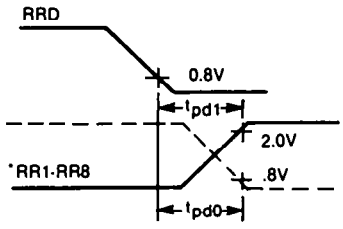


FIGURE 3. CONTROL REGISTER LOAD CYCLE



*OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM 0.8V TO 2.0V.

FIGURE 4. STATUS FLAG OUTPUT DELAYS



*RR_1-RR_3 ARE DISCONNECTED AT TRANSITION OF RRD FROM 0.8V TO 2.0V.

FIGURE 5. DATA OUTPUT DELAYS

SWITCHING CHARACTERISTICS

(See FIGURE 1-5)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
f_{clk}	Clock Frequency			V_{CC} = 4.75V
	TR1863-00	DC	1.0 MHz	
	TR1863-02	DC	2.5 MHz	
	TR1863-04	DC	3.5 MHz	
	TR1865-00	DC	1.0 MHz	with internal pull-ups on all inputs
	TR1865-02	DC	2.5 MHz	with internal pull-ups on all inputs
	TR1865-04	DC	3.5 MHz	with internal pull-ups on all inputs
t_{pw}	Pulse Widths			
	CRL (Fig. 3)	200 ns		
	THRL (Fig. 2)	200 ns		
	DRR (Fig. 1)	200 ns		
	MR	500 ns		
t_c	Coincidence Time	200 ns		
t_{hold}	Hold Time (Fig. 2, 3)	20 ns		
t_{set}	Set Time (Fig. 2, 3)	0		
	OUTPUT PROPAGATION DELAYS			
t_{pd0}	To Low State (Fig. 4, 5)		250 ns	
t_{pd1}	To High State (Fig. 4, 5)		250 ns	C_L = 20 pf, plus one TTL load
	CAPACITANCE			
c_{in}	Inputs		20 pf	f = 1 MHz, V_{IN} = 5V
c_o	Outputs		20 pf	f = 1 MHz, V_{IN} = 5V

See page 383 for ordering information.