

# TR3001

## PLL IC

# Data Sheet

tenx reserves the right to change or discontinue the manual and online documentation to this product herein to improve reliability, function or design without further notice. tenx does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. tenx products are not designed, intended, or authorized for use in life support appliances, devices, or systems. If Buyer purchases or uses tenx products for any such unintended or unauthorized application, Buyer shall indemnify and hold tenx and its officers, employees, subsidiaries, affiliates and distributors harmless against all claims, cost, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use even if such claim alleges that tenx was negligent regarding the design or manufacture of the part.

**AMENDMENT HISTORY**

<b>Version</b>	<b>Date</b>	<b>Description</b>
V1.0	Feb, 2005	New release.
V1.1	Dec, 2011	Add Ordering Information table

# CONTENTS

AMENDMENT HISTORY.....2

DESCRIPTION .....1

FEATURES .....1

BLOCK DIAGRM .....1

ABSOLUTE MAXIMUM RATINGS(Ta=25 °C).....1

ELECTRICAL CHARACTERISTICS(Ta=-10~80 °C,VDD=2.4~3.6V)....2

PIN DIAGRAM.....2

PIN DESCRIPTION .....3

FUNCTION DESCRIPTION.....4

    Serial I/O ports .....4

    Serial transfer format .....4

    Serial data transfer .....4

    Programmable counter .....4

    Setting programmable counter.....4

    SYSTEM APPLICATION BLOCK.....5

ORDERING INFORMATION .....6

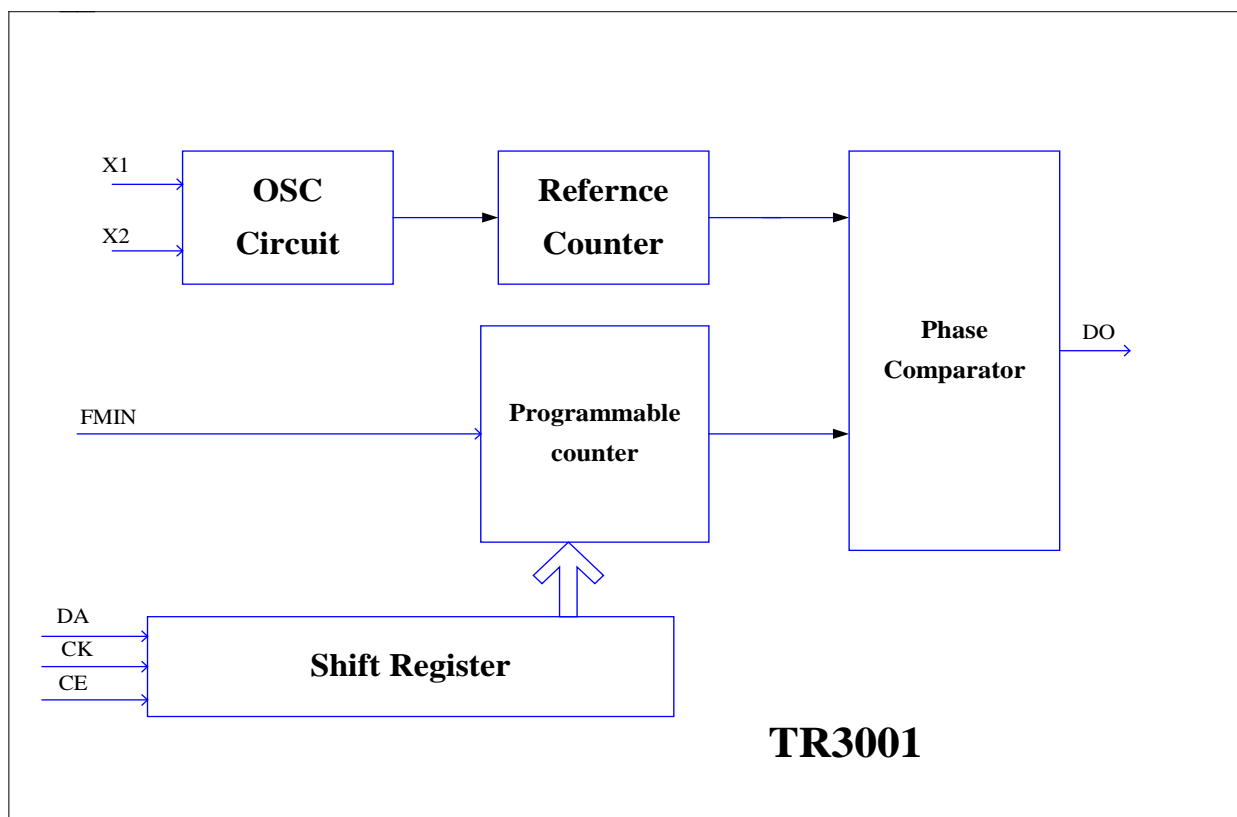
**DESCRIPTION**

The TR3001 is phase-locked loop (PLL) LSIs for FM stereo transmission application. All functions are controlled through 3 serial bus lines.

**FEATURES**

- Operate at input frequency ranging from 30~150 MHz during FMIN input .
- All functions controlled through 3 serial bus lines.
- CMOS structure with operating power supply rang of VDD=2.4~3.6V.

**BLOCK DIAGRM**



**ABSOLUTE MAXIMUM RATINGS(Ta=25°C)**

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD	-0.3~6.0	V
Input Voltage	VIN	-0.3~VDD+0.3	V
Power Dissipation	PD	300	MW
Operating Temperature	TOPR	-10~80	°C

**ELECTRICAL CHARACTERISTICS(Ta=-10~80°C,VDD=2.4~3.6V.)**

Characteristic	Symbol	Test Condition/Pin	Min	Typ.	Max	Unit
Operating Power Supply Voltage	VDD	PLL operation (normal operating)	2.4	3	3.6	V
Operating Power Supply Current	IDD	VDD=3.0V, XT=4MHz, FMIN=100MHz	--	2	4	mA

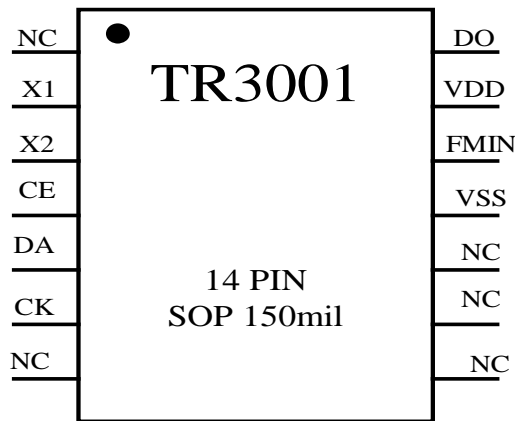
**Operating frequency range**

Crystal Oscillation Frequency		Connect crystal resonator to X1-X2 terminal		4		MHz
FMIN		VIN=0.2Vp-p	30	~	150	MHz

**Operating input amplitude range**

FMIN		30~150MHz	0.2	~	VDD-0.5	Vp-p
------	--	-----------	-----	---	---------	------

**PIN DIAGRAM**



**PIN DESCRIPTION**

Pin No.	Symbol	Pin name	Description
2	X1	Crystal oscillator pins	These pins set the reference frequency of the reference counter.
3	X2		
4	CE	Shift register enable	These pins set the frequency of PLL.
5	DA	Shift register data input	
6	CK	Shift register clock input	
12	FMIN	FM frequency input	These pins input FM band local oscillator signals by capacitor coupling. FMIN operate at low amplitude.
14	DO	Phase comparator Output	These pins are for phase comparator tri-state output.
11	VSS	Power supply pins	Applies 3.0V±10%
13	VDD		
1,7,8,9,10	NC		No connected

## FUNCTION DESCRIPTION

### Serial I/O ports

The block diagram shows that the functions are controlled by setting data in the 16 bits registers. Each bit of data in these registers is transferred through the serial ports between the controller and the DA, CK and CE pins.

### Serial transfer format

The serial transfer format consists of 16 data bits (Fig. 1).

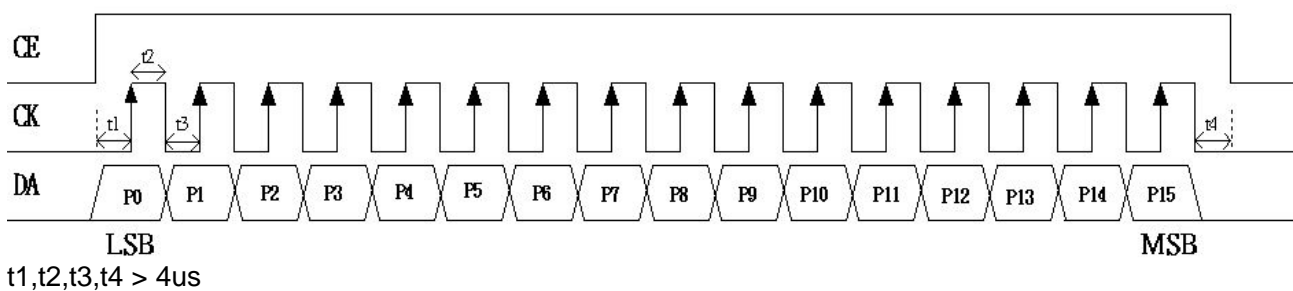


Fig.1

### Serial data transfer

Serial data are transferred in sync with the clock signal. Data transfer ceases when the CE signal is set to “L” level. Since the receiving side receives the serial data as valid data when the clock signal rises, it is effective for the sending side to produce output in sync with the clock signal fall.

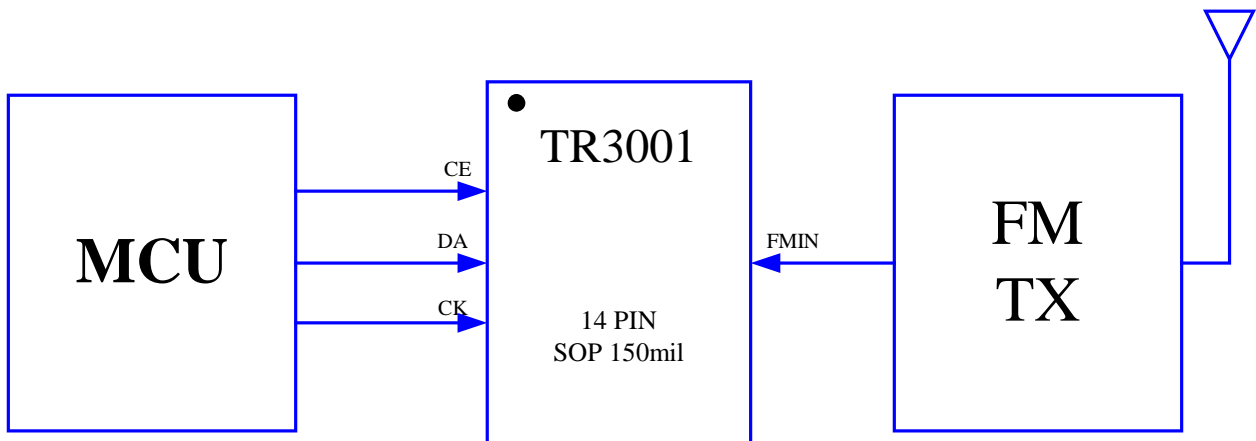
### Programmable counter

The programmable counter section consists of 16bit programmable binary counter.

### Setting programmable counter

The divisor for the programmable counter is set as binary data in bits P0~P15.(fig.1)  
Divisor setting range  $n=640H\sim FF00H$  (1600~65280)

SYSTEM APPLICATION BLOCK





ORDERING INFORMATION

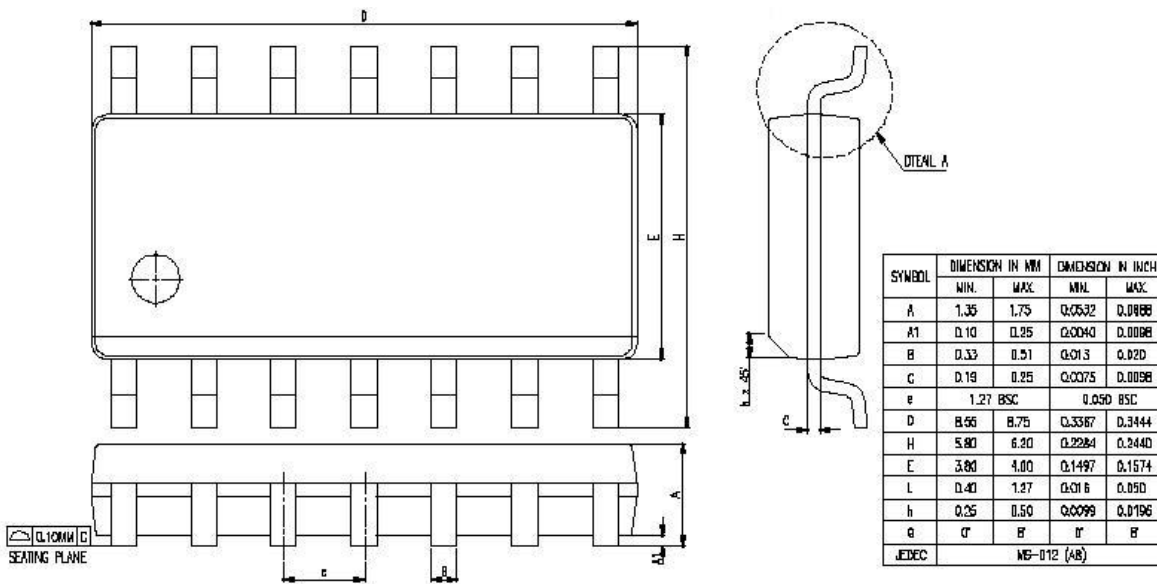
The ordering information:

Ordering number	Package
TR3001-000-15-X	SOP 14-pin (150 mil)

Note: “-X” represents the package material:

- Package material: Pb-free Code: W
- Package material: Green Package Code: G

PACKAGE OUTLINE (SOP14) 150mil



NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD FLASH ,  
PROTRUSIONS OR GATE BURRS.  
MOLD FLASH , PROTRUSIONS AND GATE BURRS SHALL  
NOT EXCEED 0.15 MM ( 0.006 INCH ) PER SIDE.

