

TR3003

PLL for FM stereo transmitter

Data Sheet

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AMENDMENT HISTORY

Version	Date	Description
V1.0	June, 2006	New release.
V1.1	Dec, 2011	Add Ordering Information table

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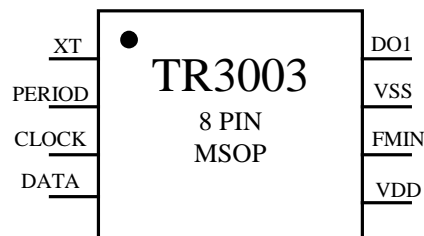
DESCRIPTION

The TR3003 is phase-locked loop (PLL) LSIs for FM stereo transmission application. All functions are controlled through 3 serial bus lines.

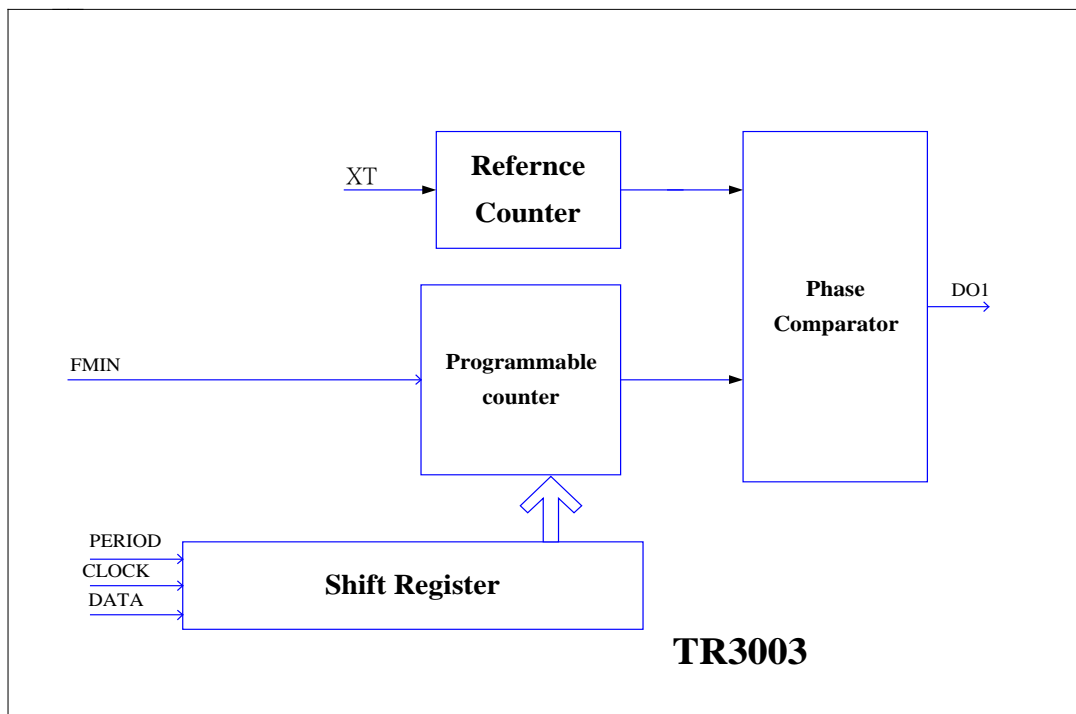
FEATURES

- Operate at input frequency ranging from 30~150 MHz during FMIN input .
- All functions controlled through 3 serial bus lines.
- CMOS structure with operating power supply rang of VDD=2.2~3.6V.

PIN CONFIGURATION



BLOCK DIAGRM



ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD	-0.3~6.0	V
Input Voltage	VIN	-0.3~VDD+0.3	V
Power Dissipation	PD	300	mW
Operating Temperature	TOPR	-10~80	°C

ELECTRICAL CHARACTERISTICS(Ta=-10~80°C,VDD=2.2~3.6V.)

Characteristic	Symbol	Test Condition/Pin	Min	Typ.	Max	Unit
Operating Power Supply Voltage	VDD	PLL operation (normal operating)	2.2	3.0	3.6	V
Operating Power Supply Current	IDD	VDD=3.0V, XT=38KHz, FMIN=100MHz	--	3	6	mA

Operating frequency range

Reference counter input frequency	fXT	Connect 38KHz reference clock to XT		38		KHz
FMIN	fFM	VIN=0.3Vp-p	30	~	150	MHz

PIN DESCRIPTION

Pin No.	Symbol	Pin name	Description
1	XT	reference clock input pin	38KHz reference clock connected to XT
2	PERIOD		All functions controlled through these 3 serial ports
3	CLOCK		
4	DATA		
6	FMIN		This pin input FM band local oscillator signals by capacitor coupling.
8	DO1	Phase comparator output	This pins is for phase comparator tri-state output.
5	VDD	Power supply pins	Applies 2.2V~3.6V
7	VSS		

FUNCTION DESCRIPTION

Serial I/O ports

As the block diagram shows, the functions are controlled by setting data in the 24 bit registers. Each bit of data in the register is transferred through the serial ports between the controller and the DATA, CLOCK and PERIOD pins.

REGISTER ASSIGNMENTS

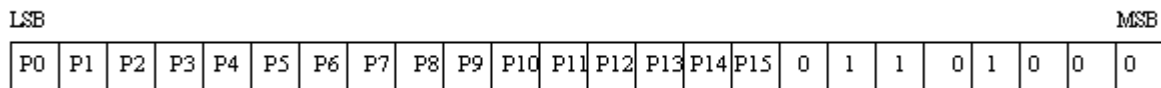


Fig. 1

Serial transfer format

The serial transfer format consists of 8 bits fixed code and 24 data bits (Fig. 2).

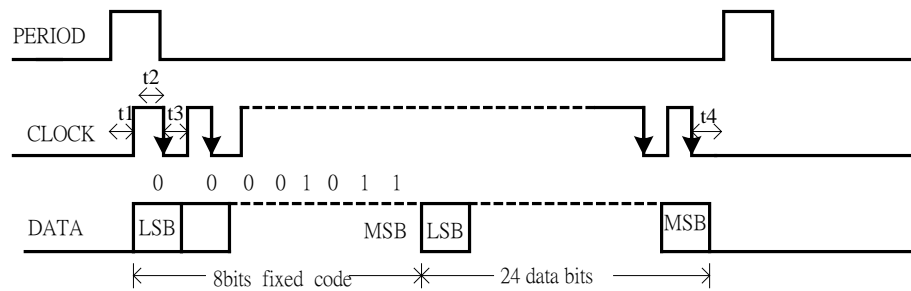


Fig. 2

t1,t2,t3,t4 > 4us

Serial data transfer

Serial data are transferred in sync with the clock signal. In the idle state, the PERIOD, CLOCK and DATA pin lines are all set to “L” level. Since the receiving side receives the serial data as valid data when the clock signal falls, it is effective for the sending side to produce output in sync with the clock signal rise.

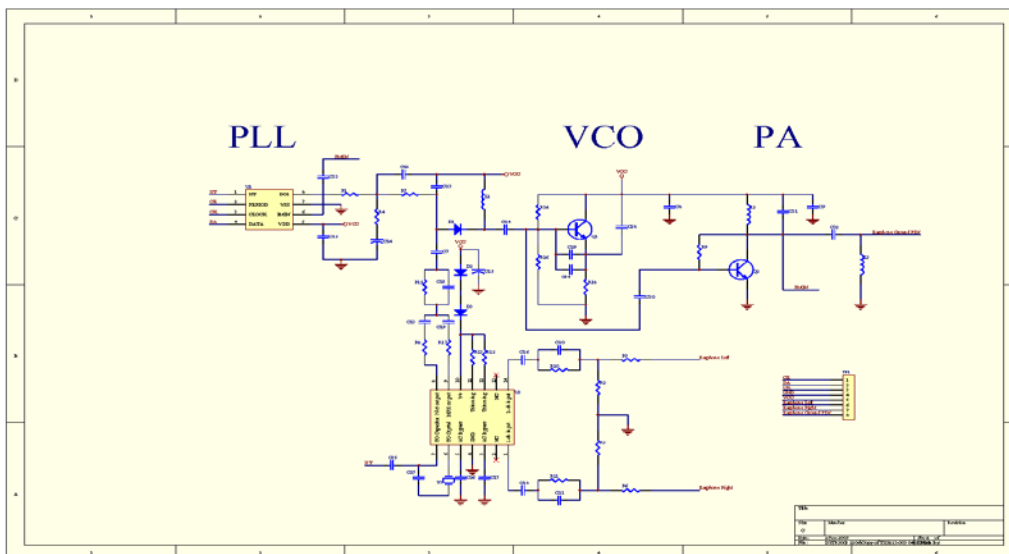
Programmable counter

The programmable counter section consists of 16bit programmable binary counter.(fig.1)

Setting programmable counter

The divisor for the programmable counter is set as binary data in bits P0~P15.(fig.1)
Divisor setting range n=640H~FF00H (1600~65280)

APPLICATION CIRCUIT



ORDERING INFORMATION

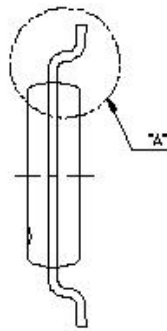
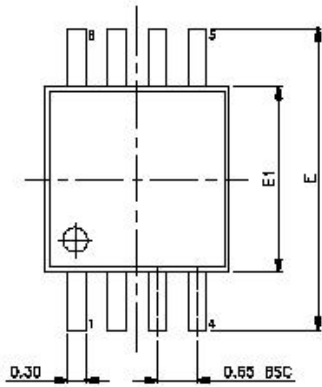
The ordering information:

Ordering number	Package
TR3003-000-52-X	MSOP 8-pin (118 mil)

Note: “-X” represents the package material:

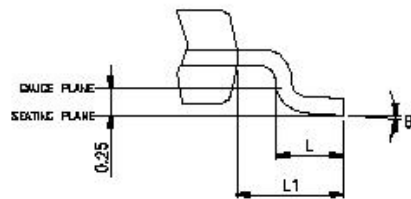
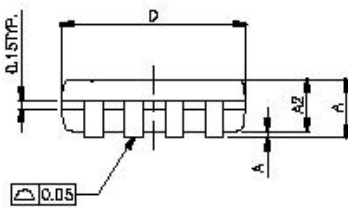
- Package material: Pb-free Code: W
- Package material: Green Package Code: G

PACKAGE OUTLINE (MSOP8)



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
θ°	0	—	8

UNIT : MM



DETAIL A