TRD16P102B

Data Sheet

V1.2

48K Embedded OTP ROM

Hi-Performance 16-bit Multimedia Processor

1. General Description

The **TxP16**™ is a high performance 16-bit MCU, pronounced as **T**ritan e**x**cellent-**P**rocessor16. It is the new generation computational kernel for **TRITAN** TRD16P102B series. It has initially aimed at the areas of controller and multimedia digital signal processing (DSP) application to demonstrate its profession. TxP16 furnish with fast **MAC** architecture, which allows multiplication+accumulation instructions to be issued with access memory simultaneously during one cycles. The TRD16P102B is equipped with TxP16 and integrating input/output ports, PWM, 32768Hz Real Time Clock, Timer and Low Voltage Reset...etc on a chip.

Furthermore, TRD16P102B internal memory capacity includes 48Kx16 program/data OTP ROM plus 3Kx16 working SRAM.

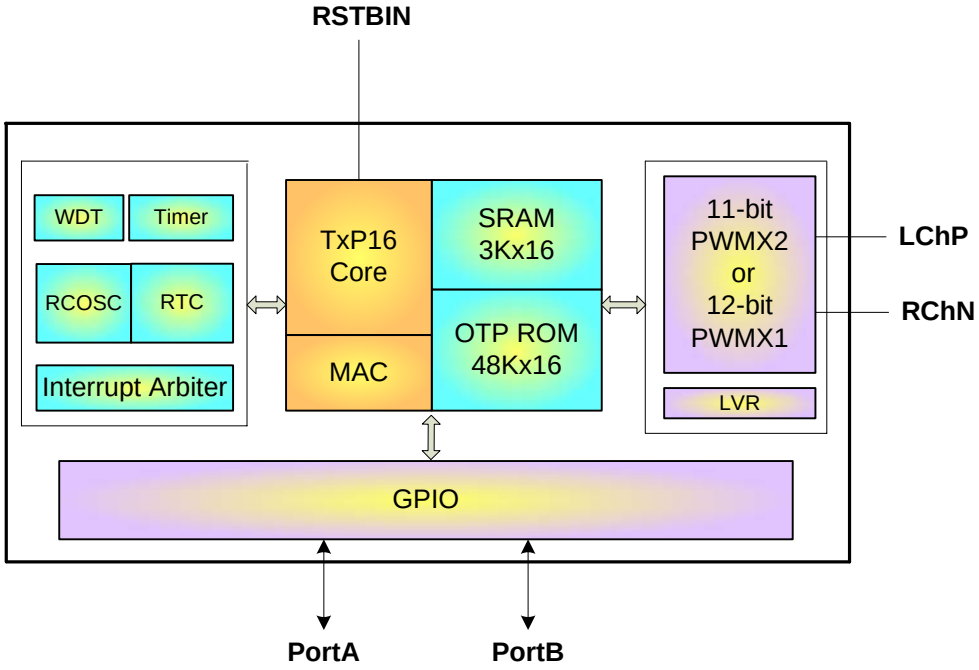
2. Features

- High-performance RISC TxP16 CPU
  - **11Mhz@2.4Volt ~ 3.6Volt**
  - Wide range of operation frequency : **6.55MHz±3%** (6.5MIPS) ~ **10.92MHz±3%** (11MIPS) by option
  - Built-in 3Kx16 SRAM
  - Hybrid Instruction and data memory share with 48Kx16 OTP ROM
  - Embedded PC Stack Level 16
- Rich DSP function
  - Hardware Circular Buffer support
  - MAC Computation power : 11MIPS (max.)
  - Multi-Function Support: In MAC calculation, simultaneously access two operands from memory in one cycle
  - Extend Dynamic Range: A 40-bit accumulator to ensure in 512 successive multiple+additions no overflows
- Software-based audio processing technical
  - Subband, Celp, Melody Synthesis Up to 8 Channels (max.)
- Support 10 General purpose I/O port
- Stereo 11-bit PWM or Mono 12-bit PWM
- 8 interrupt source
  - 5 internal interrupt (PWM, T1, T2, RTC, StackOvl)
  - 2 external interrupt
- Watch dog timer (WDT)
- **Low voltage reset : LVR provide two modes which is always turn on or disabled in halt mode**
- PB0,PB1 support three edge modes for wake-up function , both rising and falling edge trigger, rising edge trigger and falling edge trigger, selected by option.
- Port A support 4 comparators by option
- built-in low power RC oscillator128KHz±30% (typical 3uA,VDD=3v), for 1ms, 2ms, 4ms and 64ms wakeup or real time clock use.

3. Application Field

- PDA
- Electronic Dictionary
- Electronic Learning Aid (ELA)
- Electronics storybook

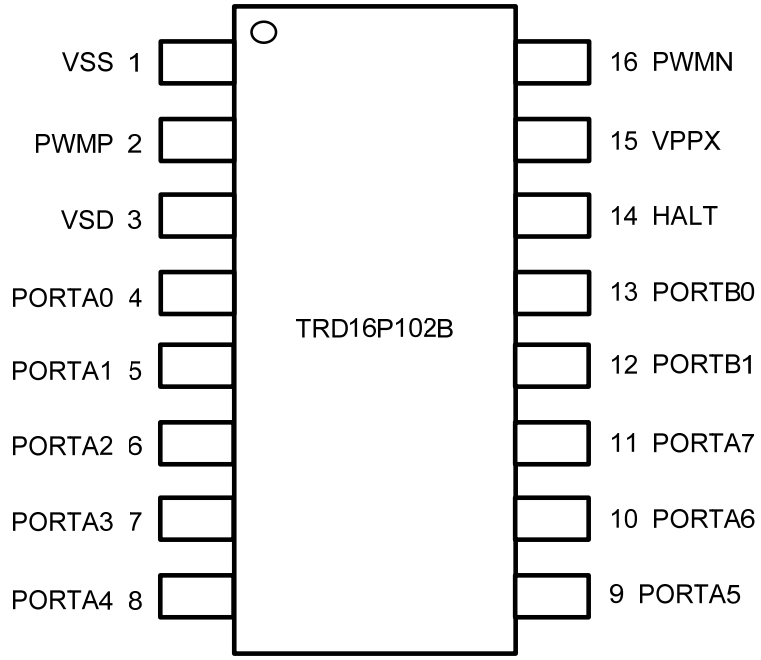
4. Block Diagram



4.1. Dice Pin Assignments /Description

Pin Name	I/O	State after RESET	FUNCTIONS
Chip Power			
VDD	I	High	Digital Power Input
GND	I	Low	Digital Ground
VPPX	I	U	OTP programming Power Supply 7.5V
VPD	I	High	PWM Block Power Input
VPS	I	Low	PWM Block Ground
Chip Control			
TESTIN	I	Low	High force chip enter test mode, internal 50K ohm pull-down
HALT	O	Low	High presents chip in Halt mode
RSTBIN	I	High	Low force chip to enter reset mode, internal 50K ohm pull-up
Clock			
OSCA	I	Clock	Connect to RC OSC Adjust
General Purpose I/O Port			
PortA[7:0]	I/O	Low	PortA is programmable Input/Output port
PortB[1:0]	I/O	Low	PortB is programmable Input/Output port
Audio			
LChP	O	High	Digital PWM output(+)
RChN	O	Low	Digital PWM output(-)

4.2. SOP16 Pin Assignments /Description



5. Function Descriptions

5.1 TxP16

As shown in the block diagram in Figure 4.1, the TxP16 with MAC module is a 16-bit data width processing capability and all instructions are operated in one cycle except parameter data ROM(PM) access. The TxP16 not only provides general arithmetic such as addition, subtraction, shifter, and other logical operations, but it also involves MAC and circular buffer operations for complexity digital signal processing.

5.2 TxP16 Registers

The TxP16 contains of register files are illustrated below:

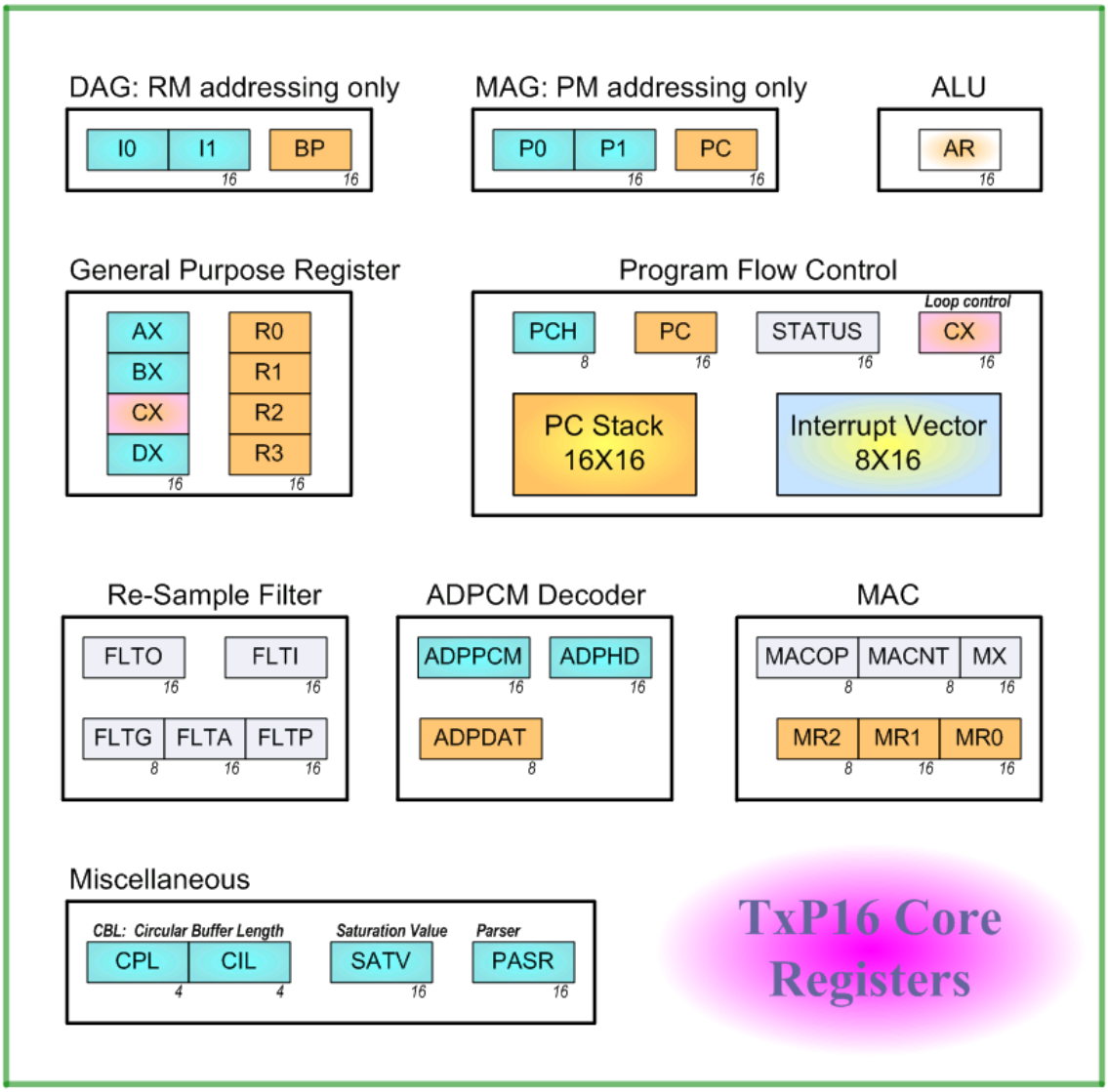


Figure 5.1 TxP16 Processor Core Registers

■ REGISTER FILES DEFINE:

AR: Accumulator Register
I0: Index 0 Register
I1: Index 1 Register
BP: Base Pointer Register
P0: Pointer 0 Register
P1: Pointer 1 Register
MACOP: MAC Operation Register
MACNT: MAC Operation Loop Counter
MX: MUL/MAC Input X Register
MR0: MUL/MAC Result Register 0
MR1: MUL/MAC Result Register 1
MR2: MUL/MAC Result Register 2
AX: General AX Register
BX: General BX Register
CX: General CX Register
DX: General DX Register
R0: General R0 Register
R1: General R1 Register
R2: General R2 Register
R3: General R3 Register
CBL: Circular Buffer Length Register
PASR: Parser Register

5.2.1 Special Registers

- Accumulator Register

The AR is a general-purpose 16-bit register that stores the result of last arithmetic or logical operation. In addition, any data write to AR will affect the status flag.

- Stack Pointer

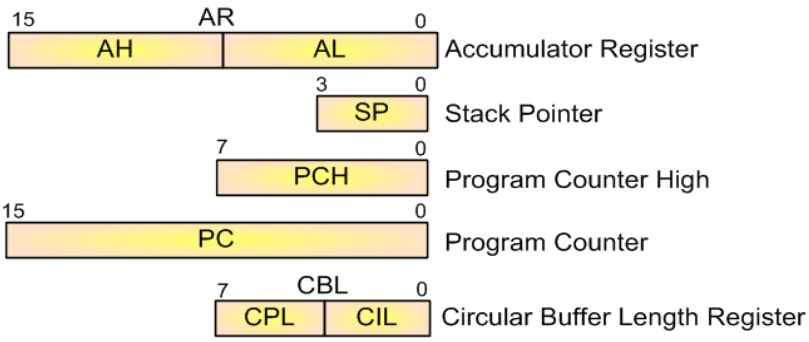


Figure 5.2 TxP16 Special Registers

The SP is a 4-bit register that is for addressing Stack position. The SP will automatically increment / decrement cause by instruction “CALL” / “RETS”, and more detail revealed as the “PC Stack” section.

- Program Counter

The 16-bit PC register provides 64K-word addressing capability. It is responsible for MCU fetch now executing instruction.

- Program Counter High

The instruction “LJMP” and “LCALL” will reference PCH register to composed of 16-bit pointer provides the 64K words PM addressing range.

- Circular Buffer Length Register

Many algorithms such as convolution, correlation, and digital filter require the circular data buffers. The TxP16 supports circular buffer operating via the I0 vs. CIL and P0 vs. CPL. The modulus logic implements automatic modulus addressing for accessing RM/PM circular buffer data.

5.2.2 Common I/O Registers

The TxP16 involves 32 common I/O registers are shown in Table 5.1. There are defined the peripheral IO control and system register.

Symbol	Adr	Reset	RW	B15/b7	b14/b6	b13/b5	b12/b4	B11/b3	B10/b2	b9/b1	b8/b0	Description
STATUS.L	00H	20	R/W	INTEN			AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR						
INTENA	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Interrupt Enable
INTREQ	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Interrupt Request
IntVect	03H	XX	R/W	IntVect[15:0]								Interrupt Vector access Window
IOC_PA	04H	00	R/W	IOC_PA[7:0]								“1”= out, “0” = in of related PA bit
IOC_PB	05H	00	R/W	IOC_PB[1:0]								“1”= out, “0” = in of related PB bit
Reserve	06H	XX	XX									Reserve
PortA	07H	XX	R/W	PortA[7:0]								Read: in port Write: out port
PortB	08H	XX	R/W	PortB[1:0]								Read: in port Write: out port
Reserve	09H	XX	XX									Reserve
Reserve	0AH	XX	XX									Reserve
Reserve	0BH	XX	XX									Reserve
Reserve	0CH	XX	XX									Reserve
Reserve	0DH	XX	R/W									Reserve l
Reserve	0EH	XX	R/W									Reserve
Reserve	0FH	XX	XX									Reserve
Reserve	10H	XX	XX									Reserve
Reserve	11H	XX	XX									Reserve
Reserve	12H	XX	XX									Reserve
Reserve	13H	XX	XX									Reserve
Reserve	14H	XX	XX									Reserve
Reserve	15H	XX	XX									Reserve
DACL	16H	XX	W	DACL [15:0]								Audio L Channel
DACR	17H	XX	W	DACR [15:0]								Audio R Channel
Reserve	18H	XX	XX									Reserve
Reserve	19H	XX	XX									Reserve
Reserve	1AH	XX	XX									Reserve
Reserve	1BH	XX	XX									Reserve
Reserve	1CH	XX	XX									Reserve
ClrWDT	1DH	XX	W									Clear WDT
RealT	1DH	00	R	RealT[15:0]								Watch Dog Real-Time Counter
IOP_IX	1EH	XX	W	IOPIX7	IOPIX6	IOPIX5	IOPIX4	IOPIX3	IOPIX2	IOPIX1	IOPIX0	Programming IO Port index
IOP_DAT	1FH	XX	W	IOPD[15:0]								Programming IO Port Data

Table 5.1 Common I/O registers

5.2.3 Basic System Registers

◆STATUS register

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS.L	00H	20	R/W	INTEN			AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR						

The Status register provides two main functions, the first system flag holds the status information generated by the computational blocks of the TxP16, which used for program sequencer control. The second indicated that special function of hardware module is enable or not.

For program flow control:

System Flag	**Definition**
AZ	ALU or AR Result Zero
AN	ALU or AR Result Negative
AV	ALU Overflow
AC	ALU Carry
PA	Parser Queue available(Read only)
FA	Filter buffer available(Read only)

System hardware control:

System Flag	Definition
INTEN	System global interrupt control bit
IntVWR	Interrupt Vector Table access window control bit

◆ Address 01H~02H: Interrupt control registers, the detail are illustrated in Interrupt section.

◆ Address 04H~1CH: GPIO registers, the detail are illustrated in GPIO section.

◆ Virtual Programming IO

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
VIO_IX	1EH	XX	W	IOPIX7	IOPIX6	IOPIX5	IOPIX4	IOPIX3	IOPIX2	IOPIX1	IOPIX0	Programming IO Port index
VIO_DATA	1FH	XX	W	IOPD[15:0]								Programming IO Port Data

Table 5.2 Virtual Programming IO

The operation steps of these group register, first select virtual IO port index then write data to programming IO port.

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
Timer1	00H	XX	W	Timer0[15:0]								Timer1
Timer2	01H	XX	W	Timer1[15:0]								Timer2
RTCTimer	02H	00	W	-	-	-	-	-	-	DIVSEL1	DIVSEL0	RTC RC-oscillator divider

5.3 PC Stack

The PC STACK is TxP16 special embedded memory used to save (PC+1) value, which is composed with 16-level.

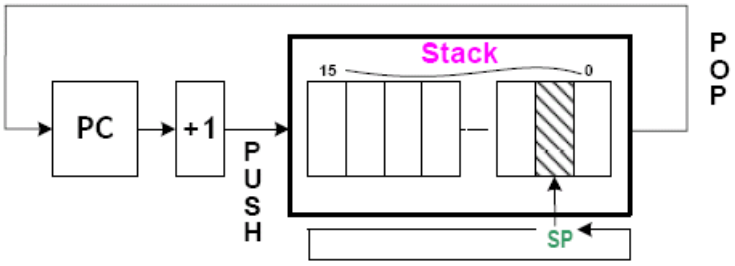


Figure 5.3 PC Stack Structure

Stack's top value is indexed by stack pointer (SP) register. When CALL instruction is executed, then the (PC+1) will PUSH onto stack addressing by SP and it will auto increment. At the end of subroutine when RETS instruction is executed the SP will auto decrement and stack content of pointer by SP will POP into PC.

The contents of STACK and SP are neither readable nor writeable by instruction. The SP is initialized to “0” after RESET.

5.4 Interrupt

5.4.1 Interrupt Vector Table

The Interrupt Vector Table is TxP16 special embedded memory, which is composed with 8-level of FIFO, used

to store the index of interrupt service routine (ISR) address. User can access Interrupt Vector Table by read/write IntVect I/O register.

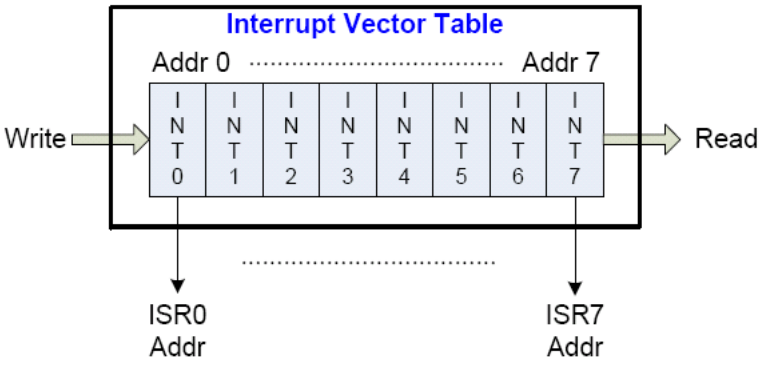


Figure 5.4 Interrupt Vector Structure

5.4.2 Interrupt Controller

Common I/O registers

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS	00H	00	R/W	INTEN				AN	AV	AC	AZ	System Status Flag
INTENA	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Int Enable
INTREQ	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Int Request

This chip provides 8 interrupt sources, user's program can control 8 interrupts, including 6 internal PWM Timer, Timer1, Timer2, RTC Timer and PC Stack Overflow interrupts, and 2 external ExtINT0, ExtINT1, interrupts. More details control will describe as follows:

Interrupt Source	Interrupt Vector	Priority
PWM Timer	0H	INT0_IRQ
Timer1	1H	INT1_IRQ
Timer2	2H	INT2_IRQ
RTC Timer	3H	INT3_IRQ
ExtINT0 Port A.b6	4H	INT4_IRQ
ExtINT1 Port A.b7	5H	INT5_IRQ
Reserve	6H	INT6_IRQ
PC Stack Overflow	7H	INT7_IRQ

Table 5.2 TRD16P102B Interrupt Sources

(a) Global interrupt enable(INTEN)

The global interrupt INTEN controls the enable/disable of all interrupts. When INTEN is cleared to "0", all interrupts are disabled. When INTEN is set to "1", all interrupts are enabled (but still dependent on value of INTENA register). The INTEN is initialized to '"0" after power on

(b) Interrupt enable (INTENA)

The interrupt enable ENA0, ENA1, ENA2, ENA3, ENA4, ENA5, ENA6, ENA7 are shown in above. An interrupt is allowed when these control bit are set to "1", and interrupt is inhibit when these control bit are cleared to "0". They are all initialized to "0" after power on.

(c) Interrupt request (INTREQ)

If an interrupt **raising edge** request is generated, the related interrupt request bit is set to “1” by hardware and waits for interrupt accept. INTREQ can be cleared to “0” by software. Hardware will not clear this bit. INTREQ are all initialized to “0” after power on.

5.4.3 Interrupt Processing

When any interrupt request(INTREQ) is generated, the acceptance of interrupt is decided by the interrupt enable(ENA) and global interrupt enable(INTEN). If the interrupt enable and global interrupt enable related bit are set to “1”, that interrupt will be accepted on the next clock. These following procedures will automatically be done in one clock cycle by hardware showing below:

(1) Program Counter(PC), PCH, AR and FLAG will be stored in special hardware registers.

(2) PC will be set to the corresponding interrupt entry address by refer to interrupt vector table.

(3) The global interrupt enable (INTEN) is cleared to “0”, which avoids the nest interrupt happened.

When interrupt service routine was finished, an RETI instruction will perform the procedures by hardware showing as follows:

(1) Restore the stored PC, PCH, AR and FLAG.

(2) The global interrupt enable (INTEN) is set to “1”, which allows to accept the subsequent interrupt.

Before executing RETI instruction, the corresponding interrupt request (INTREQ) bit must be cleared to “0” by software. If the request bit is not cleared, the same interrupt will be accepted again.

5.3 MAC (16-bit X 16-bit Multiplier and Accumulator)

A 16 bit x 16 bit MAC is provided for digital signal processing. The core of MAC operation is multiply MX&MY with 2'S complement operand and accumulation previous 40-bit MF then rounding store result in the 40-bit MR register. The basic MAC architecture is shown as Figure 5.5.

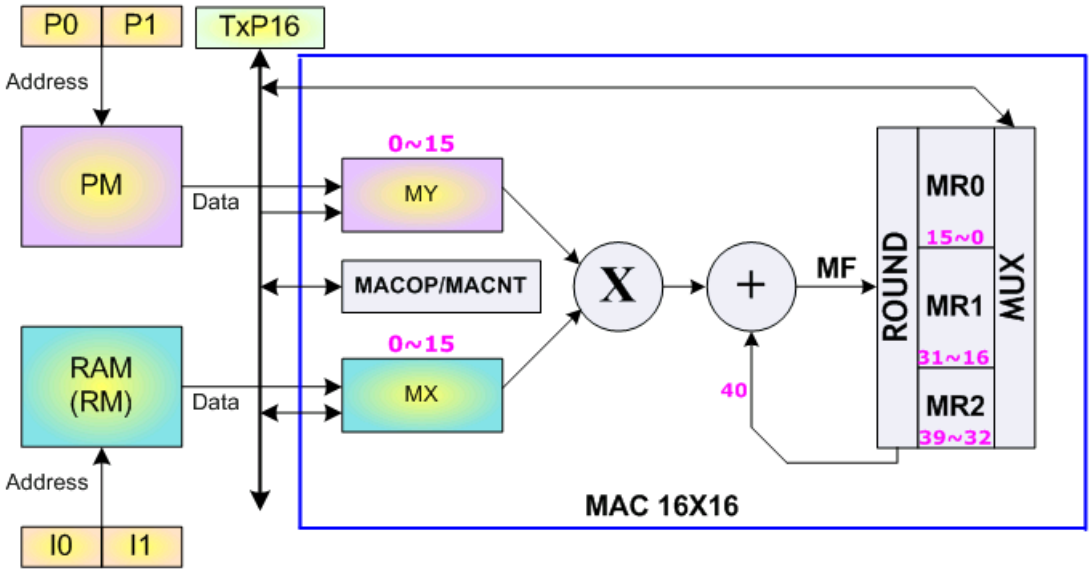


Figure 5.3 MAC Architecture

Define MAC module registers:

MX: MAC input 16-bit X register

MR: Multiplier or MAC result 40-bit register

MACOP: MAC operation define register

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
MACOP	00	R/W	RND1	RND0	P0/P1	POP:+/-	I0/I1	IOP:+/-	MY:SU(01)	MX:SU(01)	MAC Operation Setup

MACNT: MAC equation loop counter, max to 255

Basically, multiplier operates equation:

MR = MX*MY(SU) → MX: signed, MY: unsigned

Permission MY is AR or immediate value (-128~127), MX and MY are signed or unsigned assign by MACOP. So, actual multiplier instruction likes this:

MR = MX*AR or MR = MX*56

The operation of MAC equation is:

MR = MR + (MX*MY(SU))<<RND, MX=RM[I0++], MY=PM[P1--]

The means of equation is signed MX multiply unsigned MY the result value shift left RND bits and add previous MR then write back to MR.

Simultaneously, load new value to MX fixed from RM[index operation]

MY fixed from PM[pointer operation]

Therefore, MAC array operation like this:

```
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
                    .
                    .                                   Successive 64 times
                    .
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
```

Actual just one line of instruction present in assembly coding like this:

MACNT = 63

This is very benefit for reducing code size. Of curse, we need setup MACOP register previous; at this example is like this;

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
MACOP	00	R/W	RND1	RND0	P0/P1	POP:+/-	I0/I1	IOP:+/-	MY:SU(01)	MX:SU(01)	MAC Operation Setup
			0	1	1	1	0	0	0	0	

Note: Successive MAC operation will cause MCU interrupt disable.

6. Memory Configuration

6.1 Internal Program/Parameter Memory

TxP16 consider both instruction and data ROM are the same as program ROM(PM), so it's very flexible and efficient for instruction and data memory allocation in PM. On the logical PM space is organized into 64kx16-bit which is addressed by memory address generator unit (MAG). Actual PM is separated into two parts including read only 48K OTP ROM(Page0) and write available 16-word SRAM(Page1). User can dynamic download program/data to page1 for MCU get more flexible operation. More details control will describe as follows:

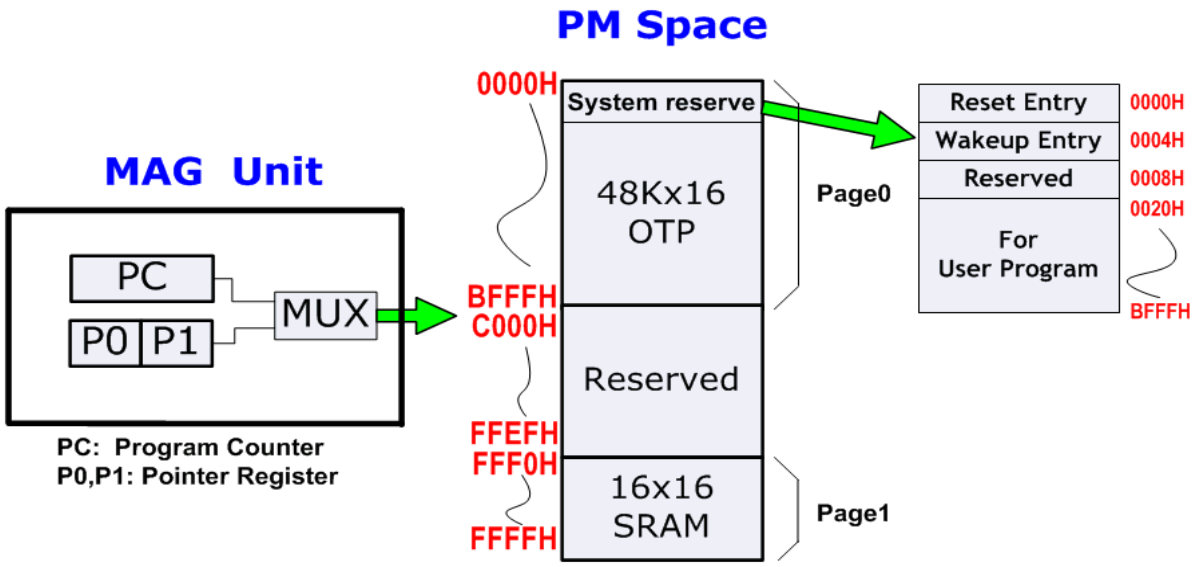


Figure 6.1 TRD16P102B PM block diagram

When TxP16 executed an instruction, the PM address is generated from PC register. Similarity, when it access a word data, the PM address is composed with 16-bit from P0 or P1. System will auto adjust execute target space when program context switch between page0 and page1.

6.2.1 Internal Data Working SRAM

The internal data working ram space is totally 3kX16-bit that named as RM. Addressing ranged from 0000H through 0BFFH, which is generated by Data Address Generator Unit (DAG). Note: Index register (I0,I1,BP) are 16-bit width, but RM address line is only 12-bit width(0~3071); therefore, RM address will be warping when index value exceed 3071.

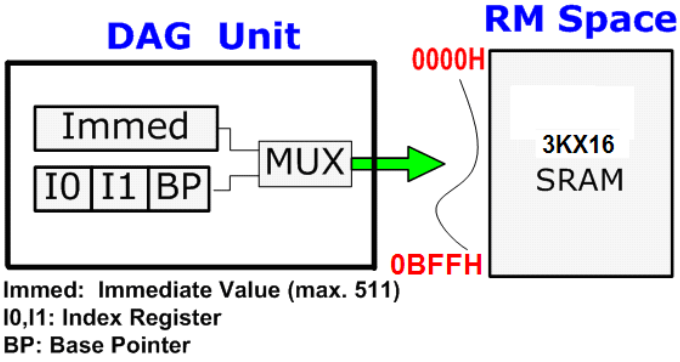


Figure 6.2 TRD16P102B RM block diagram

6.2.2 Data Stack

A Last In First Out (LIFO) STACK is implementation for temporary data storage in RM memory. Generally, Data Stack is start-up at the bottom of RM, so BP is usually set to 0x0BFFH.

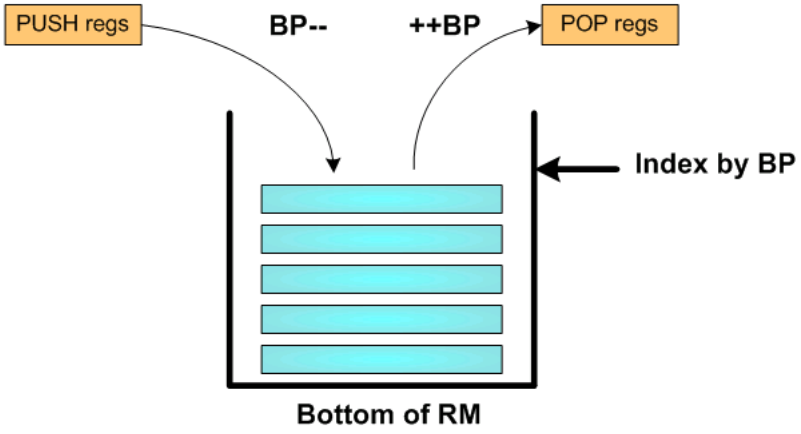


Figure 6.3 Data Stack Structure

Data Stack's top value is indexed by base pointer (BP) register. When PUSH instruction is executed, the “regs” will PUSH onto stack which address by BP and it will auto decrement. If POP instruction is performed, the BP will auto increment and stack content of pointed by BP will POP into “regs”.

7. Peripherals

7.1 Programmable Timers

Common I/O registers

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS	00H	0X	R/W	INTEN			AQ	AN	AV	AC	AZ	System Status Flag
INTENA	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Int Enable

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
Timer1	00H	XX	W	Timer0[15:0]								Timer1
Timer2	01H	XX	W	Timer1[15:0]								Timer2
RTCTimer	02H	00	W	-	-	-	-	-	-	DIVSEL1	DIVSEL0	RTC RC-oscillator divider

7.1.1 PWM Timer

PWM timer is fixed generate 32kHz interrupt request when INTENA0 bit is turned on, *If Auto FIFO_EN is setting the interrupt request rate = Ft/FIFO_Length.*

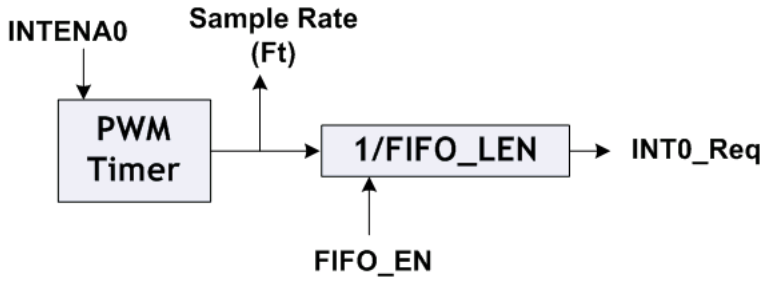


Figure 7.1 PWM Timer Structure

7.1.2 Timer1 & Timer2

The clock source of Timer1&Timer2 comes from fixed 32.768Mhz, It contains 16-bit write-only counter register. If Timer enable correspond with the INTENA bit is turned on then counting to time out, an interrupt request will be generated. At the same time, TnC in Eq.(7.1.1) will be reloaded into Timer register and up-count again. If the global interrupt enable, an interrupt signal is generated at the next clock.

Int1_Req= 32.768Mhz/(TnC+1) ---- (7.1.1)

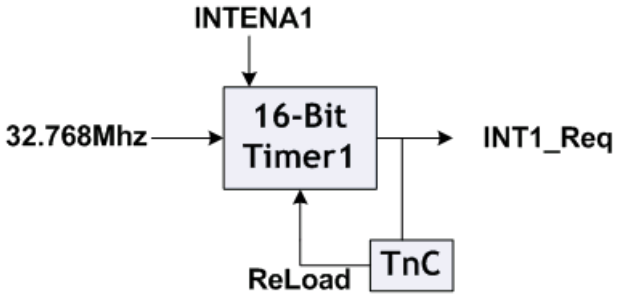
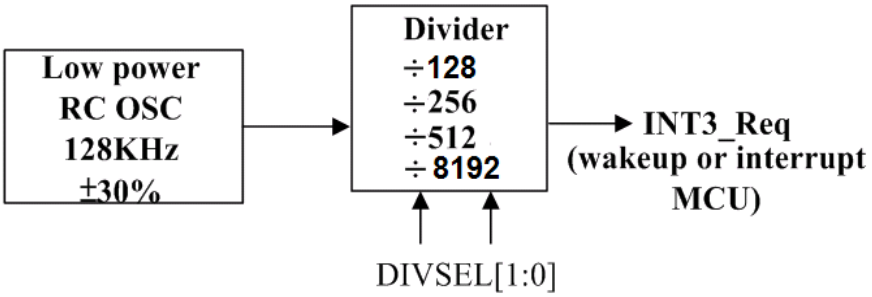


Figure 7.2 Timer1&Timer2 Structure

7.1.3 Low power RC oscillator for RTC Timer

Low power RC oscillator 128KHz is used for generating 1ms, 2ms, 4ms and 64ms interval to wake-up MCU when in halt mode or interrupt in normal mode. There is about 30% frequency deviation of RC oscillator 128KHz by different lot or chip. The wake-up function can be disabled by option, default wake-up function is enabled and INT3_Req is set to high after 1ms when reset occurred. The counter of divider will be reset once while going into halt mode, and MCU will be wake-up or interrupt after 1ms if DIVSEL1,DIVSEL0=00. The power consumption of RC oscillator is about 3uA typically, VDD=3V.



DIVSEL1	DIVSEL0	Period
0	0	1ms
0	1	2ms
1	0	4ms
1	1	64ms

Figure 7.3 RTC Timer Structure

Notice: IDE Tool has Demo Code to illustrate RTC Timer auto-calibration function.

7.2 General Purpose I/O Ports

The TRD16P102B provides 2 I/O ports for user application. There are three I/O port, PA0~PA7, PB0~PB1. PA0~PA7, PB0~PB1 wake-up function enable or disable by programmed option, and PA7~ PA6 is external interrupt pin. The pull-high or pull-low 50k resistor of each pin can be programmed by option. The basic I/O schematic is showed in Figure 7.4.

These totally 10 I/O pins work only just a general input/output port function. For more detail please refer to relative section.

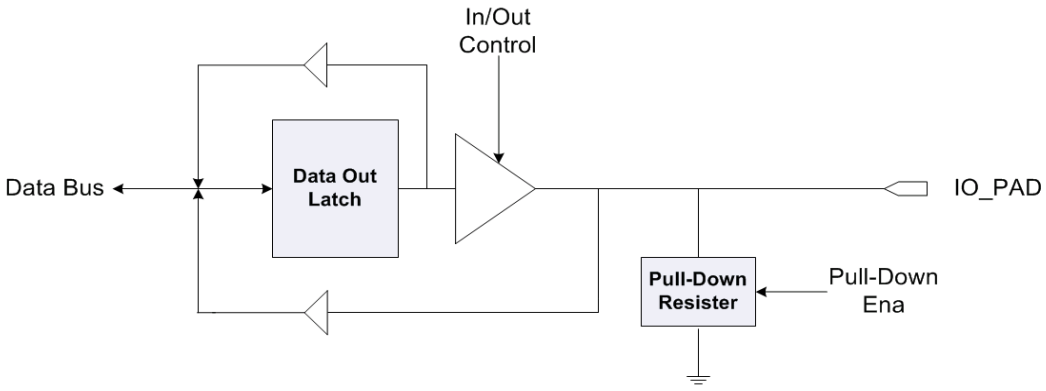


Figure 7.4 Basic I/O Configuration

PB0,PB1 support three edge modes for wake-up function , both rising and falling edge trigger, rising edge trigger and falling edge trigger, selected by option.

The PortA0~PortA7 also provides 4 comparators configuration for user application that each comparator enable or disable by programmed option.

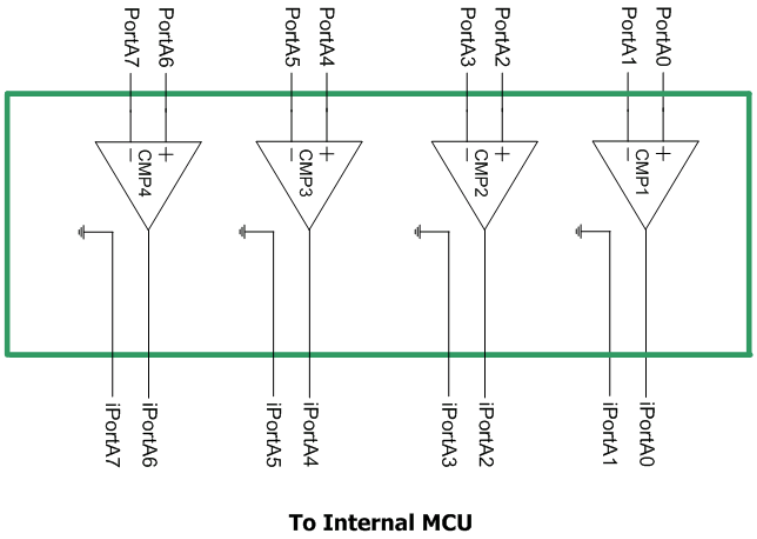
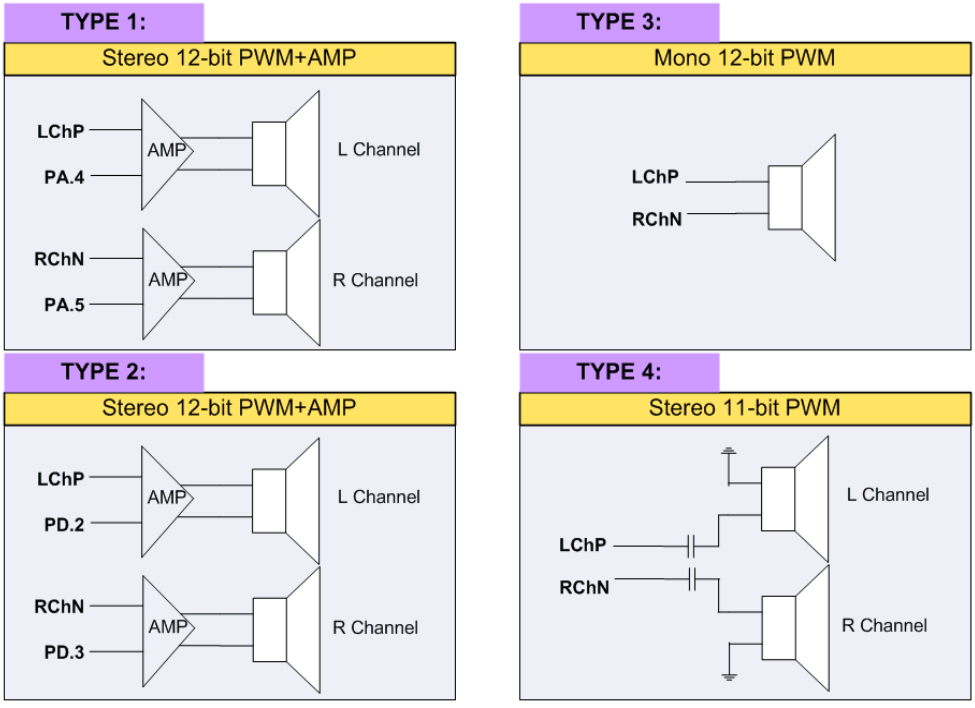


Figure 7.5 Comparator Configuration

7.3 Audio Output

The three kinds of audio output form in TRD16P102B system are stereo 11-bit PWM, stereo 12-bit PWM and mono 12-bit PWM. The kind of solution is determined by user's application. Notice that only one type of audio form can be selected at each time, which assign by option. The PWM PIN configuration shows as below:



Notice:TRD16P102 not supports TYPE2.

Figure 7.6 PWM output configuration

7.3.1 Stereo PWM Output

Two 12-bit of PWM convert are built-in TRD16P102B1A for stereo audio application. In order to get more output power driving, which require external amplifier for stereo output pin **LChP** and **RChN.**

Common I/O registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
DACL	16H	XX	W	DACL [15:0]								DAC Audio L Channel
DACR	17H	XX	W	DACR [15:0]								DAC Audio R Channel

7.3.2 PWM Output

A 12-bit of PWM amplifiers is built-in TRD16P102B system. This amplifier can be used to direct drive 8 ohm speaker without any external circuit.

Common I/O registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
DACL	16H	XX	W	DACL [15:0]								12-bit PWM Channel

7.4 Auto-FIFO

The Auto-FIFO allows user transfer base on 4-level of data to PWM D/A. In some case of frame base applications that data transfer is more efficient than sample base. It is advantageous to decrease number of context switch between main program and interrupt service routine (ISR). The FIFO structure reveal as below:

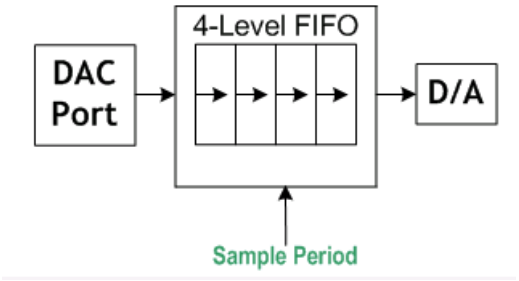


Figure 7.7 Auto FIFO Structure

An interrupt is generated when an entire 4-level FIFO is transfer completed (D\A FIFO buffer is empty), then interrupt service routine should re-load 4-level data to FIFO at ones during 32K sample period. The FIFO will automatically shift-out data to PWM D/A at each sample period.

Note: Auto-FIFO is enable/disable by option setup up.

8. System Control

8.1 Halt Mode & Wake up

The TRD16P102B is changed into HALT mode (system clock stop, RTC stop by OPTION setup) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The RTC timer, PA0~PA7 and PB0~PB7 are supporting the wake-up MCU function when related I/O port raising/falling edge which selects by option. The program counter will be 04H when HALT instruction executed immediately; in addition, MCU will release HALT state and program counter go-to next address after 16us stable clock(system clock) when wake up condition occurred. During the Halt mode period, the SRAM will keep their previous data without changing, yet INTENA register will auto clearly.

8.2 Watch Dog Timer Reset (WDT)

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
ClrWDT	1DH	XX	W									Clear WDT
RealT	1DH	0000	R	RealT[15:0]								Watch Dog Real-Time Counter

The watch dog timer (WDT) is used to reset whole chip when detect unexpected execution sequence of instructions caused by accident condition, avoiding dead lock of MCU program. This special timer can be setup counter-period by option, which range form 1s to 128ms. Software shall run an "clear watch dog timer"(CLRWDT) instruction before this timer time out. It will generate a reset signal to reset whole system when WDT overflow.

WDT will be reset when wake-up from halt or after power on or software clear. In test mode, watch dog timer will be disabled no matter watch-dog-timer is time-out or not. If programmer read the "RealT" register, it can get the content of watch dog timer base on 31.25us.

The reset watch dog timer code syntax is strongly recommended as: "**CLRWDT = AR**".

8.3 Low Voltage Reset

When VDD power is applied to the chip, the low voltage reset is initially enabled by default, it will be disabled when in halt mode. The internal system reset will be generated if VDD power below about 1.9v.

8.4 Reset System

The TRD16P102B reset is come from four signals which are power on reset, low voltage reset(LVR), external "RSTBIN" pin and WDT overflow reset. A dedicated resetb input pin is provided to reset this chip. For normal operation of this chip, a good reset is needed. This pin has 50K ohm pull up resistor. The operation frequency of MCU will go back to OTP page mode when reset occurred.

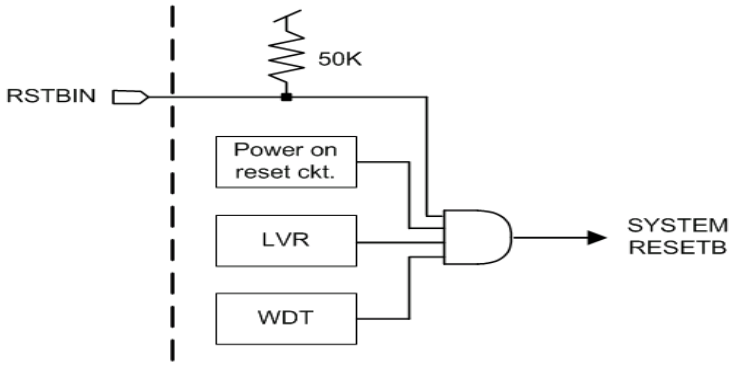


Figure 8.1 Reset system block diagram

8.5 Clock System Architecture

The TRD16P102B clcok system provides 32.768 MHZ System-Clock and 128KHz Real-Time-Clock. The RC oscillator frequency can be optional adjustment by external OSCA pin.

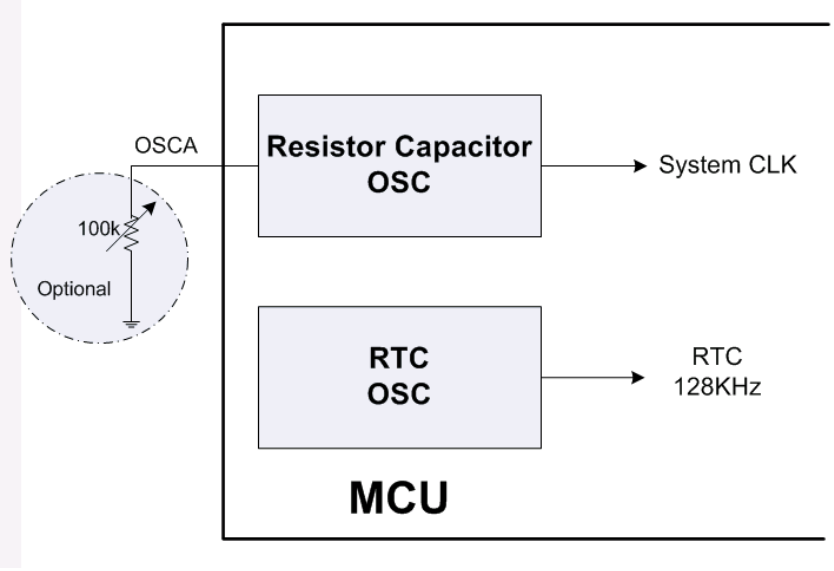


Figure 8.2 Clock System Configuration

9. Electrical Characteristics

9.1 Absolute Maximum Rating

Parameters	Symbol	Value	Unit
DC Supply Voltage	VDD	<3.6	V
Input Voltage	Vin	-0.5 to VDD+0.5	V
Operating Temperature Range	Ta	0 to 75	℃
Storage Temperature Range	Tstg	-50 to 150	℃

9.2 DC/AC Characteristics

VDD=3.0V, Ta=25℃ unless otherwise noted

Parameters	Symbol	Minimum	Typical	Maximum	Test Condition
Operating range	VDD	2.4 V	-	3.6 V	
RC oscillator frequency	Frc1		10.92MHz ±3%		
Low power RC oscillator frequency	Frc2		128KHz ±30%		
Halt Current	Ihalt1		5uA	8uA	All function off, except low power RC OSC
Halt Current	Ihalt2		<2uA		All function off
VPPX pin programming voltage	VPPX		7.5 ±0.25V		
Operating Current	Iop		10mA		no load
input high voltage	Vih	0.8 VDD			
input low voltage	Vil			0.2 VDD	
input leakage Current	Ilk			0.1 uA	
output high voltage	Voh	0.95 VDD			no load
output low voltage	Vol			0.05 V	no load
output high current1	Ioh		12 mA		Vout=2.4V, PortA[7:0]
output high current2	Ioh		5.4 mA		Vout=2.4V, PortB[1:0]
output low current1	Iol		-20 mA		Vout=0.8V PortA[7:0]
output low current2	Iol		-8 mA		Vout=0.8V PortB[1:0]
pull-down resistance1	Rpd1		100 K ohm		pins with pull-down, Port A
pull-down resistance2	Rpd2		50 K ohm		pins with pull-down, Port B

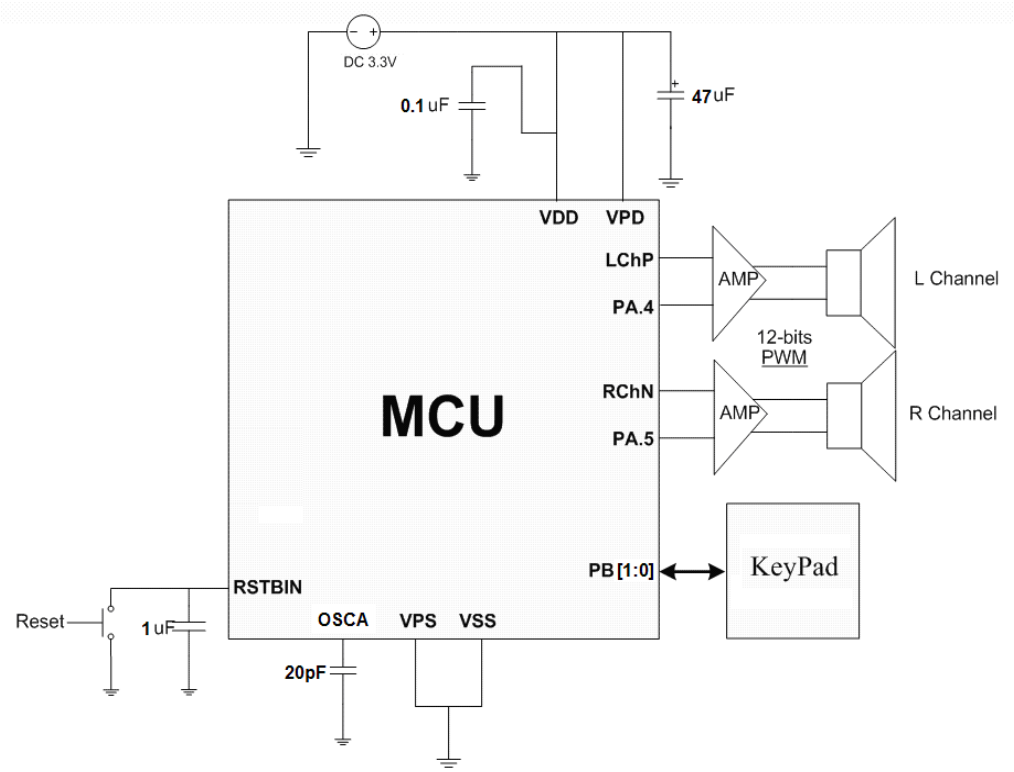
10. Development Support

TRITAN TRD16P102B™ family series are supported with full range of hardware and software development tools:

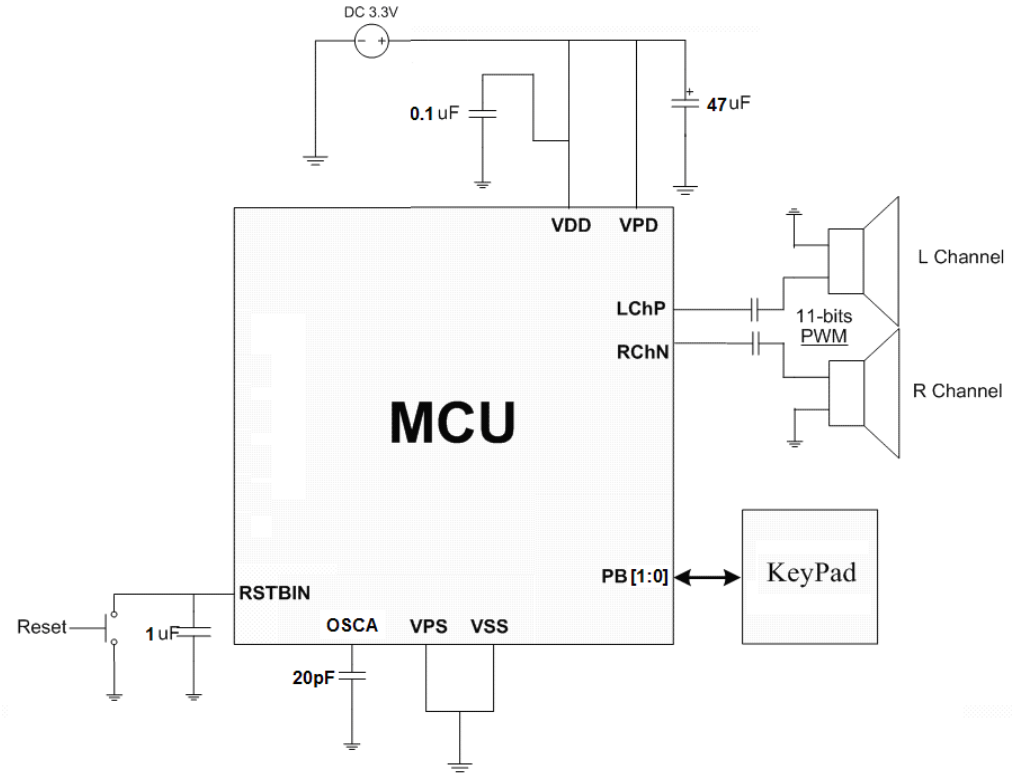
- Integrated Development Environment (IDE)
  - TRD16DevIDE software
- TRD16DevIDE contains
  - TxPASM Assembler
  - TxPCC C Compiler
  - TxPLink Object Linker
  - TxPLib Library Management
- Simulator
  - TRD16SIM software Simulator
- Emulator
  - TRD16ICE circuit hardware Emulator

Application Circuit:

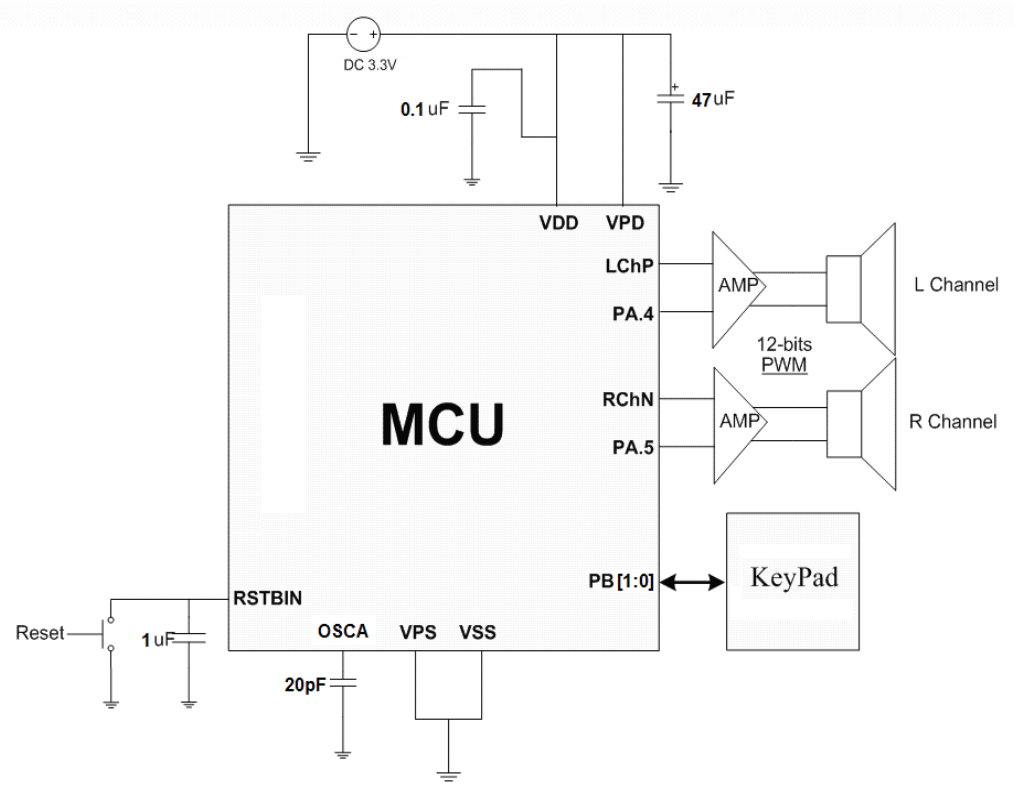
Application Circuit 1.a : Stereo 12-bit PWM AMP output



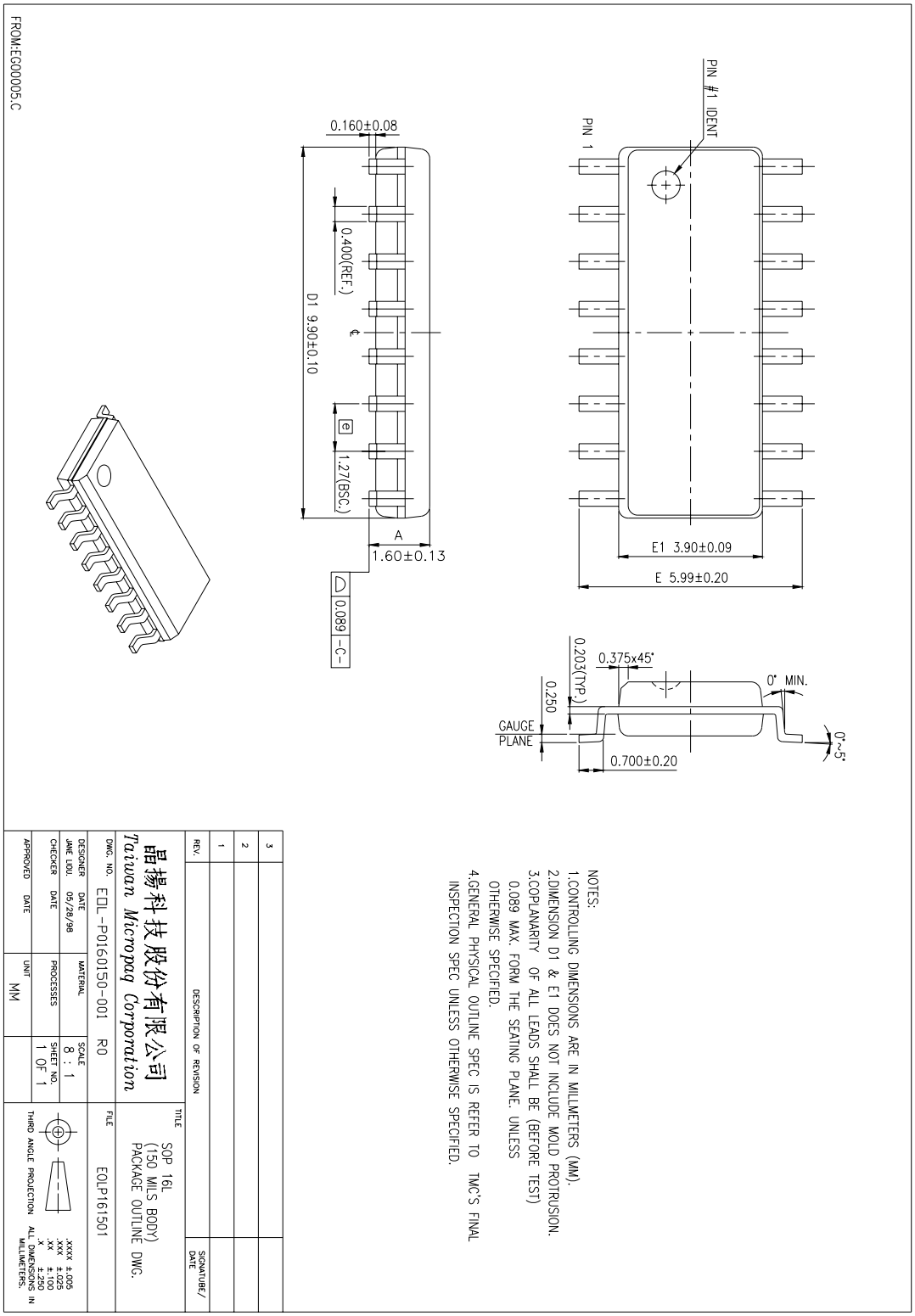
Application Circuit 1.b : Stereo 11-bit PWM output



Application Circuit 1.c : Mono12-bit PWM output



11. SOP 16 outline drawing



12. Revision history

REVISION	DESCRIPTION	PAGE	DATE
V1.0	New establish		2010.05.24
V1.1	Add SOP16 outline drawing & pin assignment		2010.06.24
V1.2	Update 40-bit accumulator Parameter	P2	2010.08.16
	Update Data Stack Description	P14	