TRF3722 Quadrature Modulator with Integrated PLL and VCO

1 Features

- IQ Modulator with Integrated PLL and VCO
- Integer-N/Fractional-N PLL
- Modulator Supports 400 MHz to 4200 MHz
- PLL and VCO Supports 280 MHz to 4100 MHz
- OIP3 at 900 MHz = 31 dBm
- OIP3 at 1800 MHz = 30 dBm
- VCO 1800-MHz Open Loop Phase Noise = –141 dBc/Hz at 1 MHz Offset
- Independent LO Output Supports divide-by 1/2/4/8
- Modulator Low Power and High Gain Modes
- Multiple Power Down Modes

2 Applications

- Wireless Infrastructure
  - CDMA: IS95, UMTS, CDMA2000, TD-SCDMA
  - LTE, TD-LTE, LTE Advanced
  - TDMA: GSM, EDGE, MC-GSM
- Point-to-Point Microwave, Point-to-Multipoint Microwave
- Software Defined Radios
- RF Repeaters, Distributed Antenna Systems

3 Description

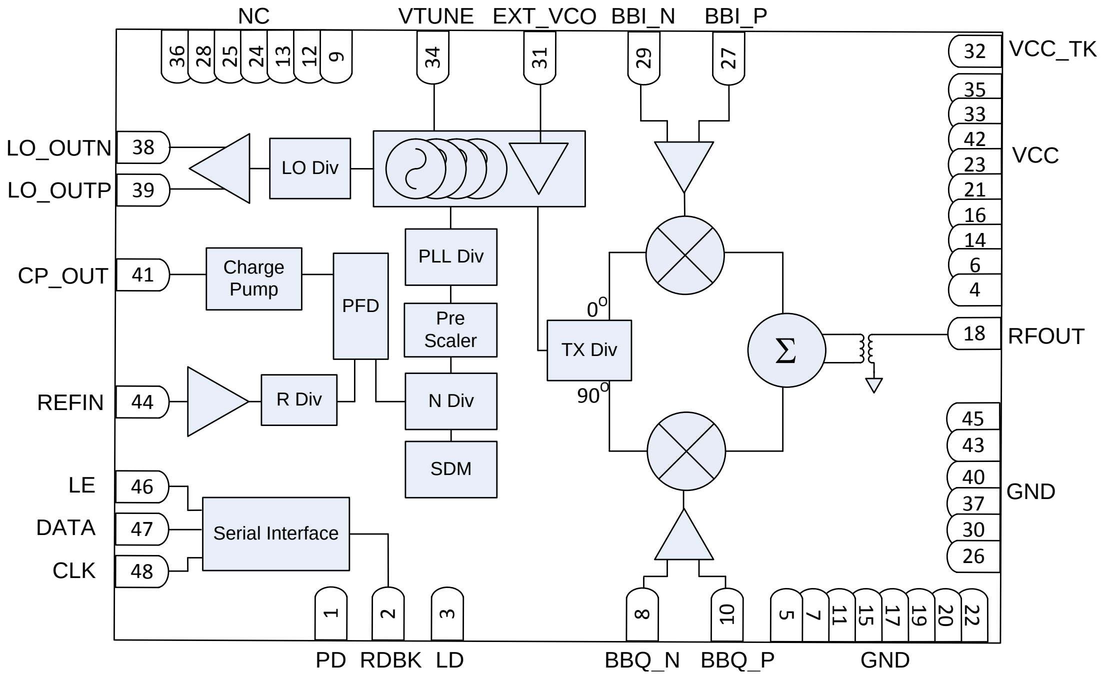
The TRF3722 is a high performance direct conversion quadrature modulator with exceptional linearity and low noise performance. The typical 0.25-V baseband common mode voltage supports seamless interface with current source DACs. The device integrates the PLL and VCO to provide the local oscillator (LO) to the modulator. The PLL and VCO provides excellent phase noise performance to satisfy the most stringent transmit communication requirements. The device also provides additional LO output for driving a second modulator or down converting mixer. The modulator features a high gain mode for a typical 3-dB gain increase and a low power mode when power optimization is desired.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRF3722	VQFN (48)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram



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4 Revision History

Changes from Revision A (June 2014) to Revision B — Page

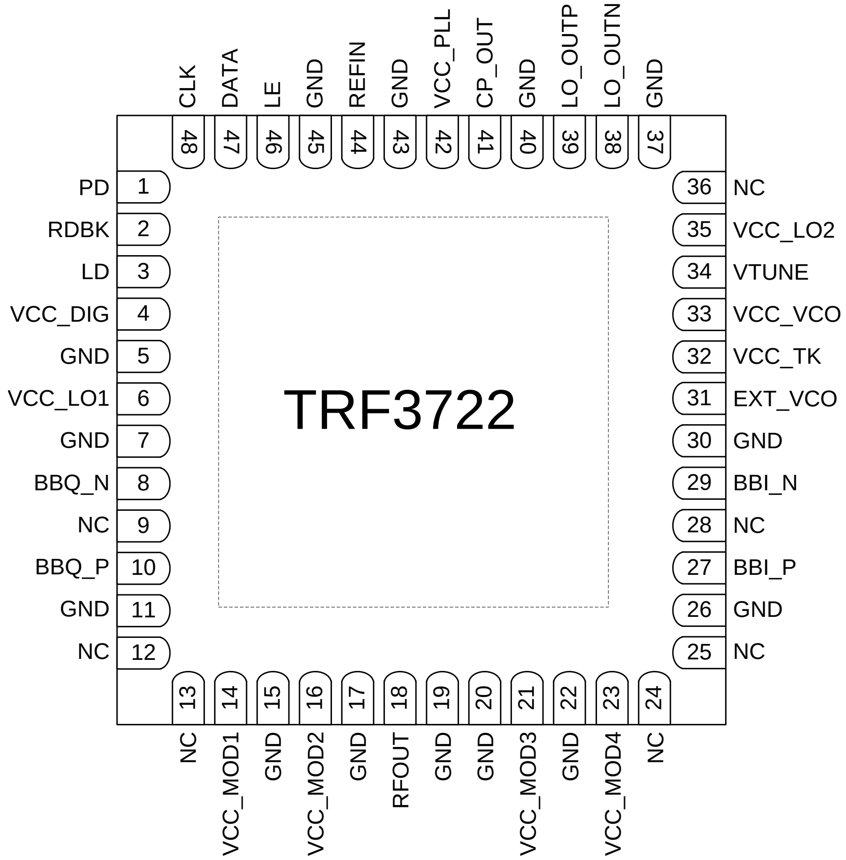
- Changed *256 MHz* to *280 MHz* in *PLL and VCO* Features bullet 1
- Changed *ESD Ratings* table title, updated to current standards 4
- Added *Typical* and footnote 2 to *Typical VCO frequency range* and *Typical output frequency range* parameters 8
- Changed Figure 1 9
- Changed location of *TRF3722 Application Schematic* figure and all associated text to be under *Typical Application* section 55

Changes from Original (May 2014) to Revision A — Page

- Changed from 1-page Product Preview to Production 1

5 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BBI_N	29	I	BB in-phase input: negative
BBI_P	27	I	BB in-phase input: positive
BBQ_N	8	I	BB quadrature input: negative
BBQ_P	10	I	BB quadrature input: positive
CLK	48	I	Serial interface clock input; digital input
CP_OUT	41	O	Charge pump output
DATA	47	I	Serial interface data input; digital input
EXT_VCO	31	I	External local oscillator input
GND	5, 7, 11, 15, 17, 19, 20, 22, 26, 30, 37, 40, 43, 45		Ground
LD	3	O	PLL lock detect output
LE	46	I	Serial interface latch enable; digital input
LO_OUTN	38	O	Local oscillator output: negative
LO_OUTP	39	O	Local oscillator output: positive
NC	9, 12, 13, 24, 25, 36		No connect
NC	28		No connect; N/C or ground to paddle

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PD	1	I	LO Div, TX Div, modulator power down (High = PD)
RDBK	2	O	Serial interface internal registers readback output
REFIN	44	I	Reference clock input
RFOUT	18	O	RF output
VCC_DIG	4		3.3 V digital power supply
VCC_LO1	6		3.3 V TX Div power supply
VCC_LO2	35		3.3 V LO Div power supply
VCC_MOD1	14		3.3 V modulator power supply
VCC_MOD2	16		3.3 V modulator power supply
VCC_MOD3	21		3.3 V modulator power supply
VCC_MOD4	23		3.3 V modulator power supply
VCC_PLL	42		3.3 V PLL power supply
VCC_TK	32		3.3 V or 5 V VCO tank power supply
VCC_VCO	33		3.3 V VCO power supply
VTUNE	34	I	VCO control voltage input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	All VCC except VCC_TK	–0.3	+3.6	V
	VCC_TK	–0.3	+5.5	
Digital I/O voltage		–0.3	3.6	V
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	3.3 V power-supply voltage	3	3.3	3.6	V
	5 V or 3.3 V power-supply voltage, VCC _TK	3	3.3/5	5.5	V
T_J	Operating junction temperature range	–40		125	°C
T_A	Ambient temperature range	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TRF3722 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended operating conditions: VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C. Optimized bias settings as per Table 16.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PARAMETERS						
I_{CC}	3.3 V Supply Current	Typical Operating Mode; LO out = Off		328(1)		mA
		Typical Operating Mode; LO out = On		374		mA
I_{CC_TK}	5 V Supply Current			21		mA
P_{DISS}	Total Power Dissipation	Typical Operating Mode; LO out = Off		1.18		W
		Typical Operating Mode; LO out = On		1.34		W
		Low Power Mode (Mod); LO out = Off		0.91		W
I_{PD}	Power Down Current	Hardware Power Down		76		mA
		Serial interface Power Down		2		mA
RFOUT FREQUENCY						
	Frequency		400		4200	MHz
IQ MODULATOR f_{LO} = 750 MHz						
G	Gain	Typical Operating Mode		0.8		dB
		High Gain Mode		3.6		dB
	Gain Flatness	In 300MHz bandwidth	–0.5		0.5	dB
OP1dB	Output Compression Point			10.2		dBm
OIP3	Output 3rd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		31		dBm
OIP2	Output 2nd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		62		dBm
SBS	Unadj. SideBand Suppression			–42		dBc
CF	Unadj. Carrier Feedthrough			–50		dBm
NSD_O	Output Noise Spectral Density	BB inputs terminated on 50 Ω		–159		dBm/Hz
$HD2_{LO}$	LO Second Harmonic	Measured at 2 x f_{LO}		–49		dBc
$HD3_{LO}$	LO Third Harmonic	Measured at 3 x f_{LO}		–47		dBc
$HD2_{BB}$	Baseband Second Harmonic	Measured at f_{LO} ± 2 x f_{BB}		–72		dBc
$HD3_{BB}$	Baseband Third Harmonic	Measured at f_{LO} ± 3 x f_{BB}		–70		dBc

(1) Powered down output buffer and LO divider.

Electrical Characteristics (continued)

Over recommended operating conditions: VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C. Optimized bias settings as per Table 16.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IQ MODULATOR f_{LO} = 900 MHz						
G	Gain	Typical Operating Mode		0.8		dB
		High Gain Mode		3.6		dB
	Gain Flatness	In 300MHz bandwidth	–0.5		0.5	dB
OP1dB	Output Compression Point			10		dBm
OIP3	Output 3rd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		31		dBm
OIP2	Output 2nd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		62.5		dBm
SBS	Unadj. Side Band Suppression			–42.5		dBc
CF	Unadj. Carrier Feed through			–50		dBm
NSD_O	Output Noise Spectral Density	BB inputs terminated on 50 Ω		–159		dBm/Hz
$HD2_{LO}$	LO Second Harmonic	Measured at 2 x f_{LO}		–47		dBc
$HD3_{LO}$	LO Third Harmonic	Measured at 3 x f_{LO}		–54.5		dBc
$HD2_{BB}$	Baseband Second Harmonic	Measured at f_{LO} ± 2 x f_{BB}		–65.5		dBc
$HD3_{BB}$	Baseband Third Harmonic	Measured at f_{LO} ± 3 x f_{BB}		–71.5		dBc
IQ MODULATOR f_{LO} = 1800 MHz						
G	Gain	Typical Operating Mode		0.3		dB
		High Gain Mode		3		dB
	Gain Flatness	In 300 MHz bandwidth	–0.5		0.5	dB
OP1dB	Output Compression Point			13		dBm
OIP3	Output 3rd Order Intercept Point	f_{BB} = 4.5, 5.5 MHz		29.5		dBm
OIP2	Output 2nd Order Intercept Point	f_{BB} = 4.5, 5.5 MHz		57		dBm
SBS	Unadj. Side Band Suppression			–54.5		dBc
CF	Unadj. Carrier Feed through			–57		dBm
NSD_O	Output Noise Spectral Density	BB inputs terminated on 50 Ω		–158		dBm/Hz
$HD2_{LO}$	LO Second Harmonic	Measured at 2 x f_{LO}		–36.5		dBc
$HD3_{LO}$	LO Third Harmonic	Measured at 3 x f_{LO}		–33.5		dBc
$HD2_{BB}$	Baseband Second Harmonic	Measured at f_{LO} ± 2 x f_{BB}		–65.5		dBc
$HD3_{BB}$	Baseband Third Harmonic	Measured at f_{LO} ± 3 x f_{BB}		–73		dBc
RL_O	RF Output Return Loss			6		dB
IQ MODULATOR f_{LO} = 2150 MHz						
G	Gain	Typical Operating Mode		0.2		dB
		High Gain Mode		3		dB
	Gain Flatness	In 300 MHz bandwidth	–0.5		0.5	dB
OP1dB	Output Compression Point			11.6		dBm
OIP3	Output 3rd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		30		dBm
OIP2	Output 2nd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		43		dBm
SBS	Unadj. Side Band Suppression			–43		dBc
CF	Unadj. Carrier Feedt hrough			–42		dBm
NSD_O	Output Noise Spectral Density	BB inputs terminated on 50 Ω		–157		dBm/Hz
$HD2_{LO}$	LO Second Harmonic	Measured at 2 x f_{LO}		–40		dBc
$HD3_{LO}$	LO Third Harmonic	Measured at 3 x f_{LO}		–31		dBc
$HD2_{BB}$	Baseband Second Harmonic	Measured at f_{LO} ± 2 x f_{BB}		–51		dBc
$HD3_{BB}$	Baseband Third Harmonic	Measured at f_{LO} ± 3 x f_{BB}		–69		dBc

Electrical Characteristics (continued)

Over recommended operating conditions: VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C. Optimized bias settings as per Table 16.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IQ MODULATOR f_{LO} = 2700 MHz						
G	Gain	Typical Operating Mode		0		dB
		High Gain Mode		2.4		dB
	Gain Flatness	In 300MHz bandwidth	–0.5		0.5	dB
OP1dB	Output Compression Point			10.4		dBm
OIP3	Output 3rd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		29.5		dBm
OIP2	Output 2nd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		45.5		dBm
SBS	Unadj. Side Band Suppression			–33		dBc
CF	Unadj. Carrier Feed through			–39.6		dBm
NSD_O	Output Noise Spectral Density	BB inputs terminated on 50 Ω		–156		dBm/Hz
$HD2_{LO}$	LO Second Harmonic	Measured at 2 x f_{LO}		–29		dBc
$HD3_{LO}$	LO Third Harmonic	Measured at 3 x f_{LO}		–37		dBc
$HD2_{BB}$	Baseband Second Harmonic	Measured at f_{LO} ± 2 x f_{BB}		–53		dBc
$HD3_{BB}$	Baseband Third Harmonic	Measured at f_{LO} ± 3 x f_{BB}		–68		dBc
IQ MODULATOR f_{LO} = 3600 MHz						
G	Gain	Typical Operating Mode		–2		dB
		High Gain Mode		0.4		dB
OP1dB	Output Compression Point			8.7		dBm
OIP3	Output 3rd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		24.5		dBm
OIP2	Output 2nd Order Intercept Point	F_{BB} = 4.5, 5.5 MHz		45.5		dBm
SBS	Unadj. Side Band Suppression			–31.5		dBc
CF	Unadj. Carrier Feed through			–39.5		dBm
$HD2_{LO}$	LO Second Harmonic	Measured at 2 x f_{LO}		–28.4		dBc
$HD3_{LO}$	LO Third Harmonic	Measured at 3 x f_{LO}		–31.5		dBc
$HD2_{BB}$	Baseband Second Harmonic	Measured at f_{LO} ± 2 x f_{BB}		–55		dBc
$HD3_{BB}$	Baseband Third Harmonic	Measured at f_{LO} ± 3 x f_{BB}		–65		dBc
BASEBAND INPUTS						
V_{CM}	Common Mode Voltage	Baseband I/Q input	0	0.25	0.5	V
BW_{BB}	Baseband Bandwidth	1 dB Bandwidth		900		MHz
Zin_{BB}	Baseband Input Impedance	Resistance		5		kΩ
		Capacitance		4		pF
REFERENCE OSCILLATOR PARAMETERS						
F_{ref}	Reference Frequency	Max		350		MHz
	Reference Input Sensitivity		0.2		3.3	V_{PP}
Zin_{ref}	Reference Input Impedance	Parallel capacitance		2		pF
		Parallel resistance		2.2		kΩ
PFD, CP						
F_{PFD}	PFD Frequency	Max, refer to the *Typical Application*			65	MHz
I_{CP_OUT}	Charge Pump Current	Max		1.94		mA
	In-band Normalized PN Floor	Integer Mode		–221		dBc/Hz

Electrical Characteristics (continued)

Over recommended operating conditions: VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C. Optimized bias settings as per Table 16.

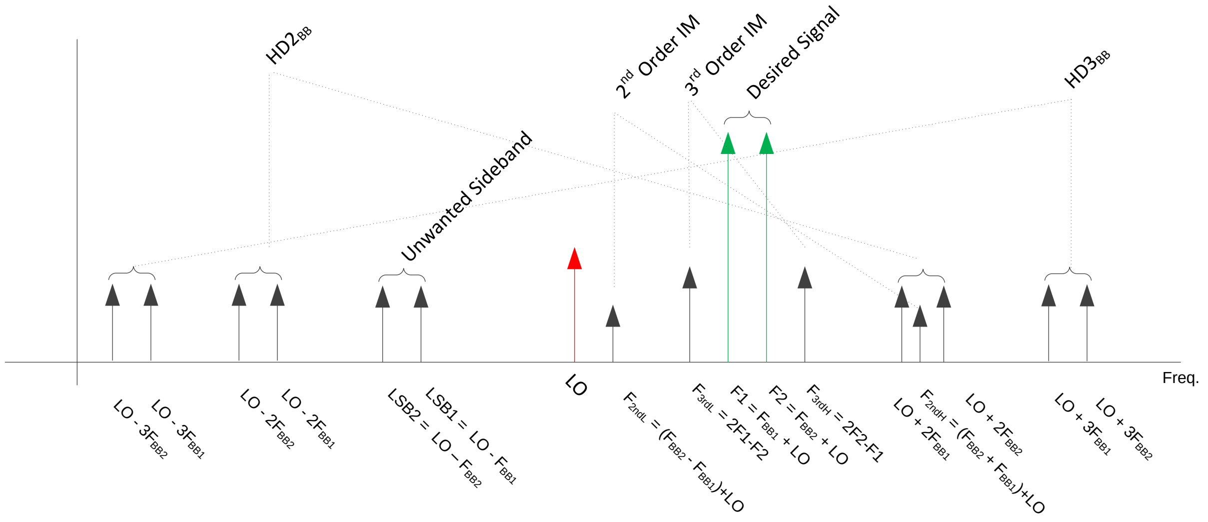
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCO						
f_{VCO}	Typical VCO frequency range[2]		2050		4100	MHz
K_V	VCO gain	VTUNE = 1.1 V		30		MHz/V
PN	VCO Open Loop Phase Noise; f_{VCO} = 3600 MHz; TX Div = Div-by-1; f_{OUT} = 3600 MHz VTUNE = 1.1 V	10 kHz		–74		dBc/Hz
		100 kHz		–109		
		1 MHz		–135		
		10 MHz		–152		
		40 MHz		–156		
	VCO Open Loop Phase Noise; f_{VCO} = 3600 MHz; TX Div = Div-by-2; f_{OUT} = 1800 MHz; VTUNE = 1.1 V	10 kHz		–80		dBc/Hz
		100 kHz		–115		
		1 MHz		–141		
		10 MHz		–156		
		40 MHz		–158		
LO OUTPUT						
f_{OUT}	Typical output frequency range[2]	Divide by 1	2050		4100	MHz
		Divide by 2	1025		2050	
		Divide by 4	512.5		1025	
		Divide by 8	256.25		512.5	
P_{LO}	Output power	SE at 1800 MHz, OUTBUF_BIAS = 2		1		dBm
	External VCO input Frequency Range		250		4200	MHz
	External VCO Input Level		–10	0	10	dBm
CLOSE LOOP PLL OR VCO						
	Integrated Phase Noise	Frac-N; PFD = 15.36 MHz; f_{OUT} = 3532.89 MHz; Integration BW =1 kHz to 10 MHz; SSB		-45.2		dB
		Int-N; PFD = 2.56 MHz; f_{OUT} = 1799.68 MHz; Integration BW = 500 Hz to 20 MHz; SSB		-49.8		dB
	VCO Close Loop Phase Noise; f_{VCO} = 3600 MHz; TX DIV = Div-by-2; f_{OUT} = 1800 MHz; Integer Mode, PFD = 2.56MHz	10 kHz		–96		dBc/Hz
		100 kHz		–114		
		1 MHz		–140		
		10 MHz		–156		
		40 MHz		–158		
DIGITAL INTERFACE						
V_{IH}	High Level Input Voltage		2	3.3		V
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{OH}	High Level Output Voltage	Referenced to VCC_DIG	0.8 x VCC			V
V_{OL}	Low Level Output Voltage	Referenced to VCC_DIG			0.2 x VCC	V

(2) Divided-down ranges minimum and maximum values are typical but are not specified.

6.6 Typical Characteristics

6.6.1 Modulator Output Spectrum

Graphical illustration of the modulator output spectrum with two tones is shown in Figure 1.



F_{BBn} = Baseband Frequency
Fn = RF Frequency
$F_{3rdH/L}$ = 3^{rd} Order Intermodulation Product Frequency (High Side / Low Side)
$F_{2ndH/L}$ = 2^{nd} Order Intermodulation Product Frequency (High Side / Low Side)
LO = Local Oscillator Frequency
LSBn = Lower Sideband Frequency
$HD2_{BB}$ = Baseband second harmonic (High Side / Low Side)
$HD3_{BB}$ = Baseband thrid harmonic (High Side / Low Side)

Figure 1. Graphical Illustration of Modulator Output Spectrum

6.7 Typical Characteristics - Output Power

Unless specified all plots were created using TRF3722EVM, V_{CC} = 3.3 V, VCC_TK = 5 V, T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, 500 mV_{PP}, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16. Total P_{out} is two tones combined power.

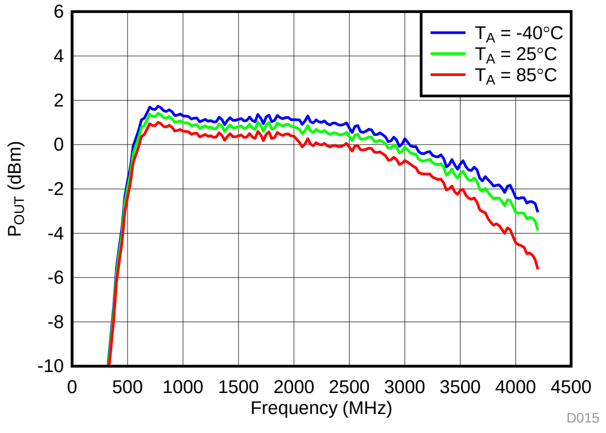


Figure 2. Total P_{OUT} vs Temperature, Typical Operating Mode

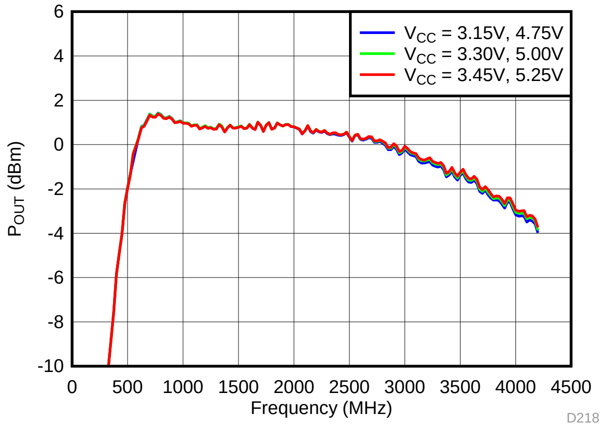


Figure 3. Total P_{OUT} vs Supply, Typical Operating Mode

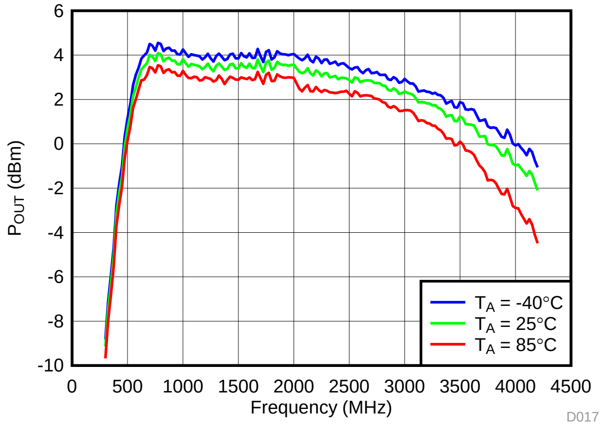


Figure 4. Total P_{OUT} vs Temperature, High Gain Mode

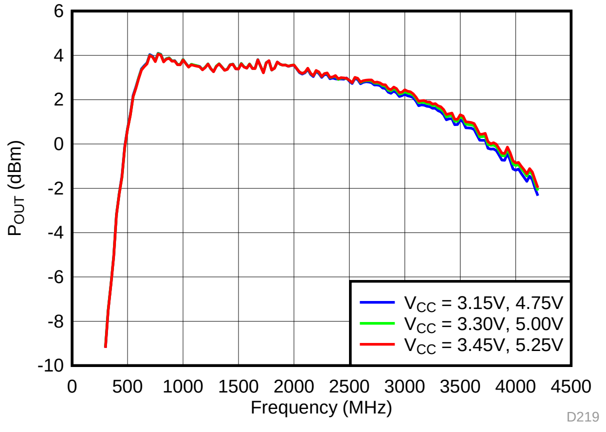


Figure 5. Total P_{OUT} vs Supply, High Gain Mode

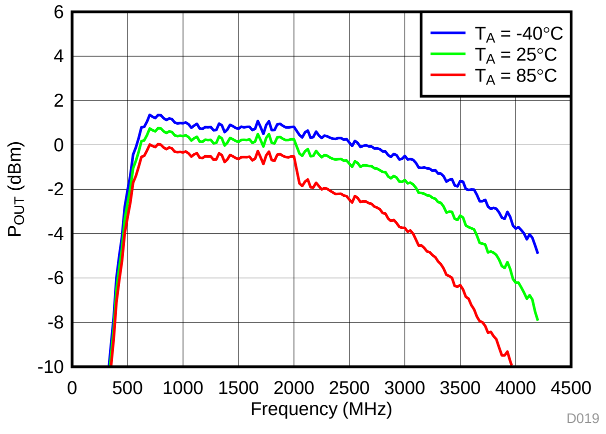


Figure 6. Total P_{OUT} vs Temperature, Low Power Mode

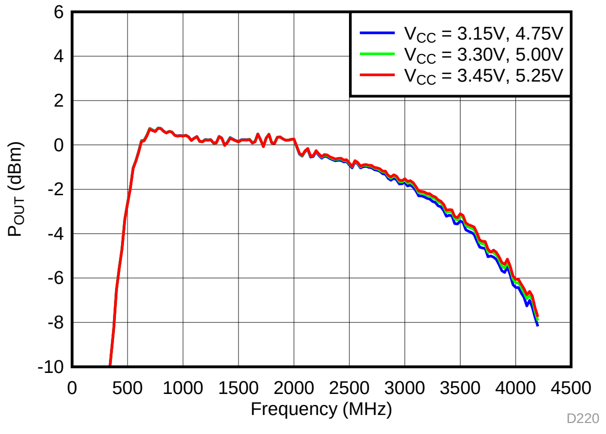


Figure 7. Total P_{OUT} vs Supply, Low Power Mode

6.8 Typical Characteristics - Gain

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16.

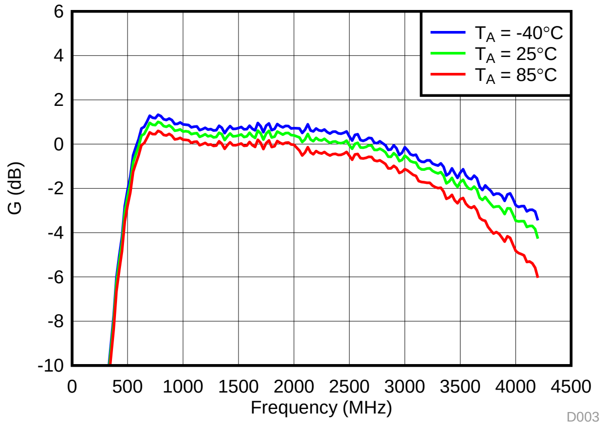


Figure 8. Voltage Gain vs Temperature, Typical Operating Mode

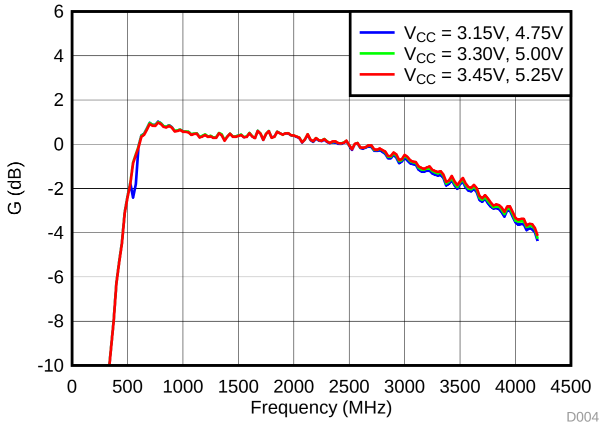


Figure 9. Voltage Gain vs Supply, Typical Operating Mode

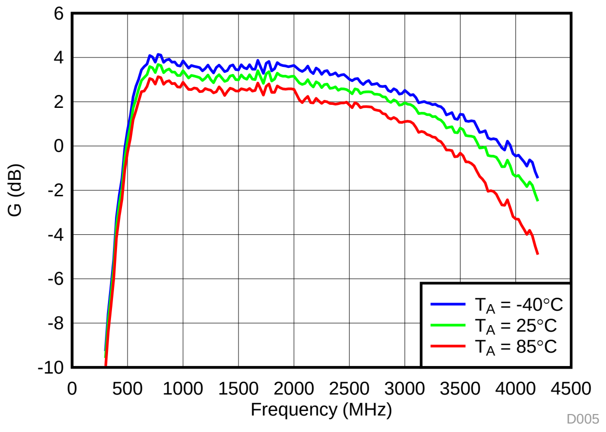


Figure 10. Voltage Gain vs Temperature, High Gain Mode

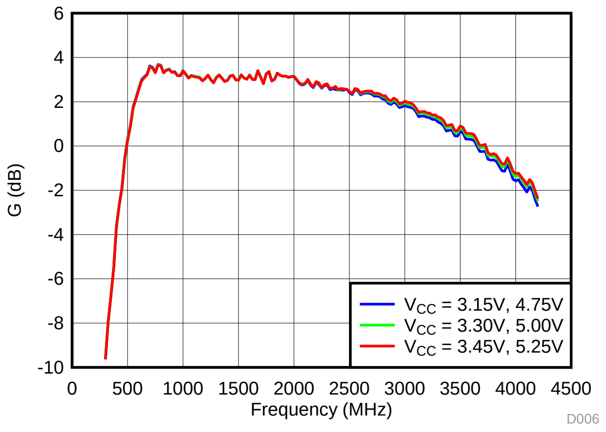


Figure 11. Voltage Gain vs Supply, High Gain Mode

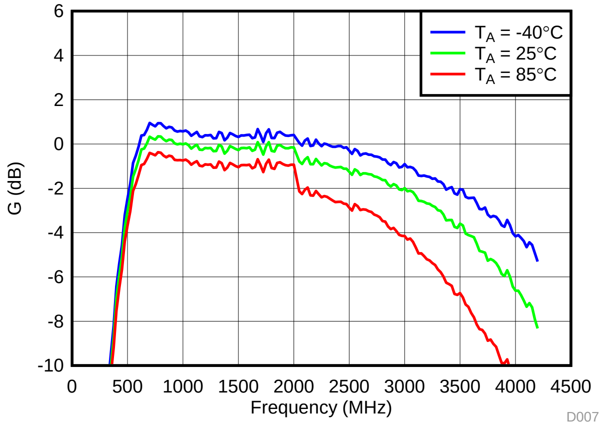


Figure 12. Voltage Gain vs Temperature, Low Power Mode

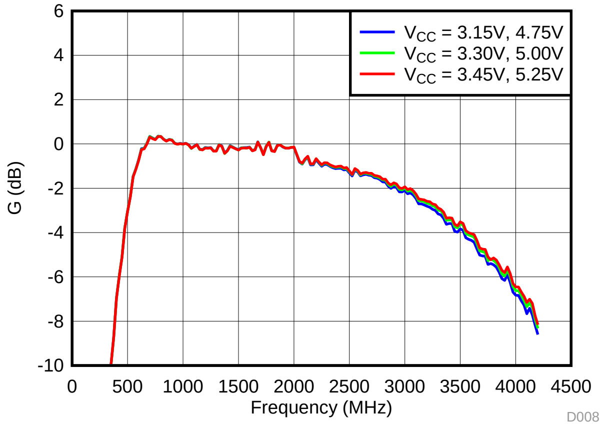


Figure 13. Voltage Gain vs Supply, Low Power Mode

6.9 Typical Characteristics - OIP3

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16. Reported OIP3 is minimum of low side and high side.

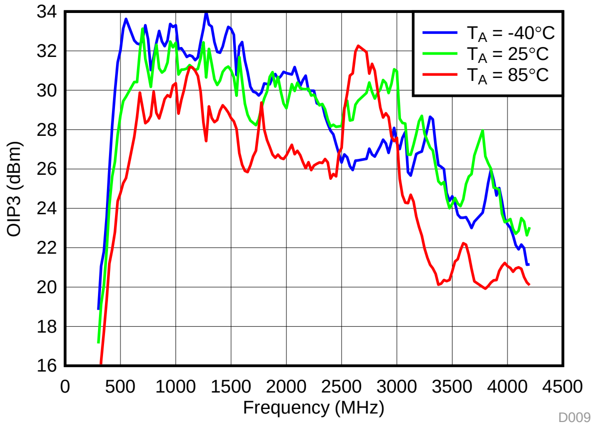


Figure 14. OIP3 vs Temperature, Typical Operating Mode

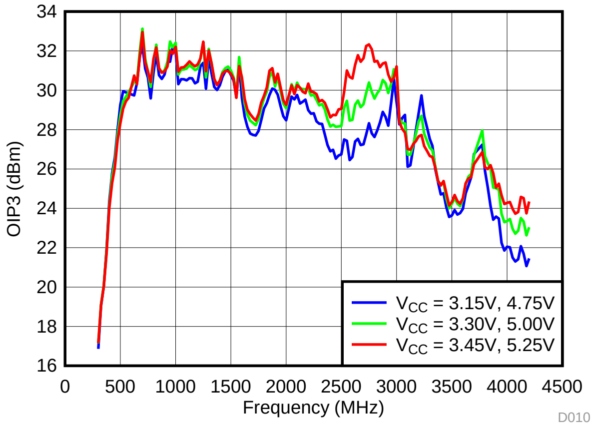


Figure 15. OIP3 vs Supply, Typical Operating Mode

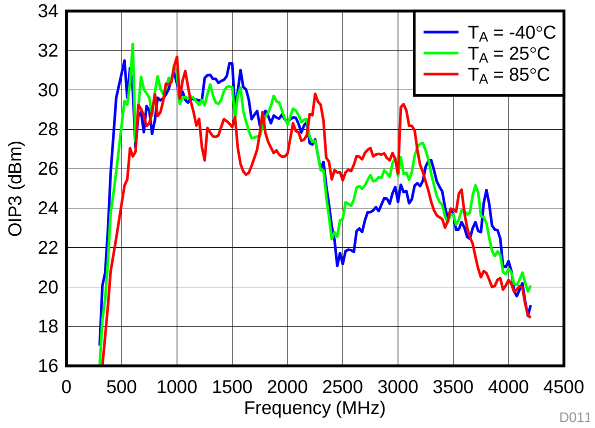


Figure 16. OIP3 vs Temperature, High Gain Mode

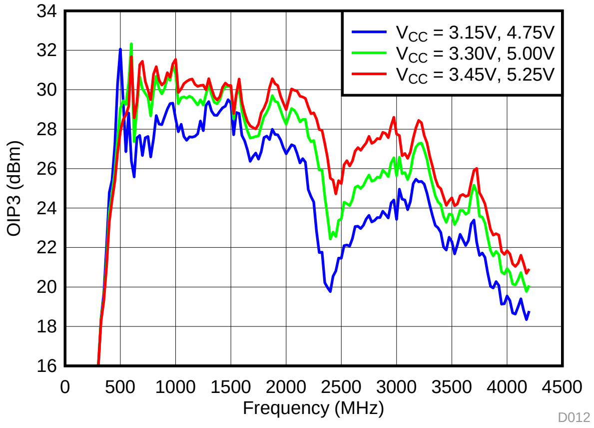


Figure 17. OIP3 vs Supply, High Gain Mode

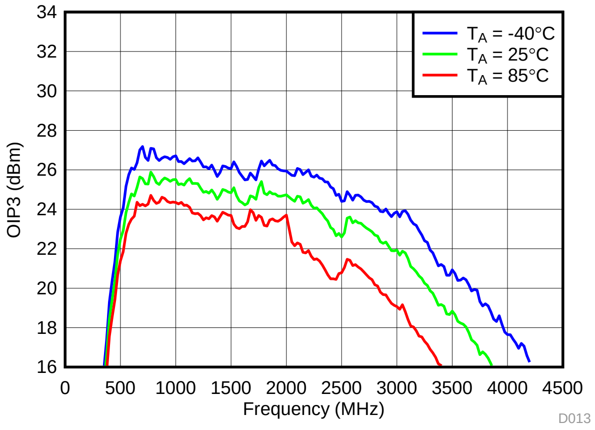


Figure 18. OIP3 vs Temperature, Low Power Mode

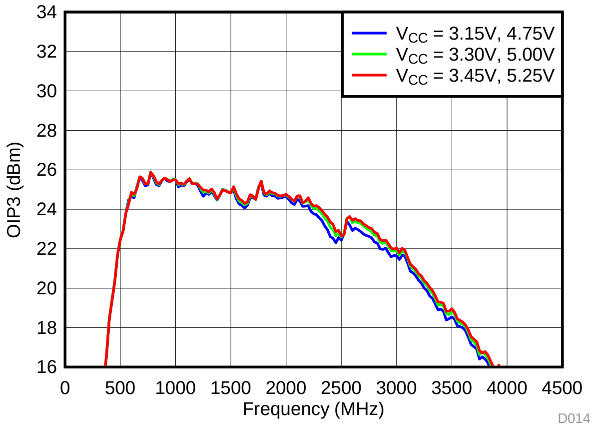


Figure 19. OIP3 vs Supply, Low Power Mode

6.10 Typical Characteristics - OIP2

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16. Reported OIP2 is minimum of low side and high side.

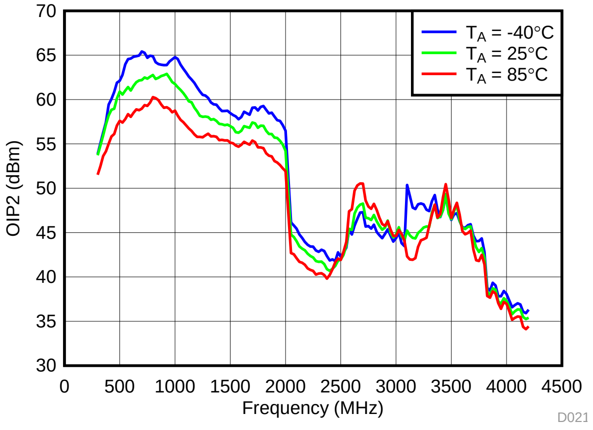


Figure 20. OIP2 vs Temperature, Typical Operating Mode

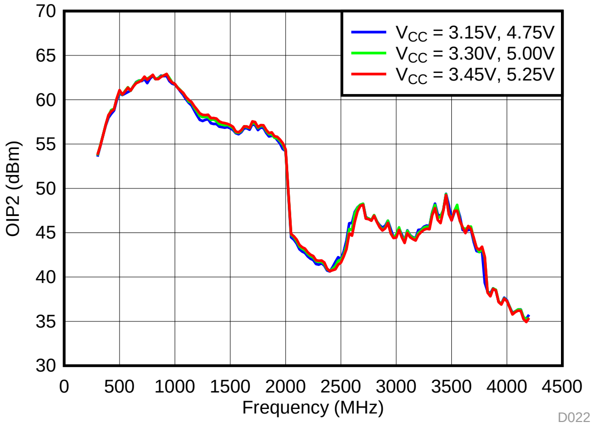


Figure 21. OIP2 vs Supply, Typical Operating Mode

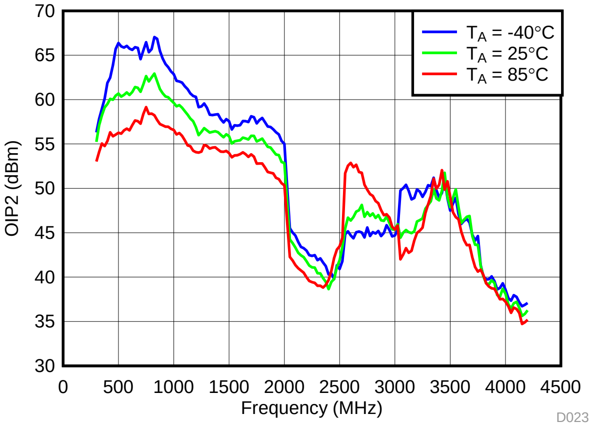


Figure 22. OIP2 vs Temperature, High Gain Mode

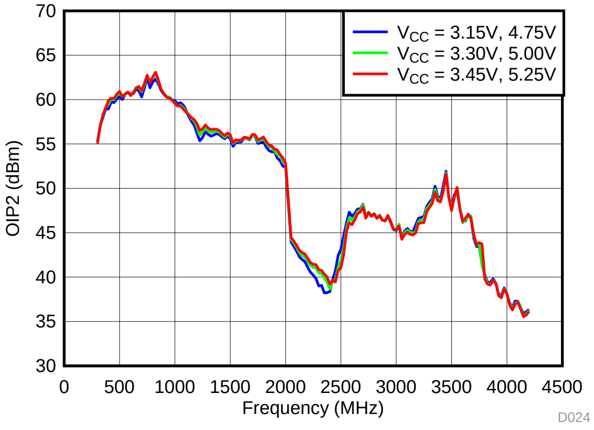


Figure 23. OIP2 vs Supply, High Gain Mode

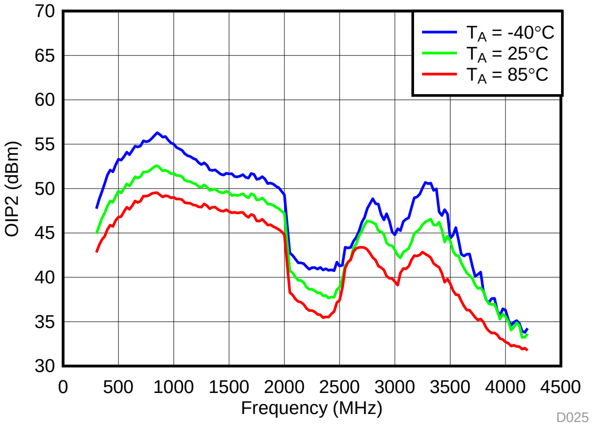


Figure 24. OIP2 vs Temperature, Low Power Mode

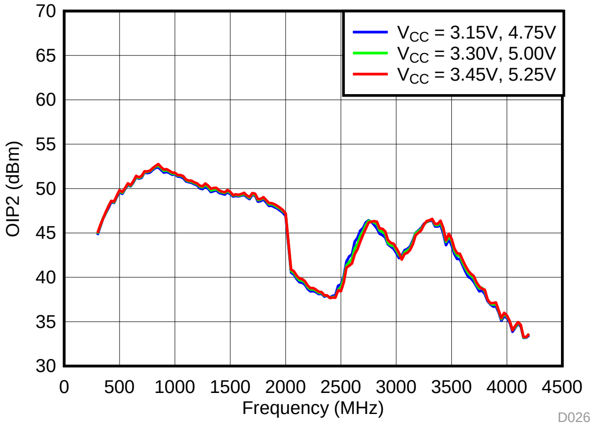


Figure 25. OIP2 vs Supply, Low Power Mode

6.11 Typical Characteristics - OP1dB

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C, I/Q frequency (f_{BB}) 5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16.

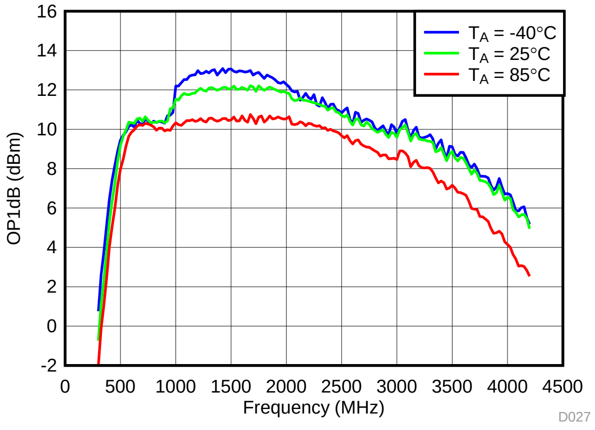


Figure 26. OP1dB vs Temperature, Typical Operating Mode

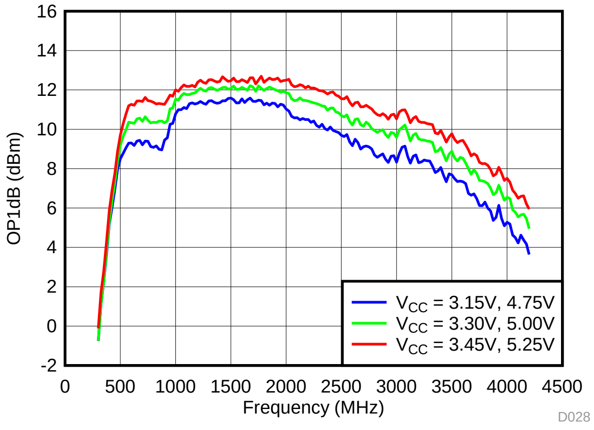


Figure 27. OP1dB vs Supply, Typical Operating Mode

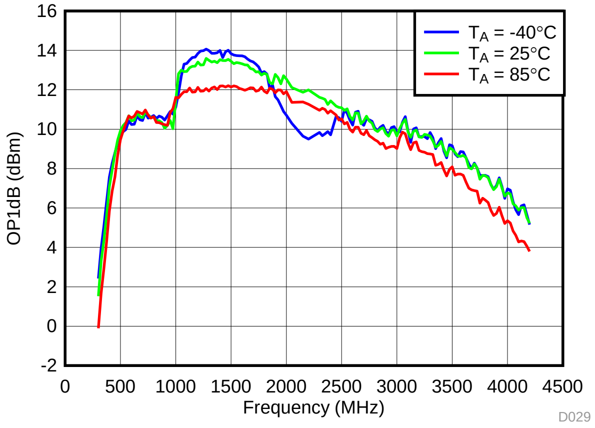


Figure 28. OP1dB vs Temperature, High Gain Mode

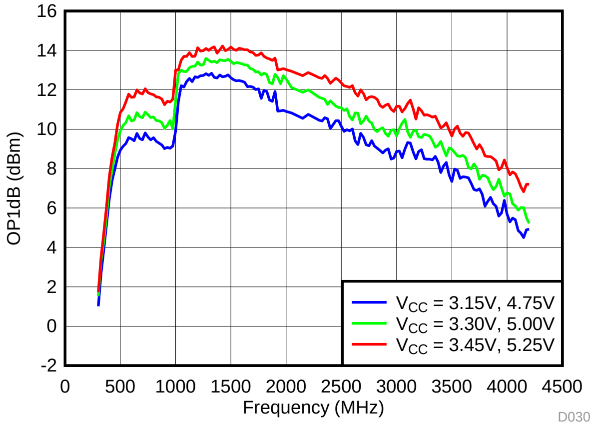


Figure 29. OP1dB vs Supply, High Gain Mod

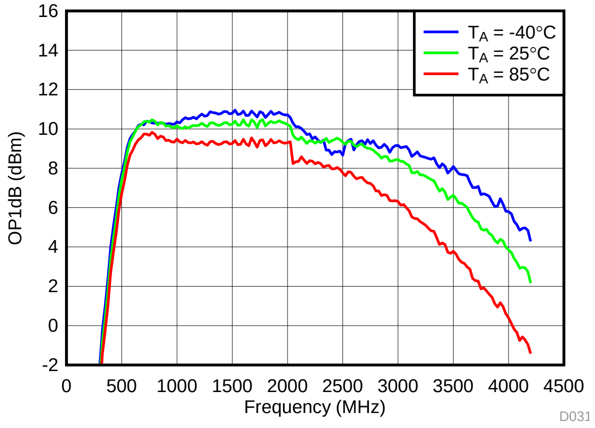


Figure 30. OP1dB vs Temperature, Low Power Mode

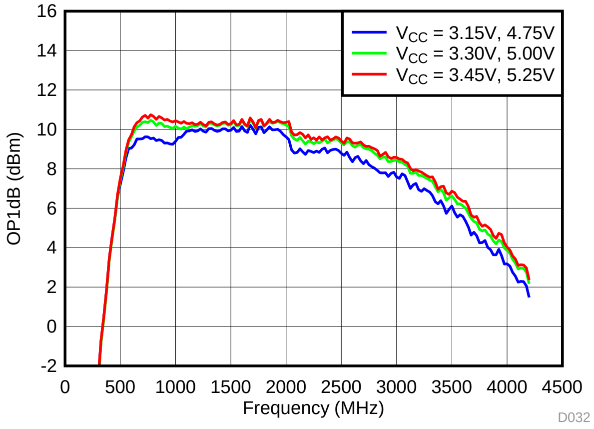


Figure 31. OP1dB vs Supply, Low Power Mode

6.12 Typical Characteristics - Noise

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, T_A = 25°C, BB inputs terminated to 50 Ω and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16.

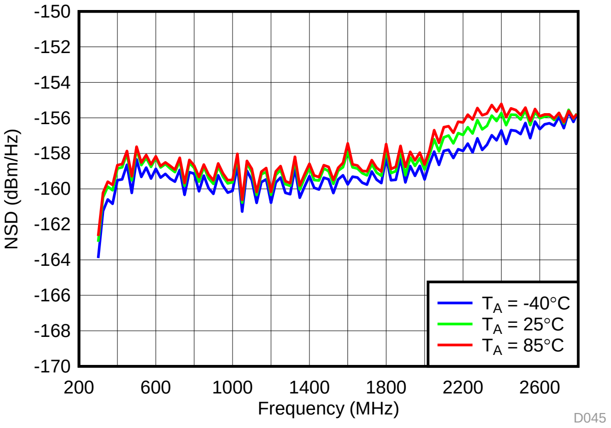


Figure 32. Noise vs Temperature, Typical Operating Mode

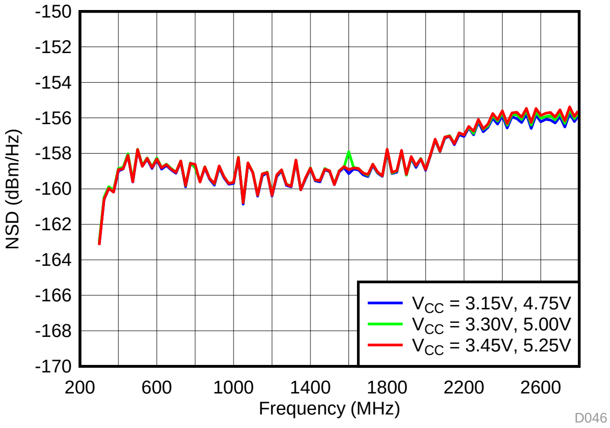


Figure 33. Noise vs Supply, Typical Operating Mode

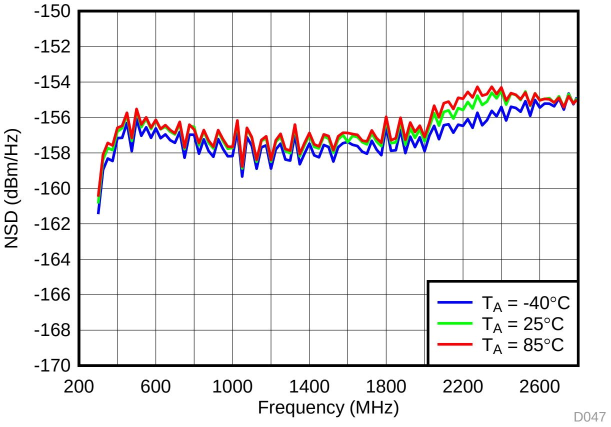


Figure 34. Noise vs Temperature, High Gain Mode

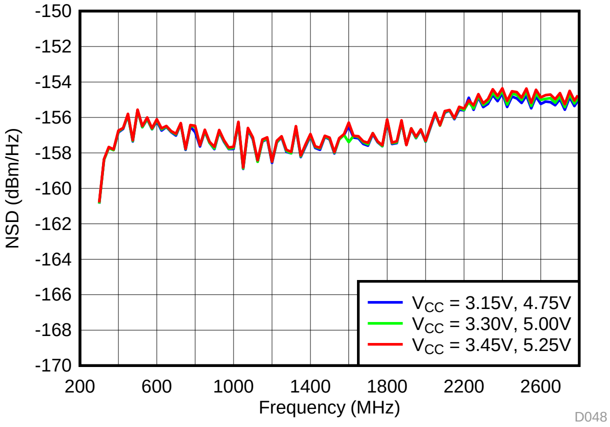


Figure 35. Noise vs Supply, High Gain Mode

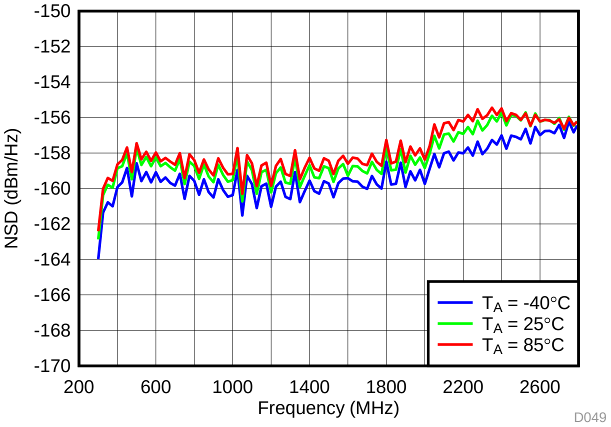


Figure 36. Noise vs Temperature, Low Power Mode

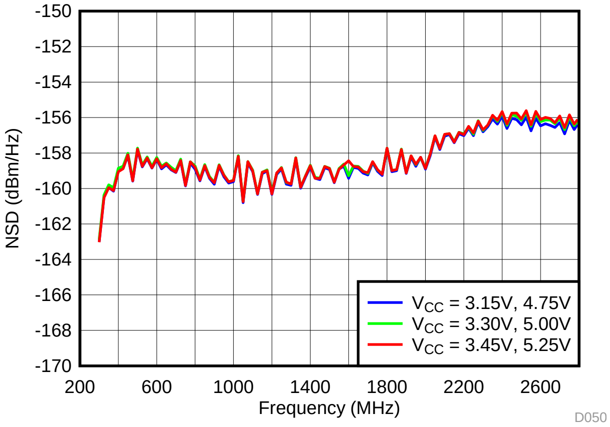


Figure 37. Noise vs Supply, Low Power Mode

6.13 Typical Characteristics - Unadjusted CF

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK= 5 V, T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16.

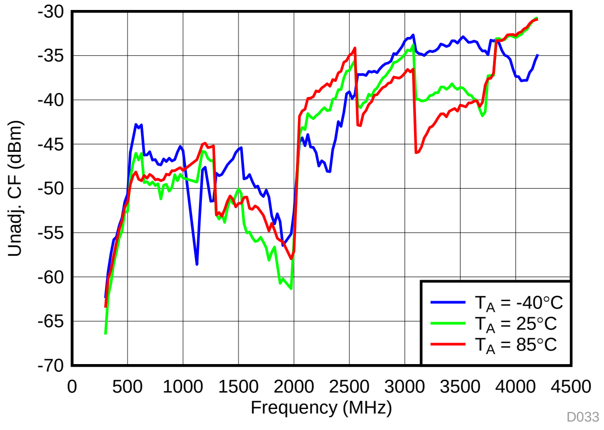


Figure 38. Unadjustable CF vs Temperature, Typical Operating Mode

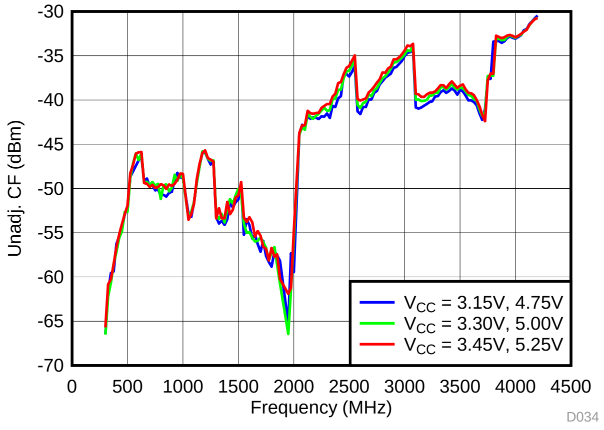


Figure 39. Unadjustable CF vs Supply, Typical Operating Mode

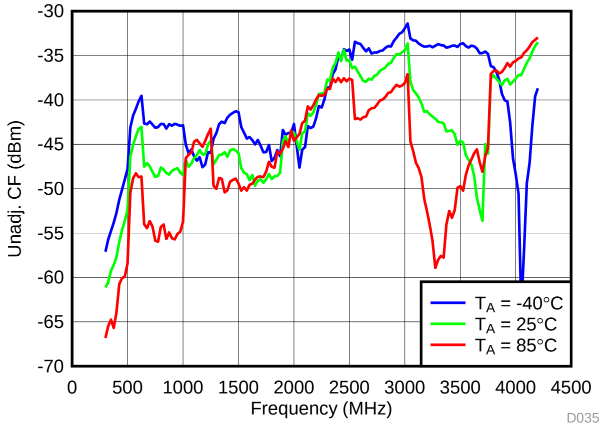


Figure 40. Unadjustable CF vs Temperature, High Gain Mode

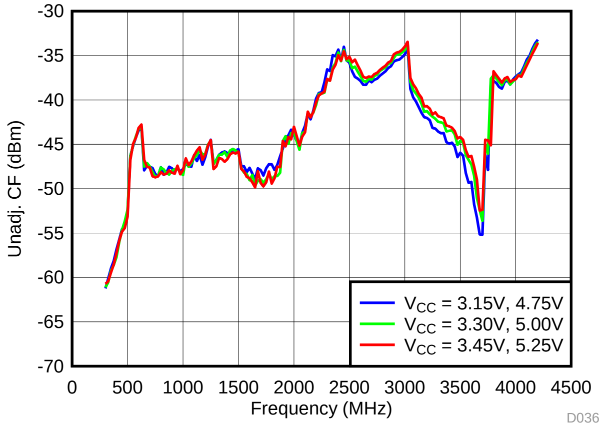


Figure 41. Unadjustable CF vs Supply, High Gain Mode

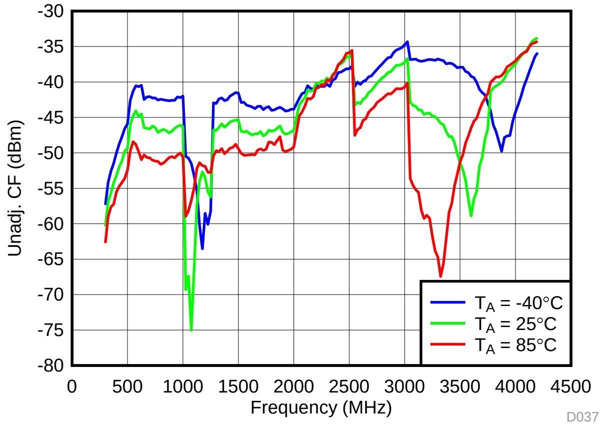


Figure 42. Unadjustable CF vs Temperature, Low Power Mode

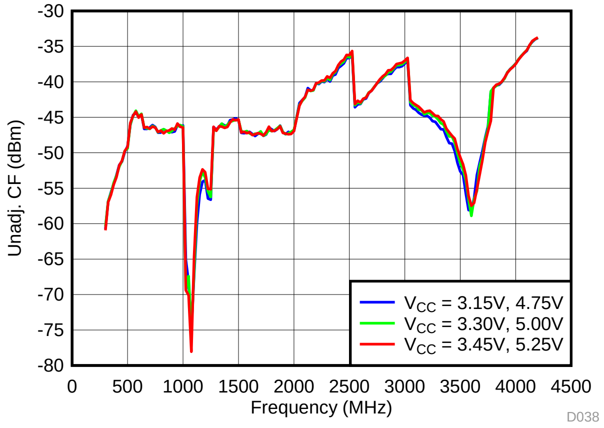


Figure 43. Unadjustable CF vs Supply, Low Power Mode

6.14 Typical Characteristics - Unadjusted SBS

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK= 5 V, and T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16.

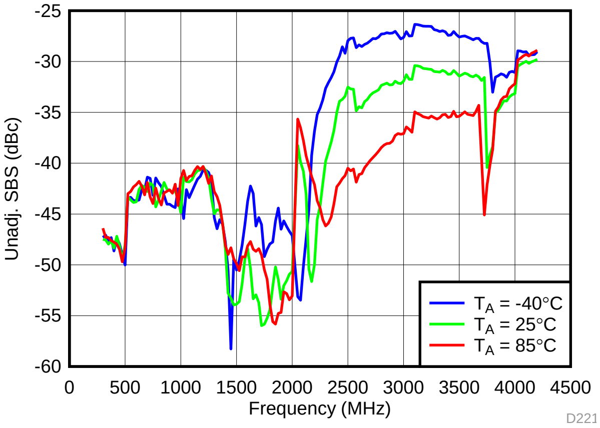


Figure 44. Unadjustable SBS vs Temperature, Typical Operating Mode

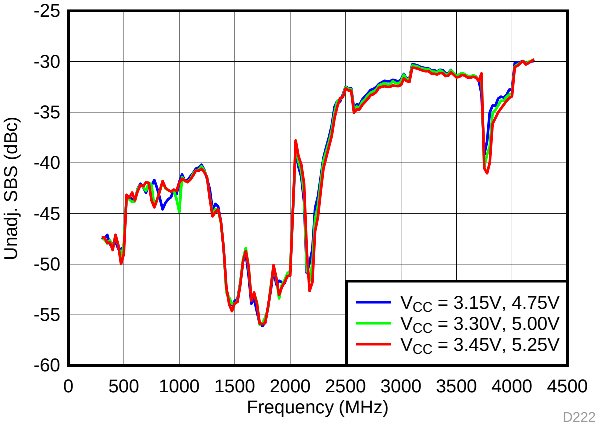


Figure 45. Unadjustable SBS vs Supply, Typical Operating Mode

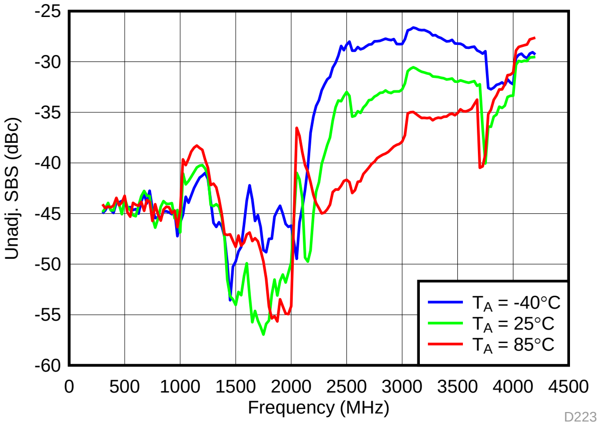


Figure 46. Unadjustable SBS vs Temperature, High Gain Mode

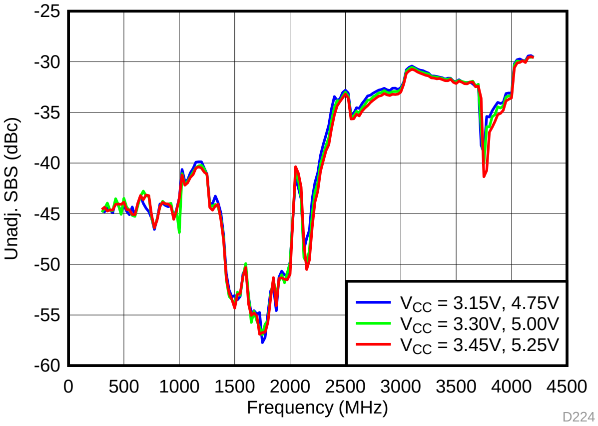


Figure 47. Unadjustable SBS vs Supply, High Gain Mode

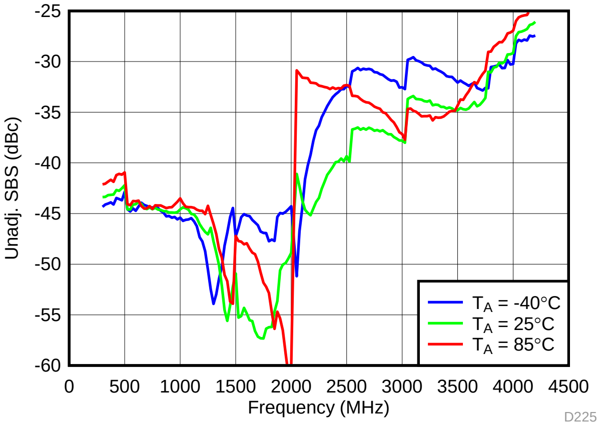


Figure 48. Unadjustable SBS vs Temperature, Low Power Mode

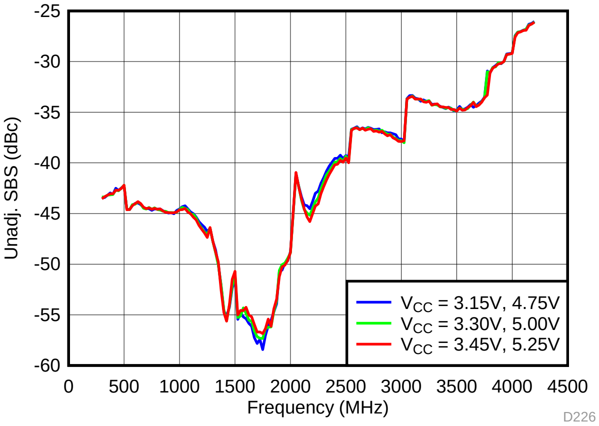


Figure 49. Unadjustable SBS vs Supply, Low Power Mode

6.15 Typical Characteristics - LO Harmonic

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16.

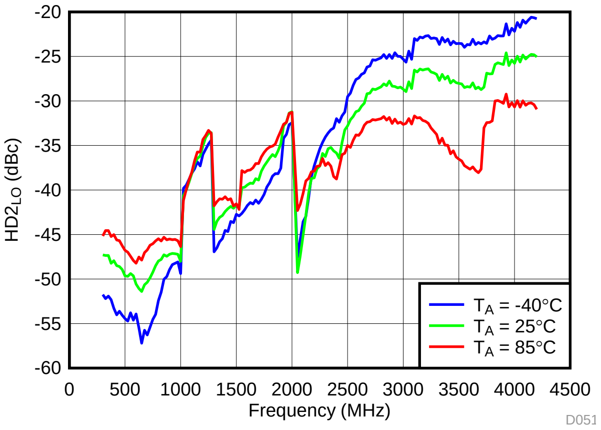


Figure 50. LO Second Harmonic vs Temperature, Typical Operating Mode

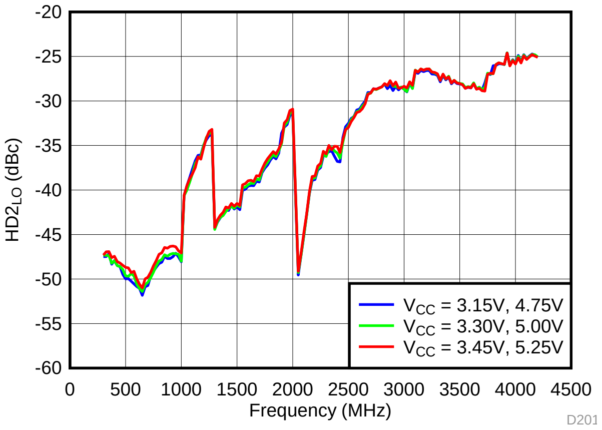


Figure 51. LO Second Harmonic vs Supply, Typical Operating Mode

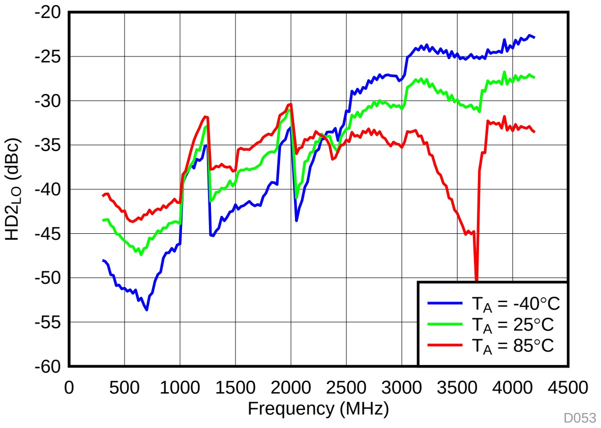


Figure 52. LO Second Harmonic vs Temperature, High Gain Mode

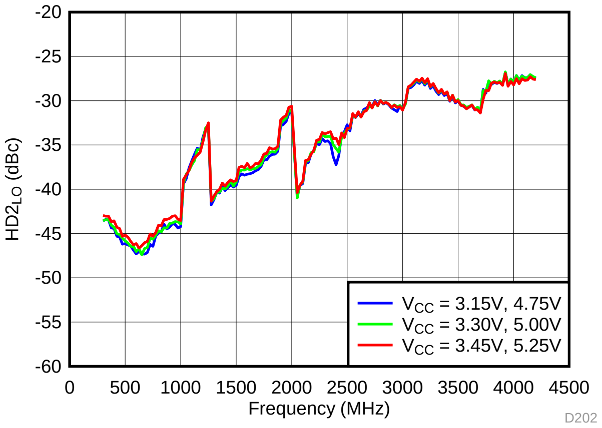


Figure 53. LO Second Harmonic vs Supply, High Gain Mode

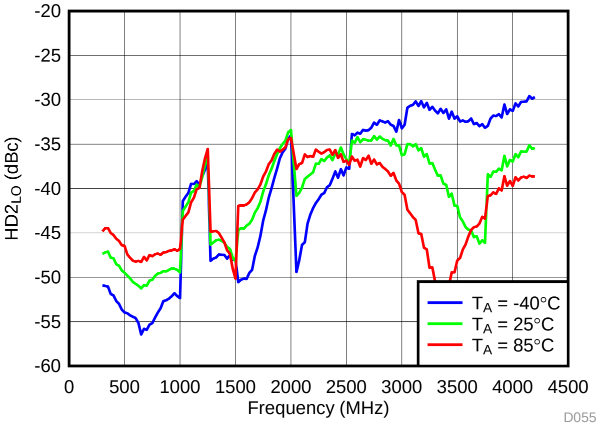


Figure 54. LO Second Harmonic vs Temperature, Low Power Mode

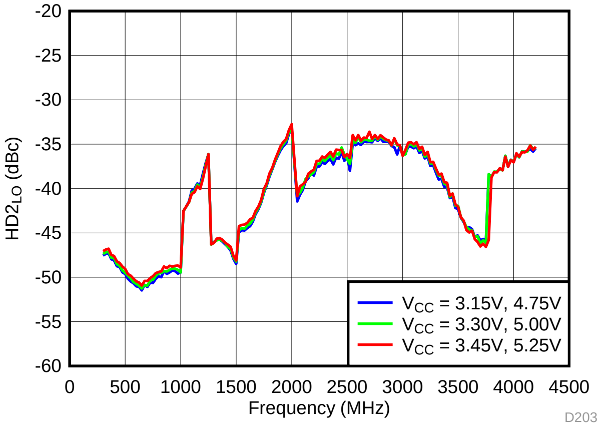


Figure 55. LO Second Harmonic vs Supply, Low Power Mode

Typical Characteristics - LO Harmonic (continued)

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16.

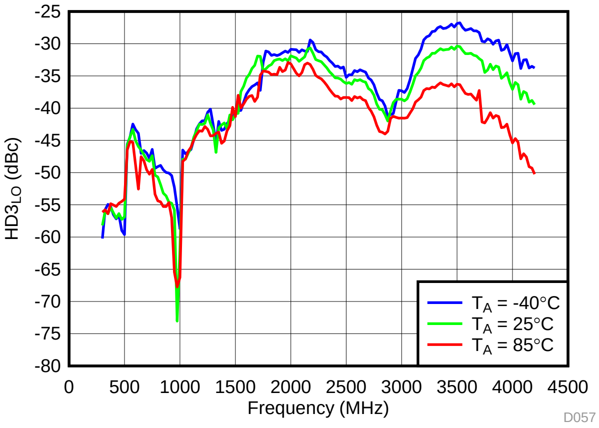


Figure 56. LO Third Harmonic vs Temperature, Typical Operating Mode

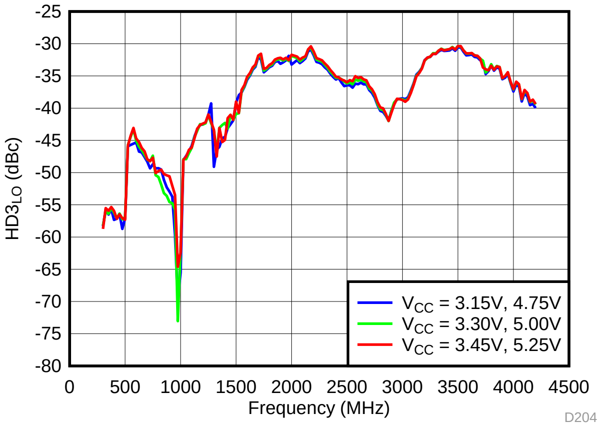


Figure 57. LO Third Harmonic vs Supply, Typical Operating Mode

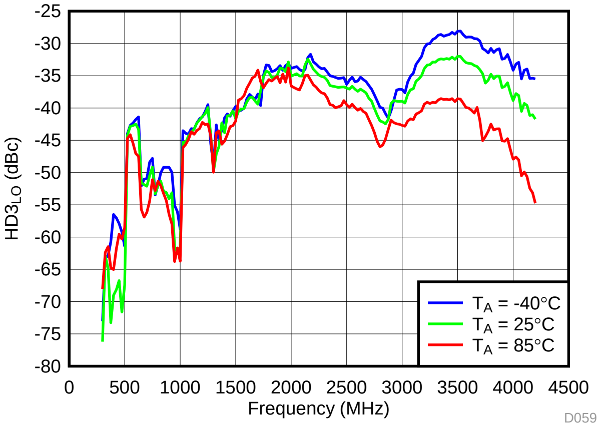


Figure 58. LO Third Harmonic vs Temperature, High Gain Mode

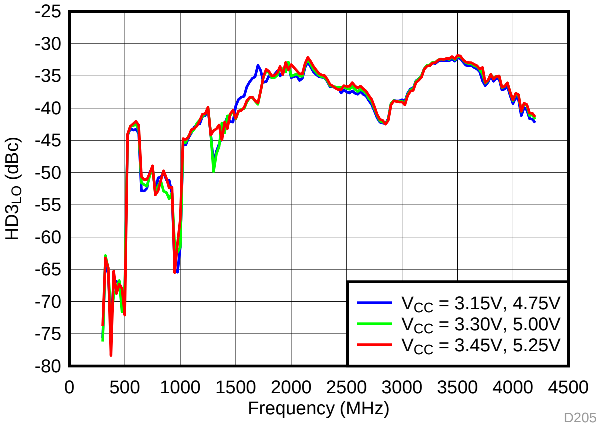


Figure 59. LO Third Harmonic vs Supply, High Gain Mode

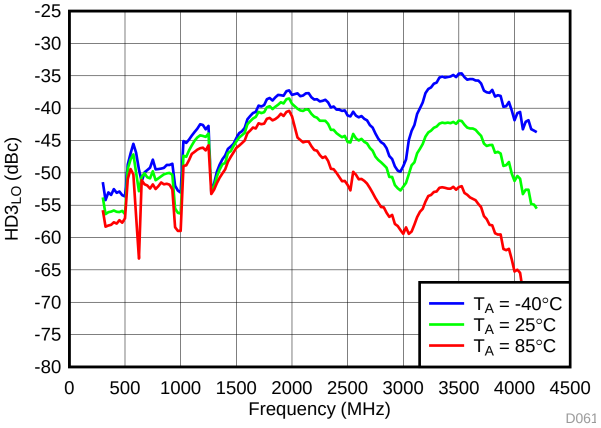


Figure 60. LO Third Harmonic vs Temperature, Low Power Mode

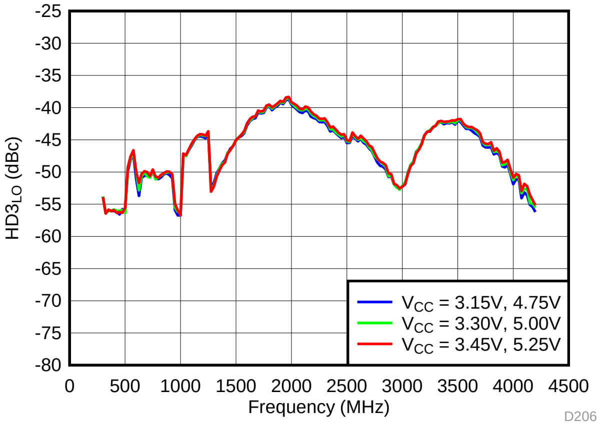


Figure 61. LO Third Harmonic vs Supply, Low Power Mode

6.16 Typical Characteristics - BB Harmonic

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK= 5 V, and T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16. Reported BB harmonic is from (f_{BB}) 4.5MHz.

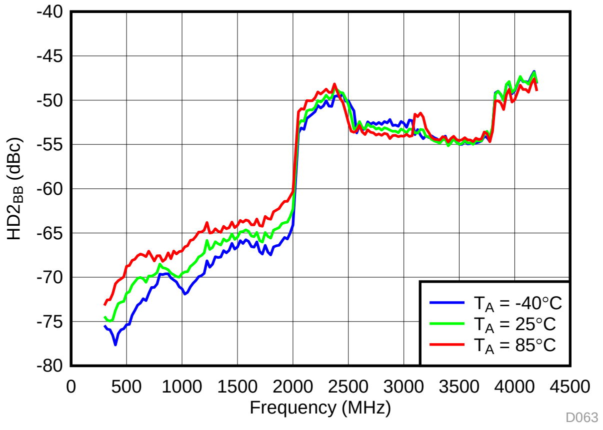


Figure 62. BB-HD2 vs Temperature, Typical Operating Mode

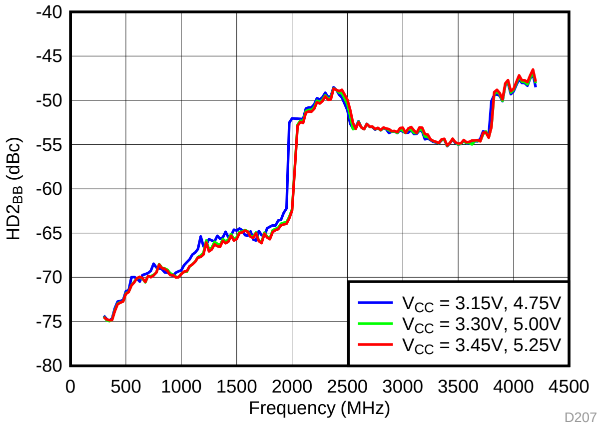


Figure 63. BB-HD2 vs Supply, Typical Operating Mode

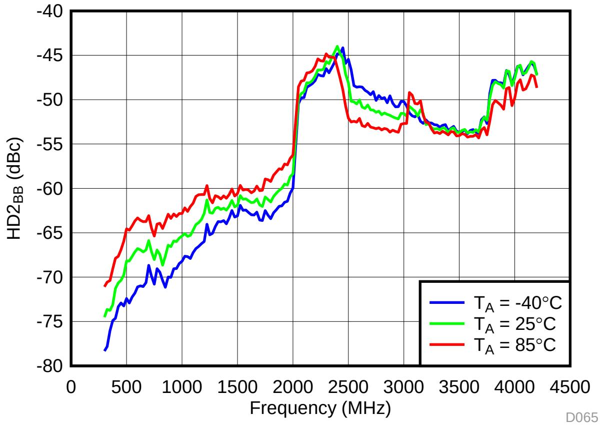


Figure 64. BB-HD2 vs Temperature, High Gain Mode

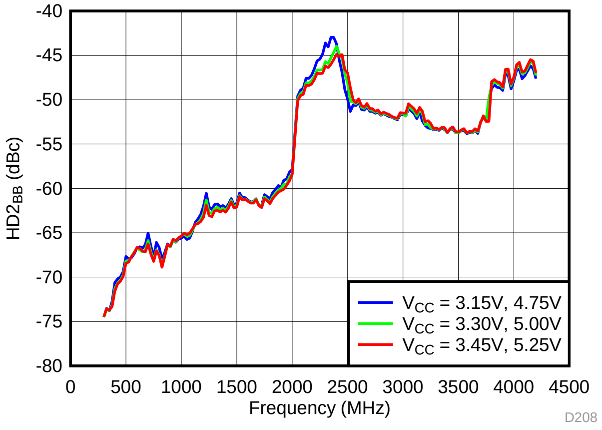


Figure 65. BB-HD2 vs Supply, High Gain Mode

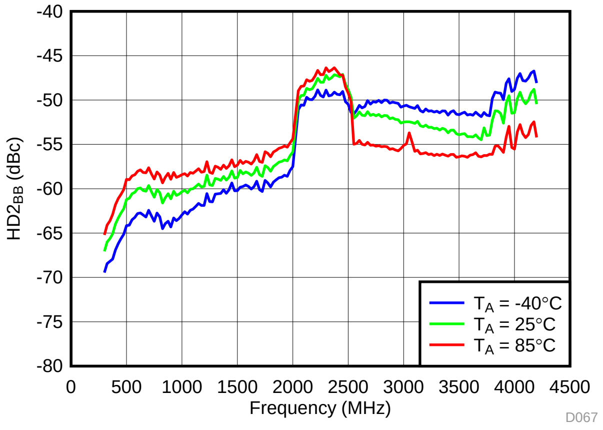


Figure 66. BB-HD2 vs Temperature, Low Power Mode

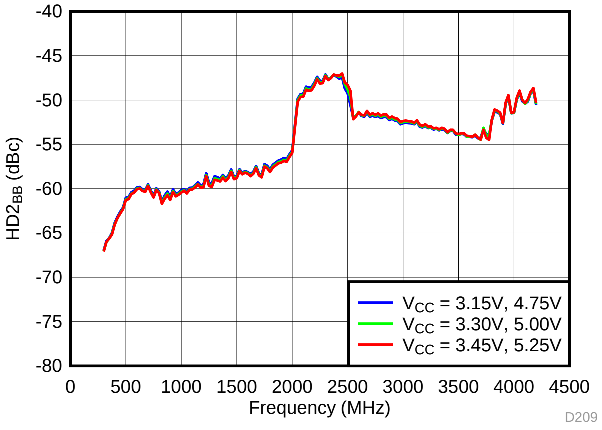


Figure 67. BB-HD2 vs Supply, Low Power Mode

Typical Characteristics - BB Harmonic (continued)

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK= 5 V, and T_A = 25°C, I/Q frequency (f_{BB}) 4.5 MHz and 5.5 MHz, V_{CM} = 0.25 V, and 4.7 pF series capacitor at RFOUT. Optimized bias settings as per Table 16. Reported BB harmonic is from (f_{BB}) 4.5MHz.

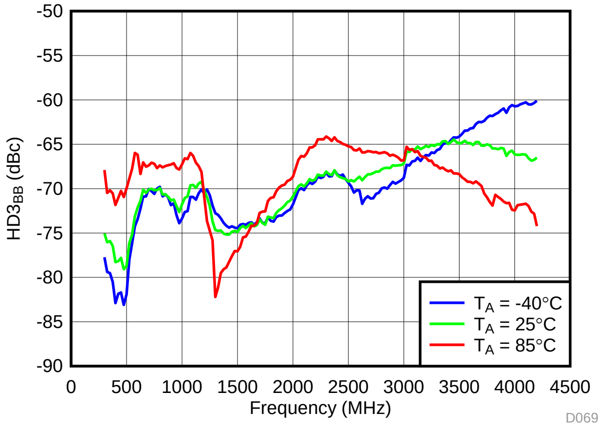


Figure 68. BB-HD3 vs Temperature, Typical Operating Mode

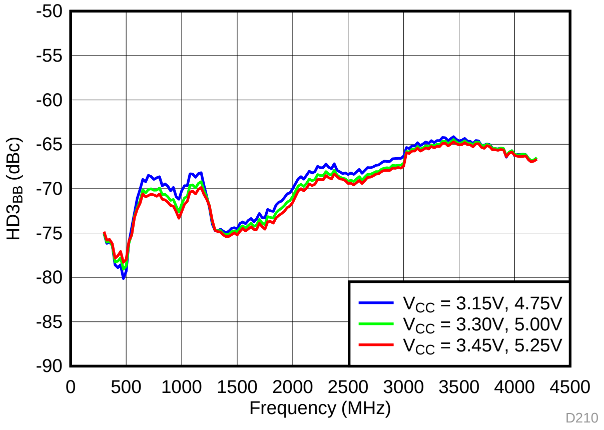


Figure 69. BB-HD3 vs Supply, Typical Operating Mode

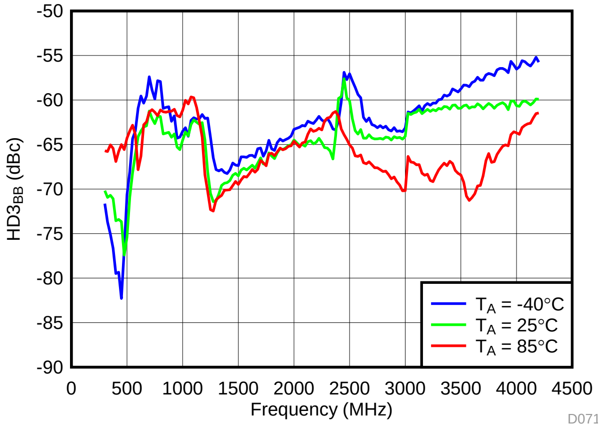


Figure 70. BB-HD3 vs Temperature, High Gain Mode

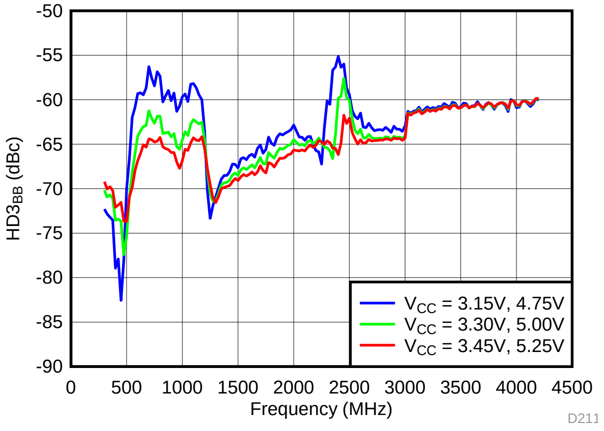


Figure 71. BB-HD3 vs Supply, High Gain Mode

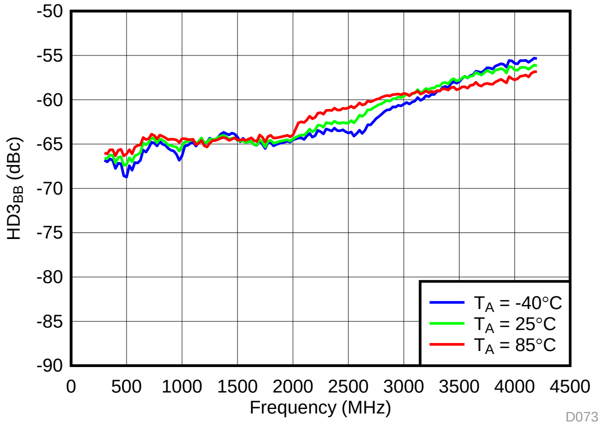


Figure 72. BB-HD3 vs Temperature, Low Power Mode

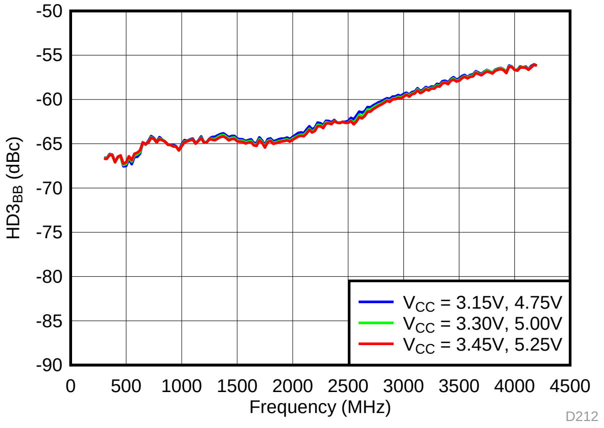
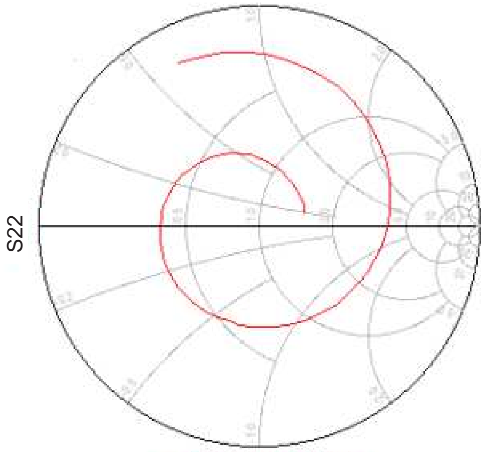


Figure 73. BB-HD3 vs Supply, Low Power Mode

6.17 Typical Characteristics - RF Output Return Loss

Unless specified all plots were created at RFOUT pin using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C



Frequency (400 MHz to 4200 MHz)

Figure 74. Smith Chart

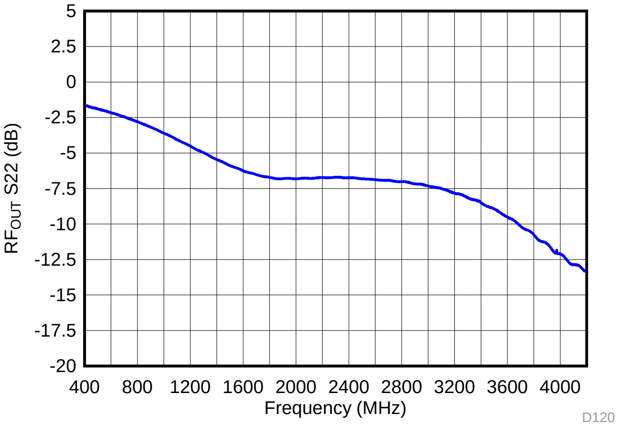


Figure 75. RF_{OUT} S22 vs Frequency

6.18 Typical Characteristics - PLL/VCO

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Measured at LO_OUTP with 50 Ω bias resistor and 47 pF series capacitor. Modulator section powered down. Reference frequency is set to 61.44 MHz. Optimized bias settings as per Table 16.

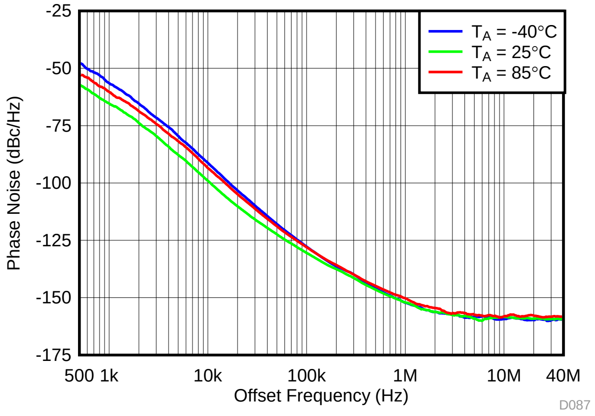


Figure 76. Open Loop Phase Noise at 450 MHz vs Temperature

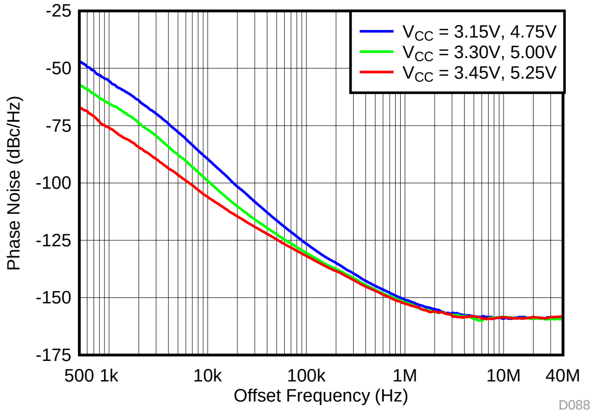


Figure 77. Open Loop Phase Noise at 450 MHz vs Supply

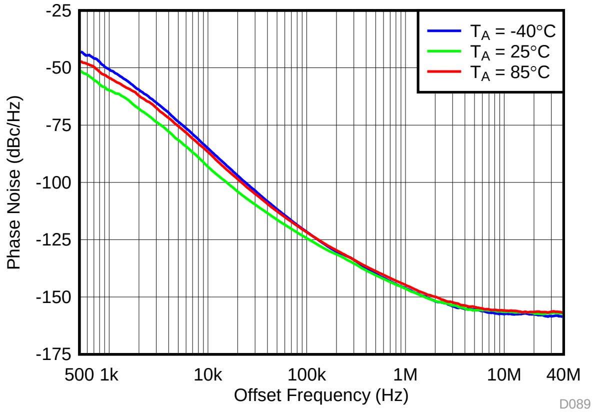


Figure 78. Open Loop Phase Noise at 900 MHz vs Temperature

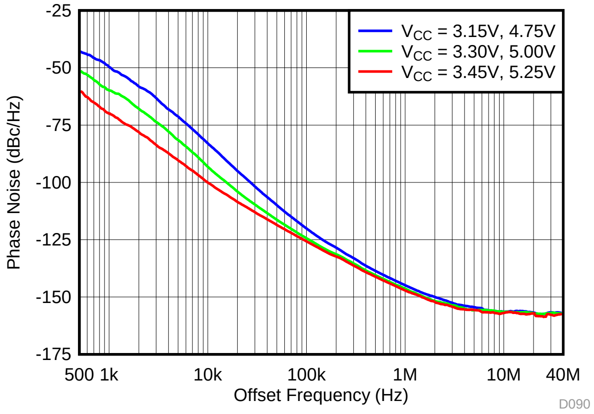


Figure 79. Open Loop Phase Noise at 900 MHz vs Supply

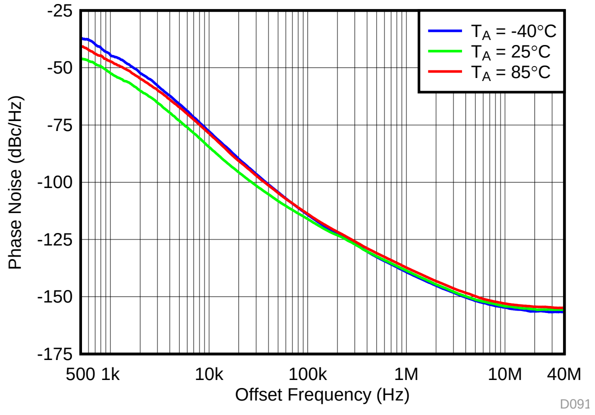


Figure 80. Open Loop Phase Noise at 1800 MHz vs Temperature

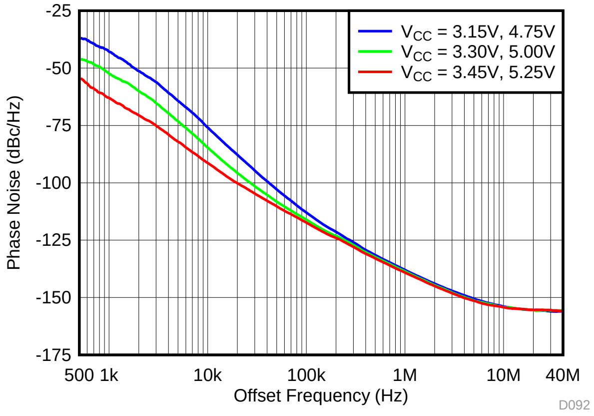


Figure 81. Open Loop Phase Noise at 1800 MHz vs Supply

Typical Characteristics - PLL/VCO (continued)

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Measured at LO_OUTP with 50 Ω bias resistor and 47 pF series capacitor. Modulator section powered down. Reference frequency is set to 61.44 MHz. Optimized bias settings as per Table 16.

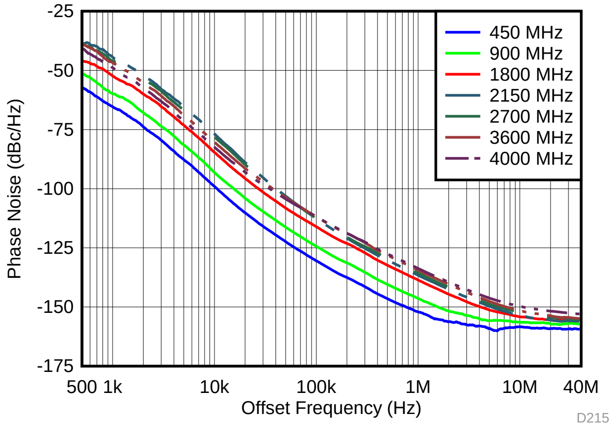


Figure 82. Open Loop Phase Noise vs Frequency

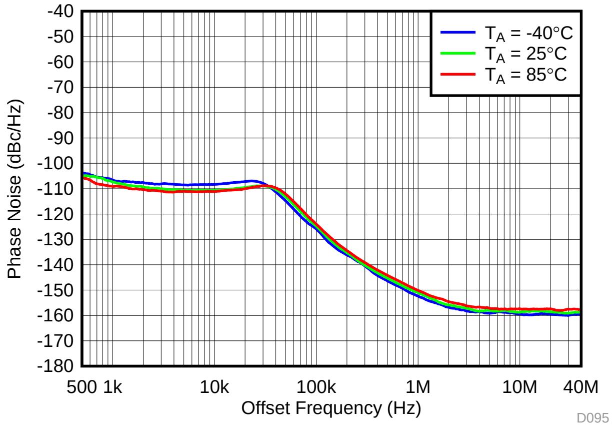


Figure 83. 450 MHz Frac-N (Closed Loop Phase Noise) vs Temperature

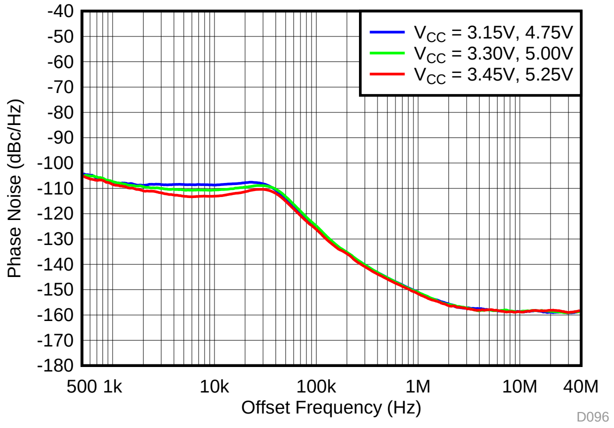


Figure 84. 450 MHz Frac-N (Closed Loop Phase Noise) vs Supply

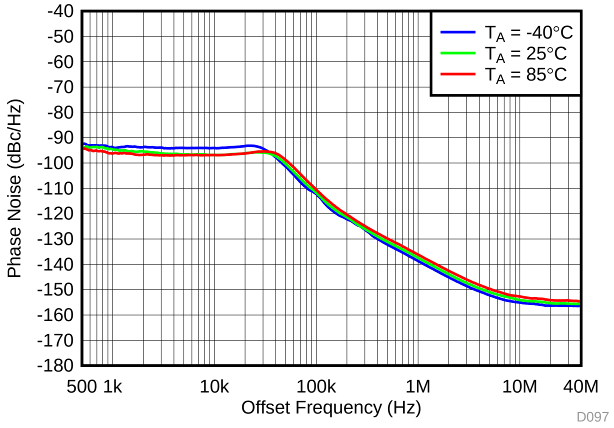


Figure 85. 1800 MHz Frac-N (Closed Loop Phase Noise) vs Temperature

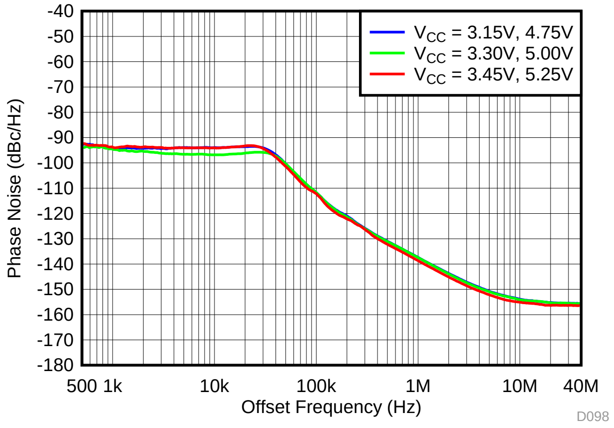


Figure 86. 1800 MHz Frac-N (Closed Loop Phase Noise) vs Supply

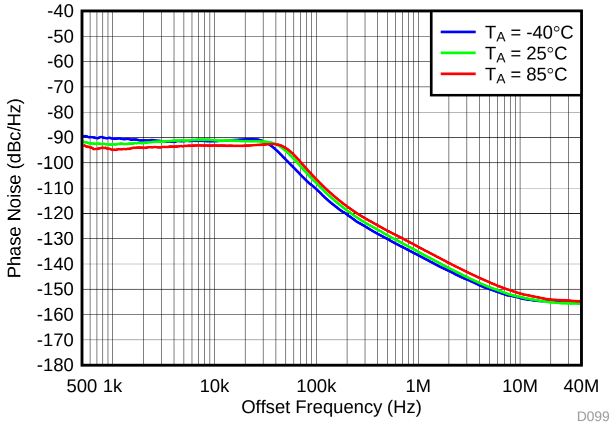


Figure 87. 2150 MHz Frac-N (Closed Loop Phase Noise) vs Temperature

Typical Characteristics - PLL/VCO (continued)

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Measured at LO_OUTP with 50 Ω bias resistor and 47 pF series capacitor. Modulator section powered down. Reference frequency is set to 61.44 MHz. Optimized bias settings as per Table 16.

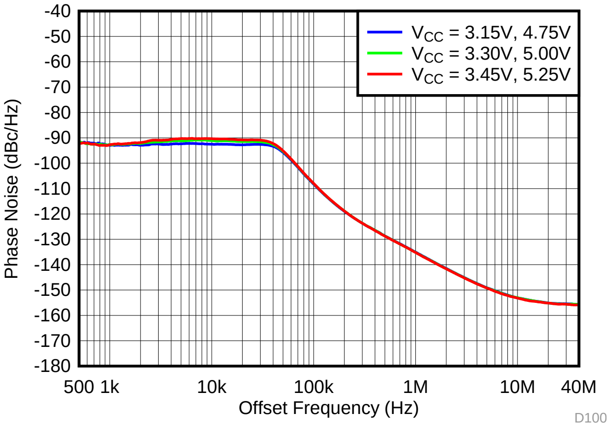


Figure 88. 2150 MHz Frac-N (Closed Loop Phase Noise) vs Supply

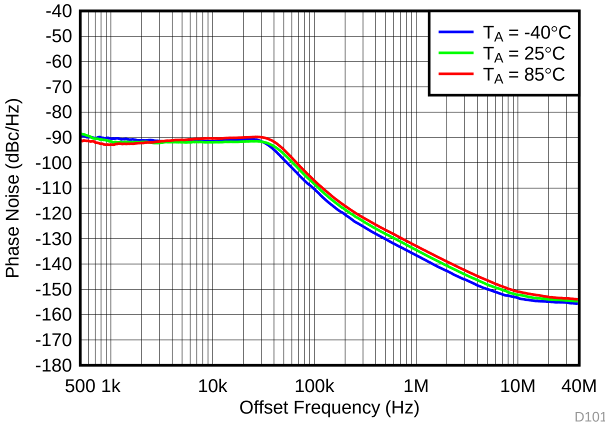


Figure 89. 2700 MHz Frac-N (Closed Loop Phase Noise) vs Temperature

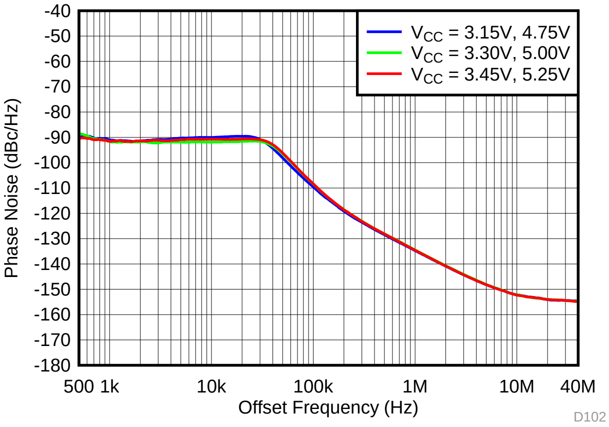


Figure 90. 2700 MHz Frac-N (Closed Loop Phase Noise) vs Supply

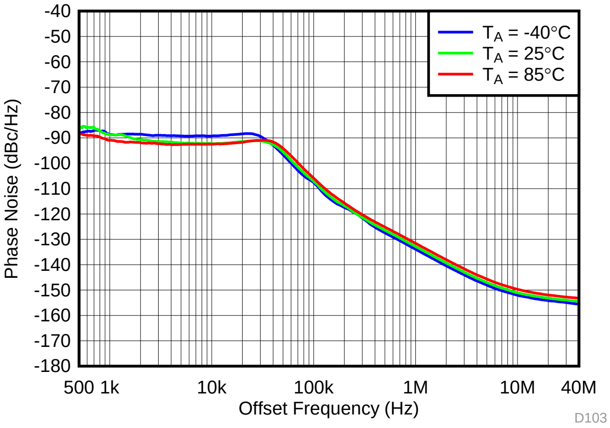


Figure 91. 3600 MHz Frac-N (Closed Loop Phase Noise) vs Temperature

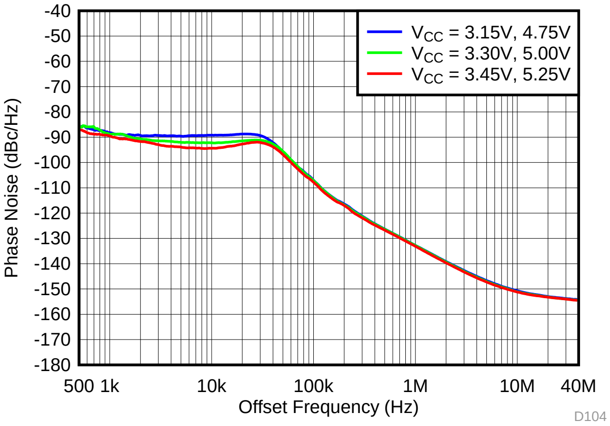


Figure 92. 3600 MHz Frac-N (Closed Loop Phase Noise) vs Supply

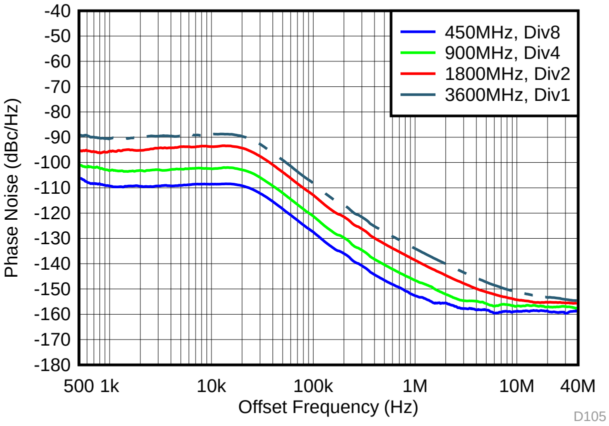


Figure 93. 450, 900, 1800, 3600 MHz Closed Loop Phase Noise vs Offset Frequency

Typical Characteristics - PLL/VCO (continued)

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Measured at LO_OUTP with 50 Ω bias resistor and 47 pF series capacitor. Modulator section powered down. Reference frequency is set to 61.44 MHz. Optimized bias settings as per Table 16.

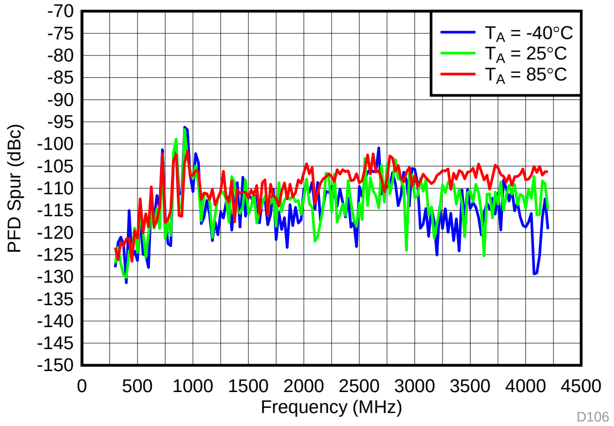


Figure 94. PFD Spur vs Temperature

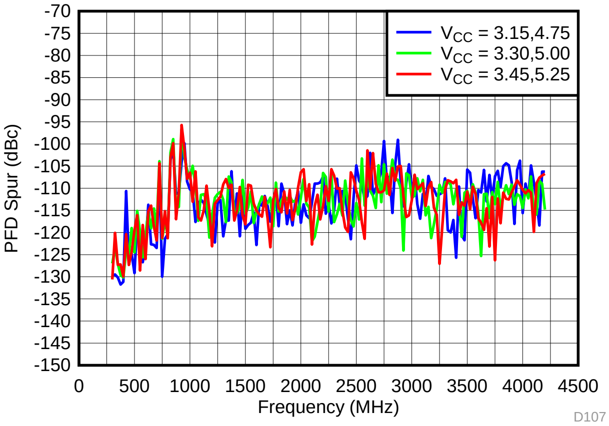


Figure 95. PFD Spur vs Supply

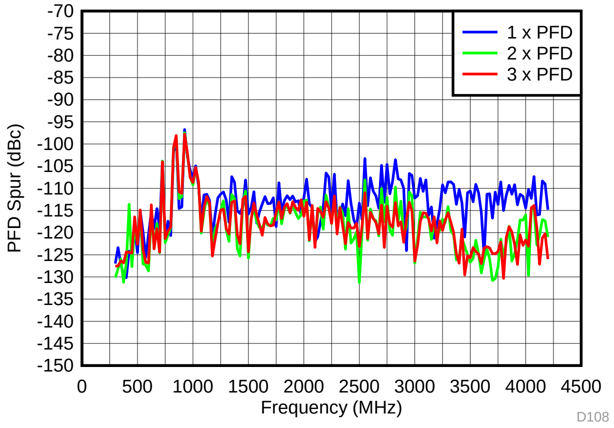


Figure 96. PFD Spur vs PFD Multiples

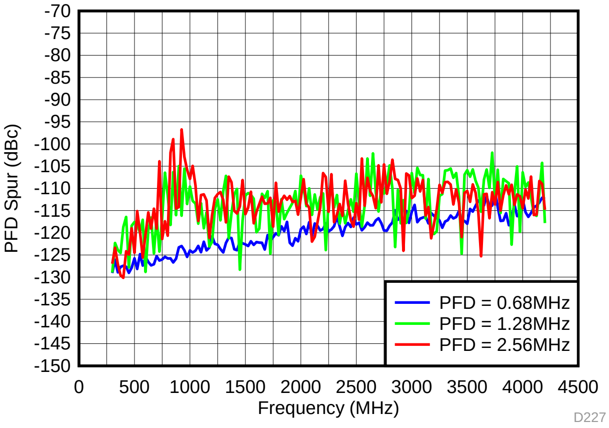


Figure 97. PFD Spur vs Frequency

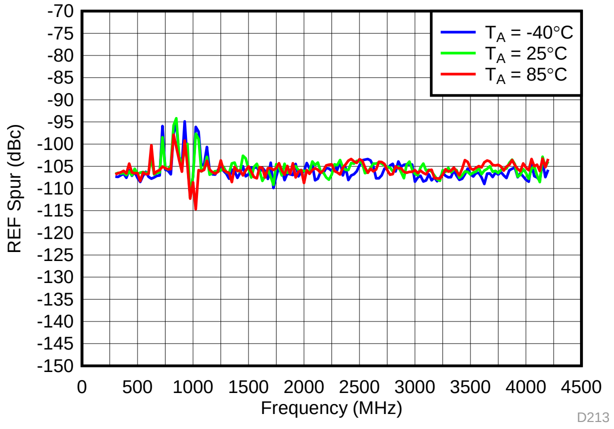


Figure 98. 1 x Reference Spur vs Temperature

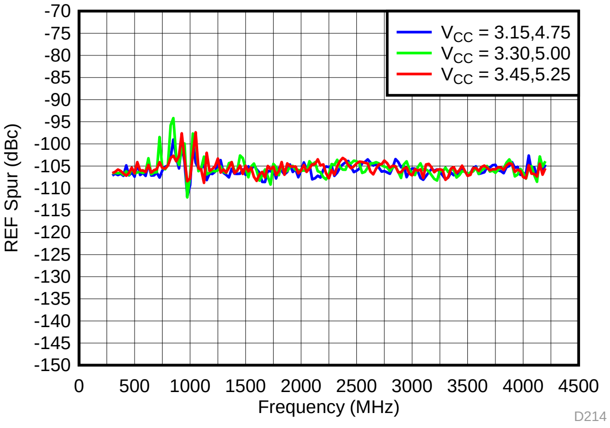


Figure 99. Reference Spur vs Supply

Typical Characteristics - PLL/VCO (continued)

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Measured at LO_OUTP with 50 Ω bias resistor and 47 pF series capacitor. Modulator section powered down. Reference frequency is set to 61.44 MHz. Optimized bias settings as per Table 16.

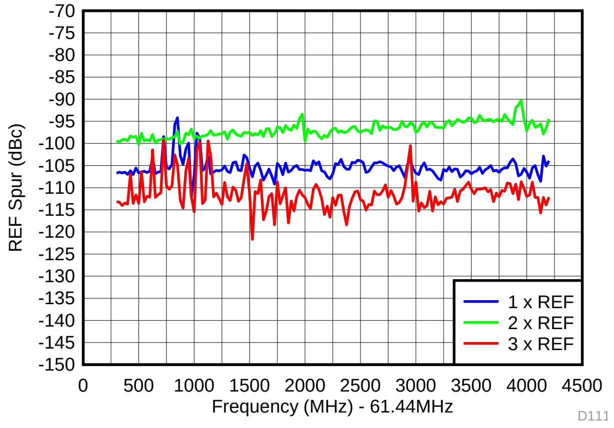


Figure 100. Reference Spur vs Reference Multiples

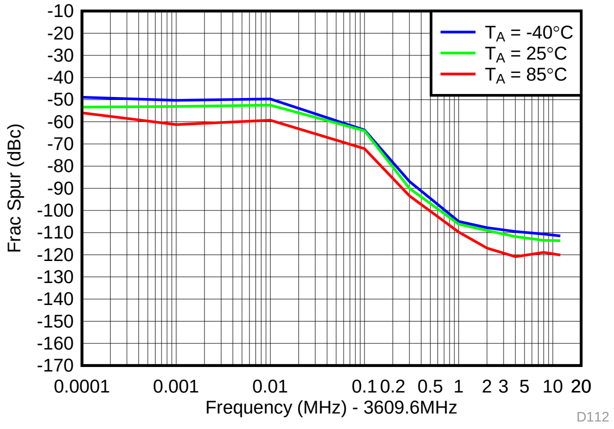


Figure 101. 3609.6 MHz Integer Boundary Spur vs Temperature

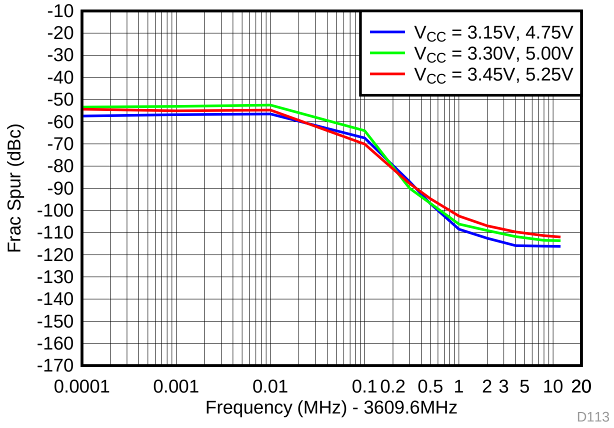


Figure 102. 3609.6 MHz Integer Boundary Spur vs Supply

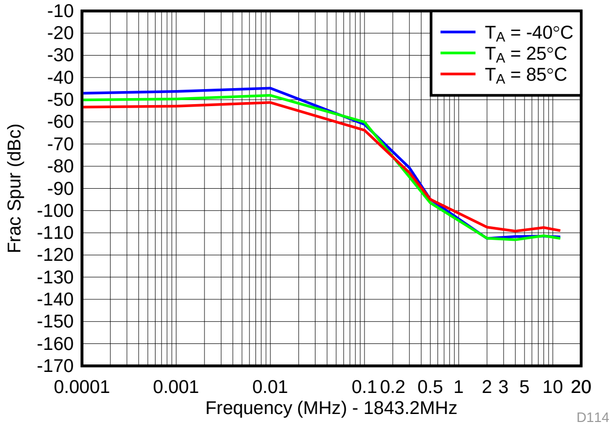


Figure 103. 1843.2 MHz Integer Boundary Spur vs Temperature

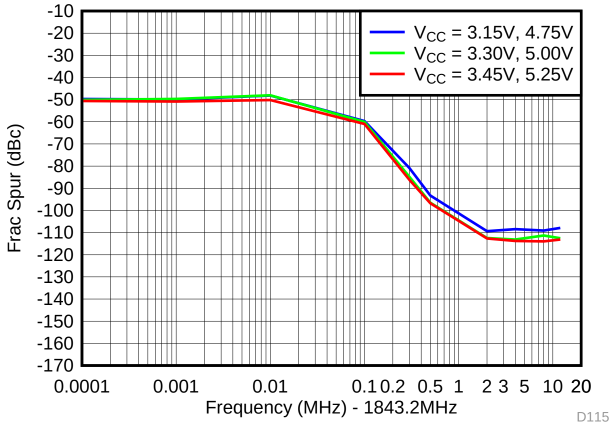
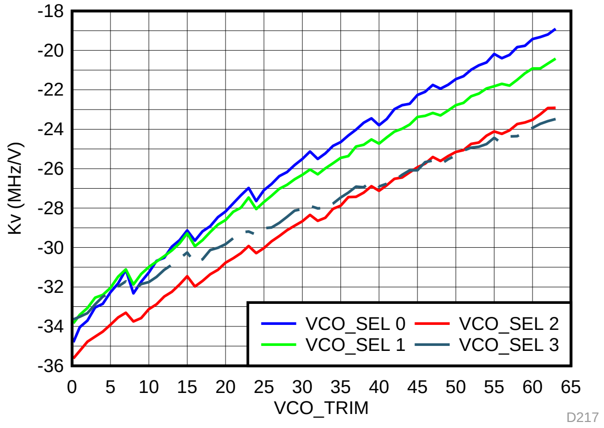


Figure 104. 1842.2 MHz Integer Boundary Spur vs Supply

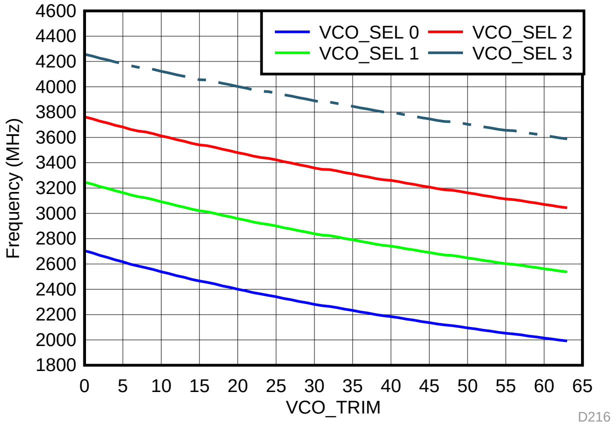


$V_{(tune)}$ = 1.1 V

Figure 105. K_{VCO} vs VCO Trim

Typical Characteristics - PLL/VCO (continued)

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Measured at LO_OUTP with 50 Ω bias resistor and 47 pF series capacitor. Modulator section powered down. Reference frequency is set to 61.44 MHz. Optimized bias settings as per Table 16.



$V_{(tune)}$ = 1.1 V

Figure 106. Frequency vs VCO_TRIM

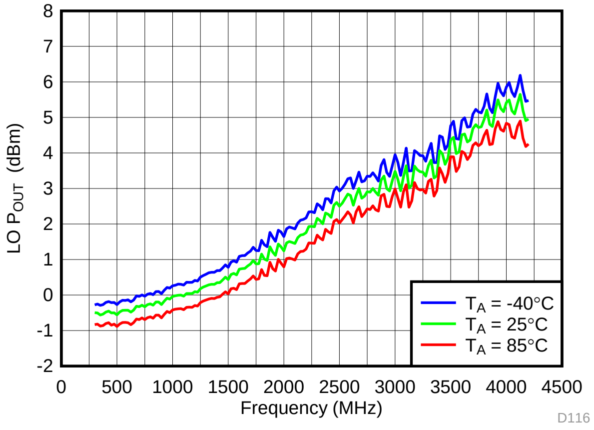


Figure 107. LO Output Power at LO_OUTP vs Temperature

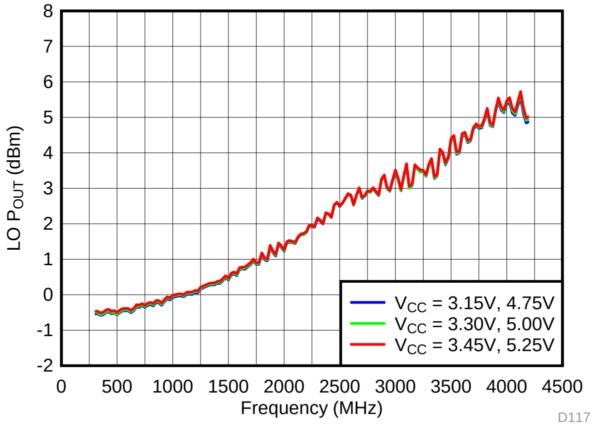


Figure 108. LO Output Power at LO_OUTP vs Supply

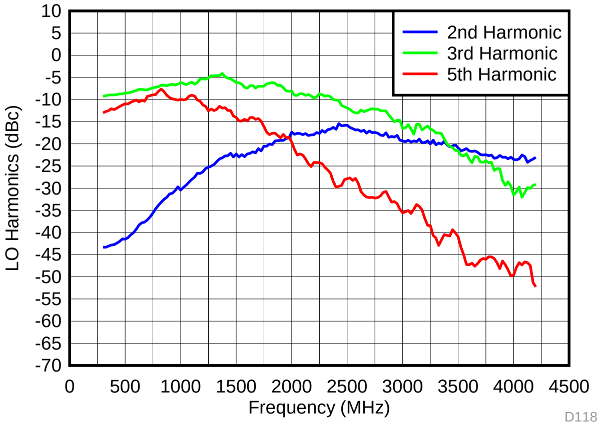


Figure 109. LO Harmonics at LO_OUTP vs Frequency

6.19 Typical Characteristics - Current Consumption

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Optimized bias settings as per Table 16

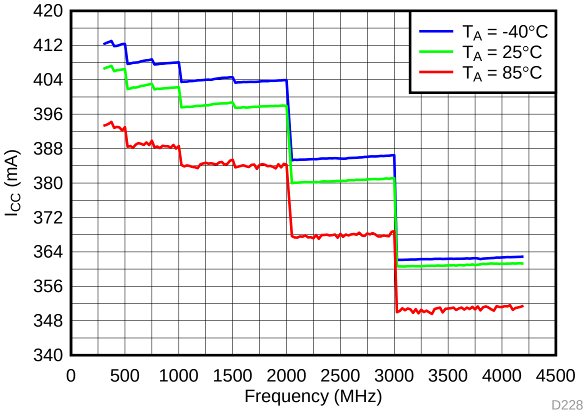


Figure 110. 3.3V Supply Current vs Temperature, Typical Operating Mode

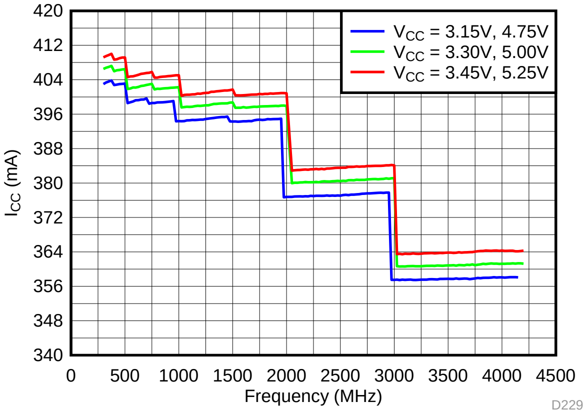


Figure 111. 3.3V Supply Current vs Supply, Typical Operating Mode

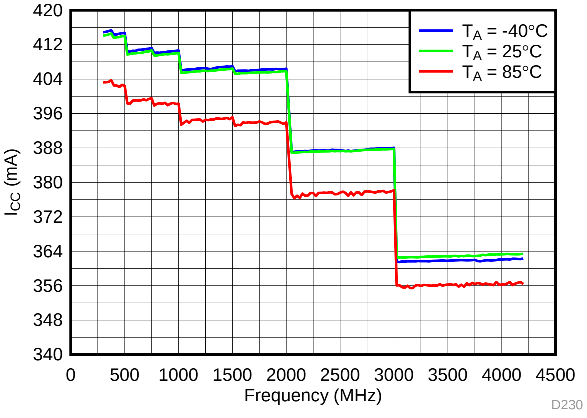


Figure 112. 3.3V Supply Current vs Temperature, High Gain Mode

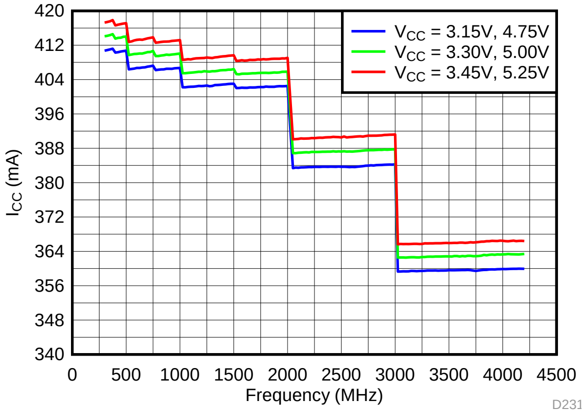


Figure 113. 3.3V Supply Current vs Supply, High Gain Mode

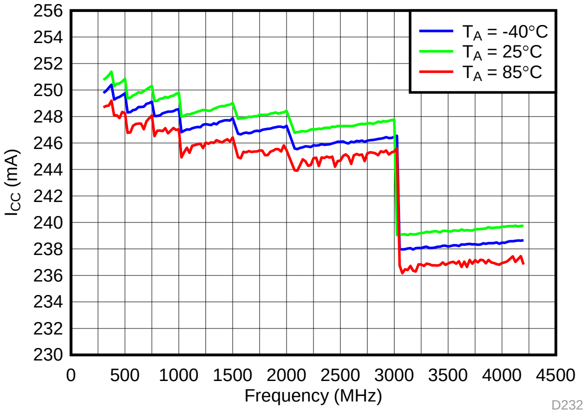


Figure 114. 3.3V Supply Current vs Temperature, Low Power Mode

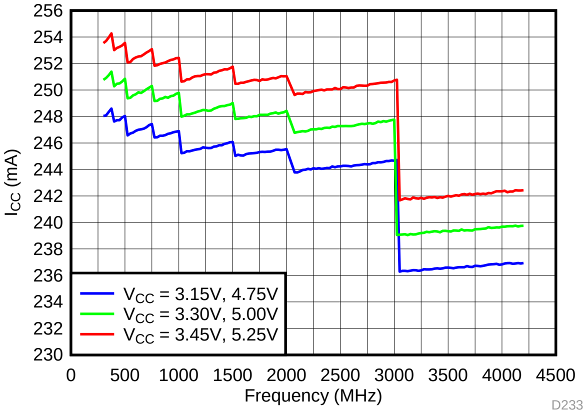


Figure 115. 5V Supply Current vs Supply, Low Power Mode

Typical Characteristics - Current Consumption (continued)

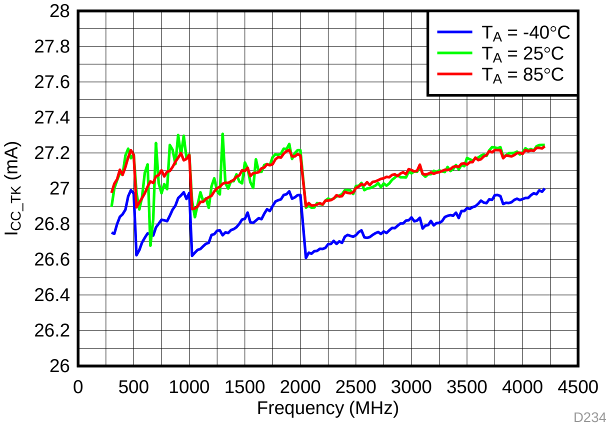


Figure 116. 5V Supply Current vs Temperature, Typical Operating Mode

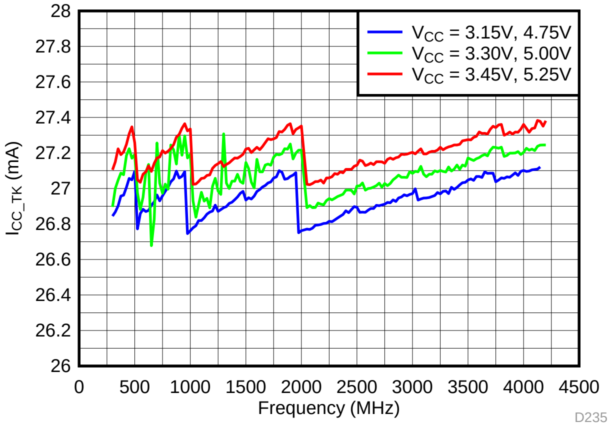


Figure 117. 5V Supply Current vs Temperature, Typical Operating Mode

6.20 Typical Characteristics - Power Dissipation

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Optimized bias settings as per Table 16.

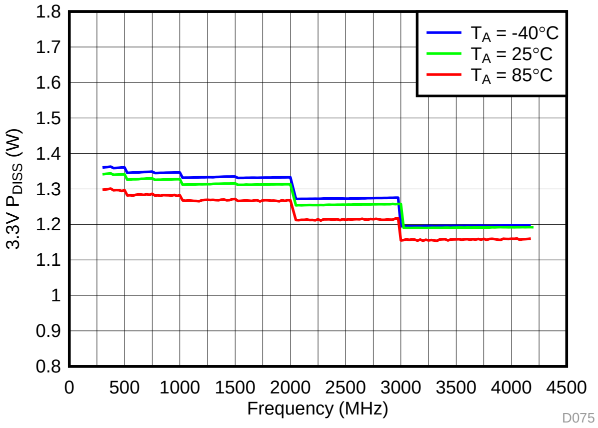


Figure 118. 3.3 V P_{DISS} vs Temperature, Typical Operating Mode

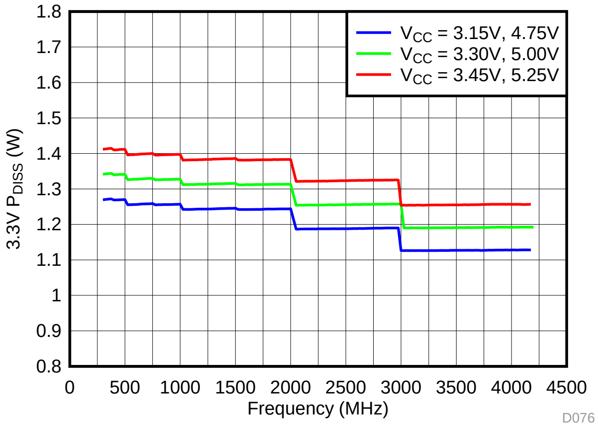


Figure 119. 3.3 V P_{DISS} vs Supply, Typical Operating Mode

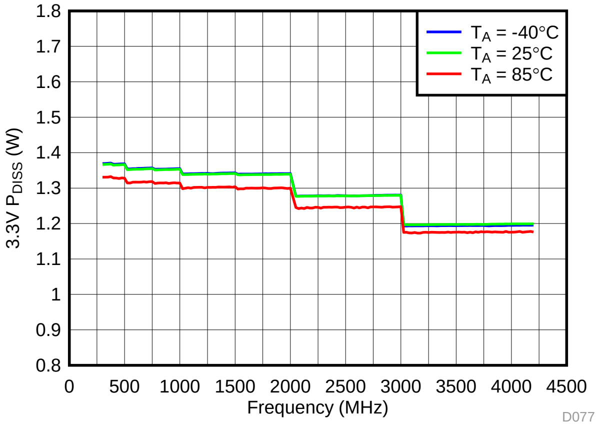


Figure 120. 3.3 V P_{DISS} vs Temperature, High Gain Mode

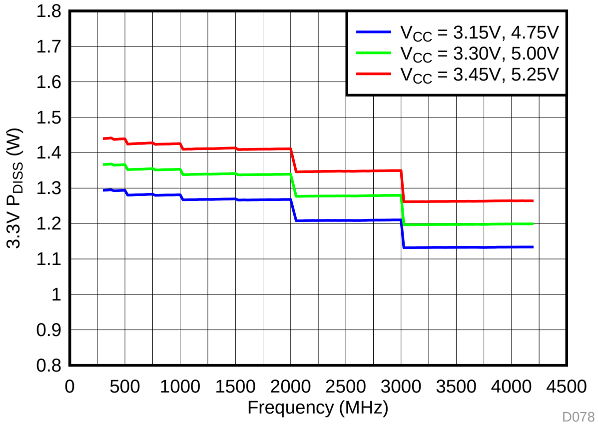


Figure 121. 3.3 V P_{DISS} vs Supply, High Gain Mode

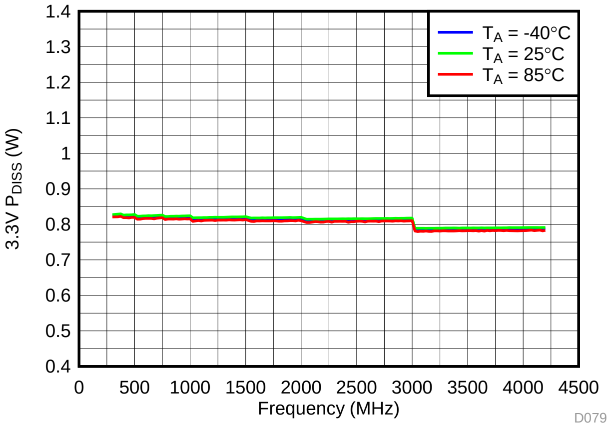


Figure 122. 3.3 V P_{DISS} vs Temperature, Low Power Mode

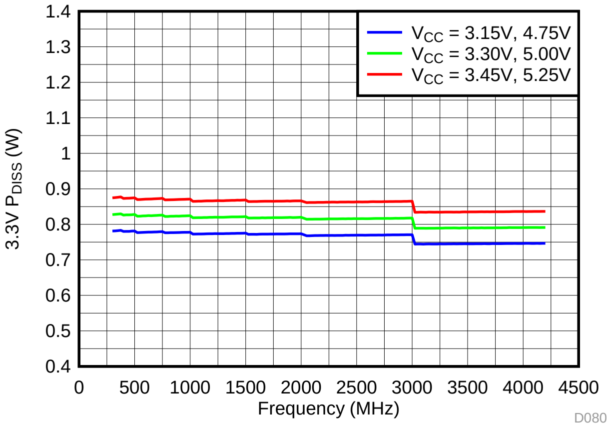


Figure 123. 3.3 V P_{DISS} vs Supply, Low Power Mode

Typical Characteristics - Power Dissipation (continued)

Unless specified all plots were created using TRF3722EVM, VCC = 3.3 V, VCC_TK = 5 V, and T_A = 25°C. Optimized bias settings as per Table 16.

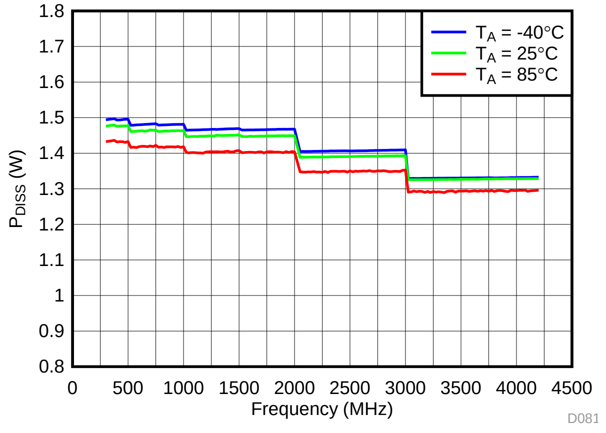


Figure 124. Total P_{DISS} vs Temperature, Typical Operating Mode

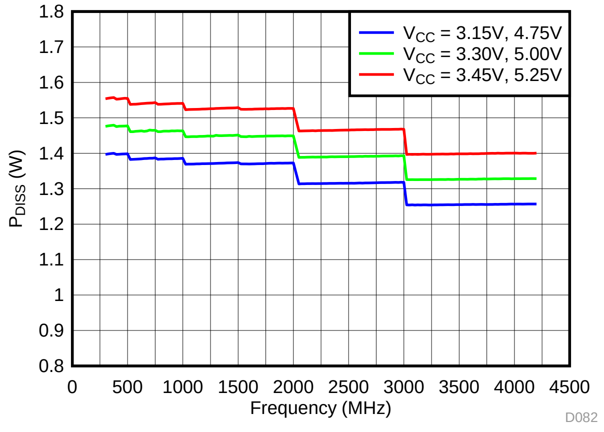


Figure 125. Total P_{DISS} vs Supply, Typical Operating Mode

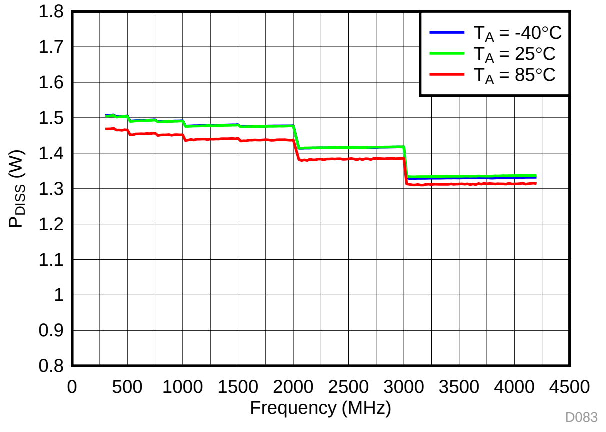


Figure 126. Total P_{DISS} vs Temperature, High Gain Mode

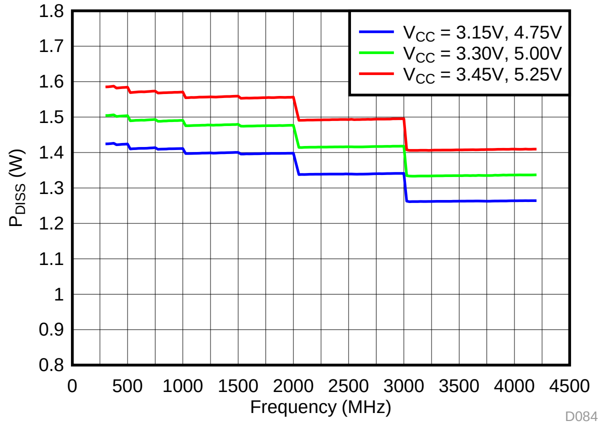


Figure 127. Total P_{DISS} vs Supply, High Gain Mode

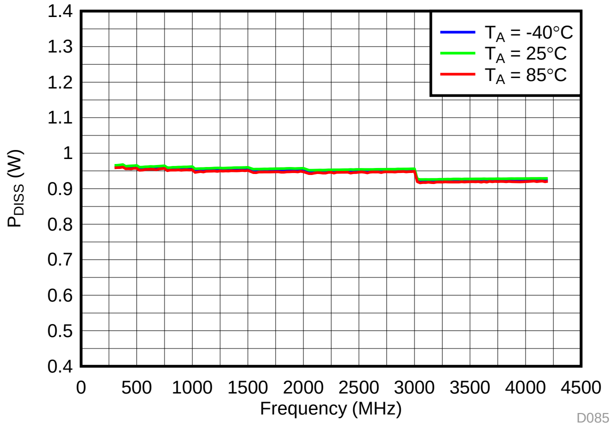


Figure 128. Total P_{DISS} vs Temperature, Low Power Mode

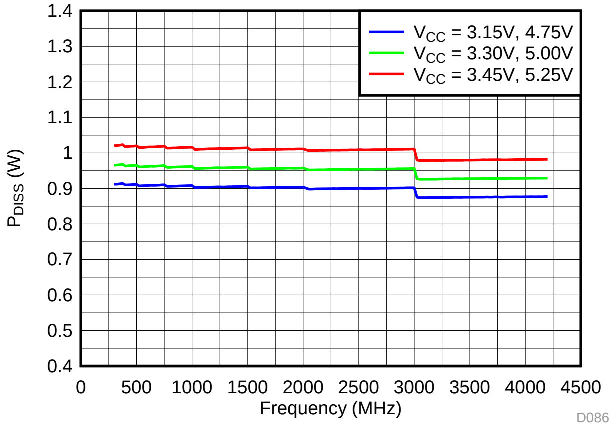


Figure 129. Total P_{DISS} vs Supply, Low Power Mode

7 Parameter Measurement Information

7.1 Serial Interface Timing Diagram

The TRF3722 features a four-wire serial programming interface (4WI) that controls an internal 32-bit shift register with seven parallel registers. There are total of three signals that must be applied: the clock (CLK), the serial data (DATA), and the latch enable (LE). The fouth signal is the read back (RDBK) signal. The serial data (DB0-DB31) are loaded least significant bit (LSB) first, and read on the rising edge of the CLK. LE is asynchronous to the CLK signal; at its rising edge, the data in the shift register are loaded into the selected internal register. Figure 130 shows the timing diagram the 4WI. Table 1 lists the 4WI timing for the write operation.

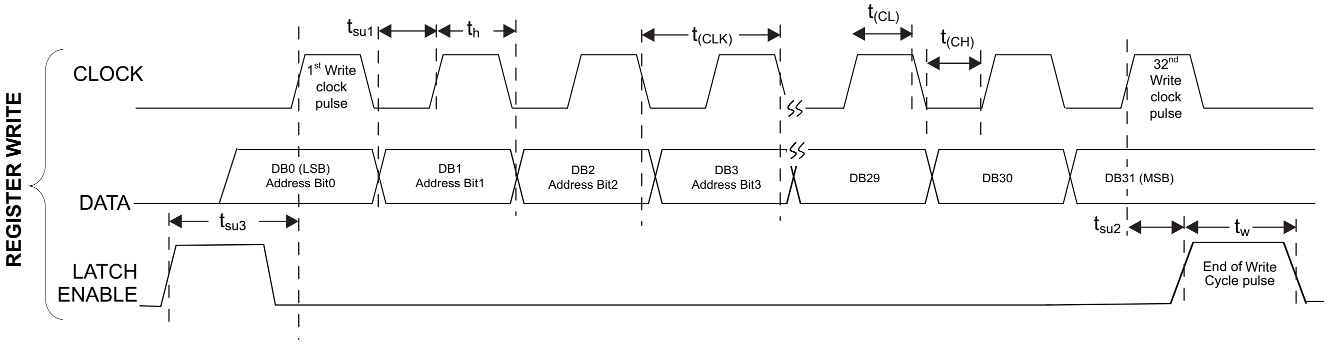


Figure 130. 4WI Writing Timing Diagram

Table 1. 4WI Timing for Write Operation

		MIN	TYP	MAX	UNIT
t_h	Hold time, data to clock	20			ns
t_{SU1}	Setup time, data to clock	20			ns
t_{CH}	Clock low duration	20			ns
t_{CL}	Clock High duration	20			ns
t_{SU2}	Setup time, clock to enable	20			ns
t_{CLK}	Clock period	50			ns
t_W	Enable Time	50			ns
t_{SU3}	Setup time, Latch to Data	70			ns

TRF3722 integrates 7 registers: Register 0 (000) to Register 6 (110). Registers 1 through 6 are used to set-up and control the TRF3722 functionalities, while register 0 is used for the read-back function. Each read-back is composed by two phases: writing followed by the actual reading of the internal data. This is shown in the timing diagram in Figure 131.

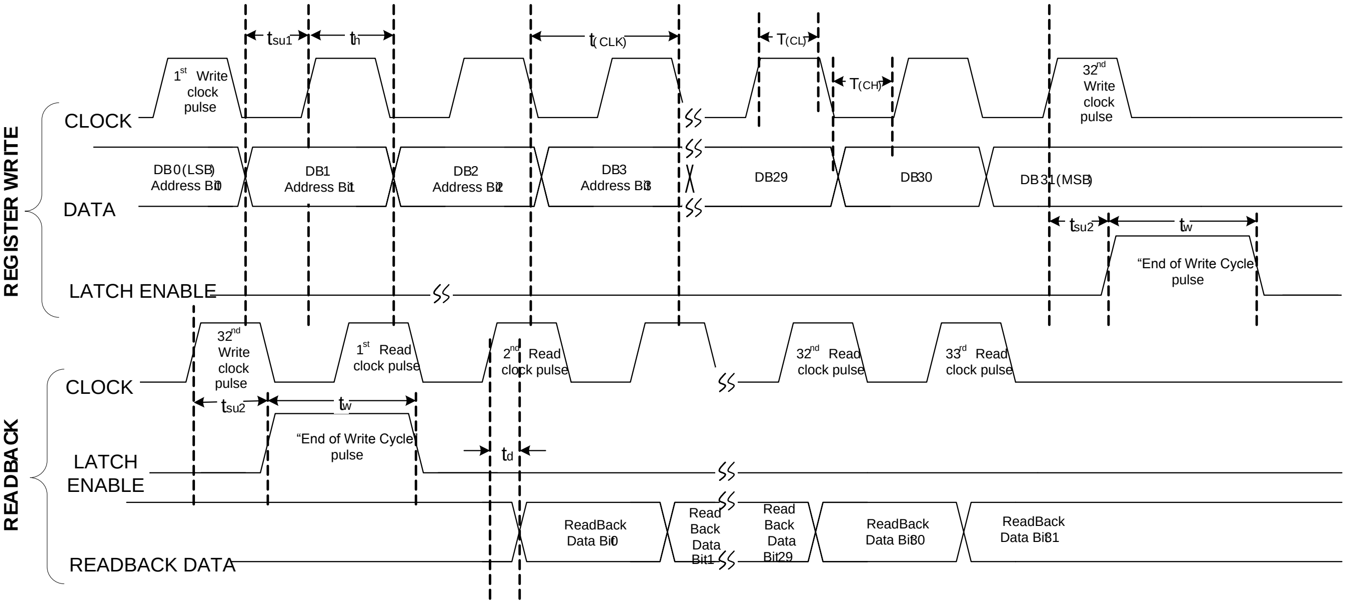


Figure 131. 4WI Read-Back Timing Diagram

During the writing phase a command is sent to TRF3722 register 0 to set it in read-back mode and to specify which register is to be read. In the proper reading phase, at each rising clock edge, the internal data is transferred into the RDBK pin and can be read at the following falling edge (LSB first). The first clock after the LE goes high (end of writing cycle) is idle and the following 32 clocks pulses will transfer the internal register content to the RDBK pin. Table 2 shows the Readback timing.

Table 2. 4WI Timing for Readback Timing

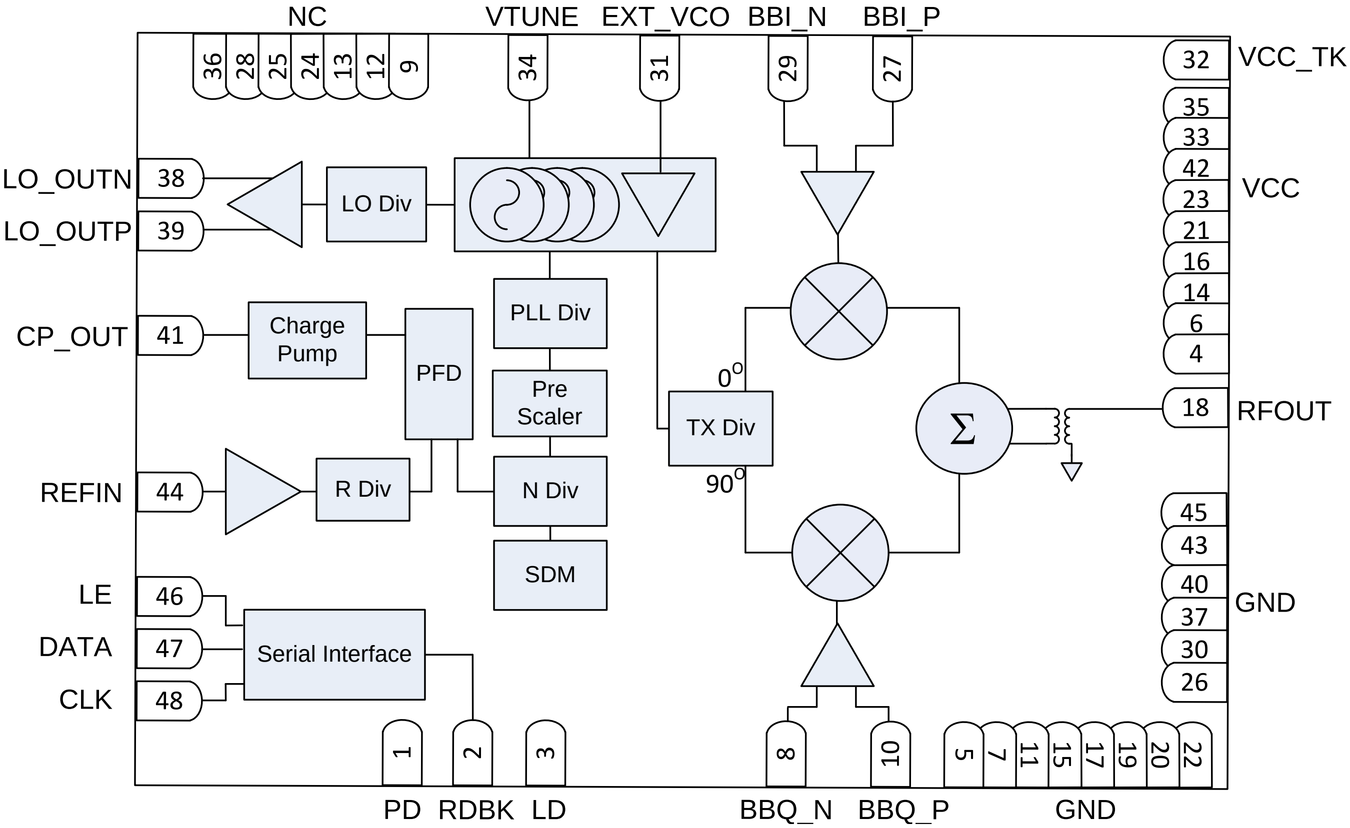
		MIN	TYP	MAX	UNIT	COMMENT
t_h	Hold time, data to clock	20			ns	
t_{SU1}	Setup time, data to clock	20			ns	
t_{CH}	Clock low duration	20			ns	
t_{CL}	Clock High duration	20			ns	
t_{SU2}	Setup time, clock to enable	20			ns	
t_{SU3}	Setup time, enable to Readback clock	20			ns	
t_d	Delay time, clock to Readback data output	10				
t_W	Enable Time	50			ns	Equals Clock period
$t_{(CLK)}$	Clock period	50			ns	

8 Detailed Description

8.1 Overview

TRF3722 integrates a high performance direct conversion quadrature modulator with exceptional linearity and low noise performance. The modulator which upconverts low frequency baseband signal to high frequency RF typically operates at 0.25 V common mode. It supports seamless interface with current source DACs. It also features high gain and low power operating modes. Additionally, TRF3722 integrates PLL and VCO to provide the local oscillator (LO) to the integrated modulator. The PLL and VCO provides excellent phase noise and extremely low spurious performance. The device also provides an LO output for driving another modulator or mixer. TRF3722 supports the use of an external VCO or LO signal.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 RF Output

The RF output is single ended and can drive a 50-Ω load. It can be tuned with the use of an output matching network to optimize the linearity and return loss performance within a selected band.

8.3.2 Baseband Inputs

The baseband inputs consist of the in-phase signal (I) and the quadrature-phase signals (Q). These I and Q signals are differential. The baseband lines are nominally biased at 0.25-V common-mode voltage (V_{CM}); however, the device can operate with a V_{CM} in the range of 0 V to 0.5 V. The baseband input lines are normally terminated externally 50 Ω on TRF3722 evaluation board, though it is possible to modify this value if necessary to match to an external filter load impedance requirement.

8.3.3 LO Output

The LO outputs are open collector differential outputs and are biased externally. These differential outputs can be tuned to optimized output power along with OUTBUF_BIAS register settings. It also is possible to use LO outputs in single ended mode.

8.3.4 PLL Architecture

Figure 132 illustrates a block diagram of the PLL architecture.

The VCO output frequency (f_{VCO}) is given by Equation 1:

$$f_{VCO} = \frac{f_{REF}}{RDIV} \text{ x PLL DIV x } \left(NINT + \frac{NFRAC}{2^{25}} \right) \quad (1)$$

$$f_{PFD} = \frac{f_{REF}}{RDIV} \quad (2)$$

$$\text{PLL DIV} = 2^{PLL\_DIV\_SEL} \quad (3)$$

$$f_{VCO} = f_{PFD} \text{ x PLL DIV x } \left(NINT + \frac{NFRAC}{2^{25}} \right) \quad (4)$$

Where f_{REF} is the reference input frequency, RDIV is the reference divider division ratio and the phase - frequency detector frequency is f_{PFD}. PLL_DIV_SEL controls the division ratio of the programmable divider (PLL DIV) before the dual-modulus prescaler (DMP). NINT and NFRAC/2^{25} is the integer and fractional part of the fractional divider (N.f), respectively. In Integer mode, the fractional setting is ignored and Equation 5 is applied.

$$f_{VCO} = f_{PFD} \text{ x PLL DIV x NINT} \quad (5)$$

The complete feedback divider block consists of a PLL DIV, DMP, and N.f. The prescaler can be programmed as either a 4/5 or an 8/9. N.f includes an *A* and *M* digital counters.

Feature Description (continued)

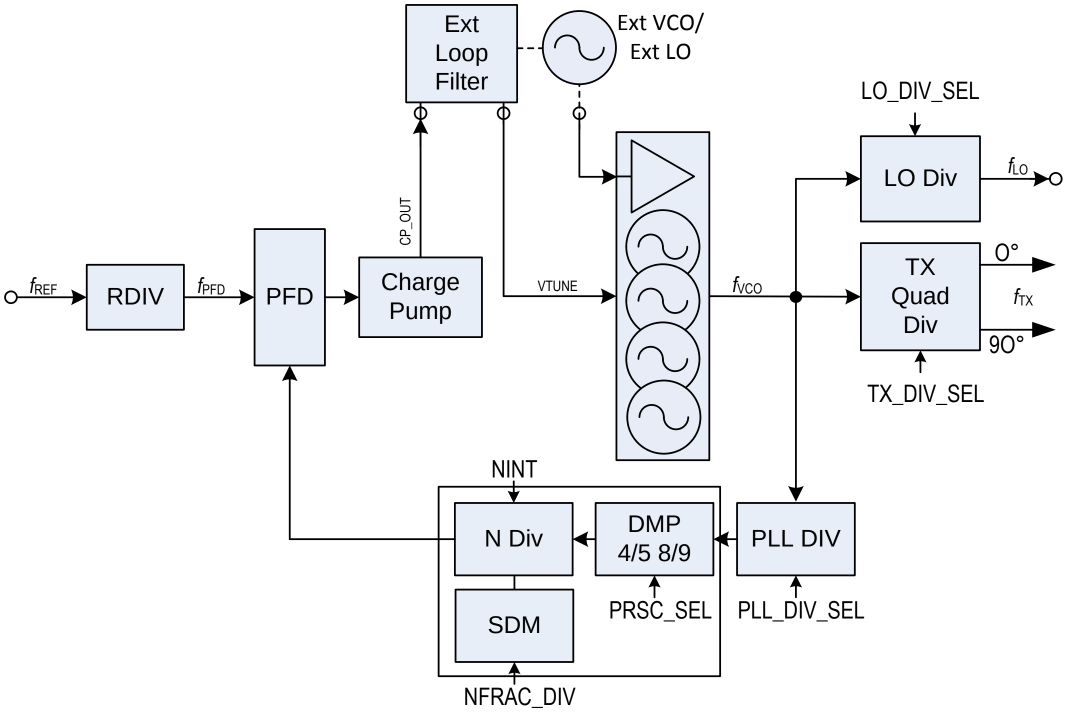


Figure 132. PLL Architecture

8.3.5 External VCO

An external LO or VCO signal may be applied. If an external LO is used the internal PLL can be powered down. Alternatively, dividers, phase-frequency detector, and charge pump can remain enabled and may be used to control the V_{TUNE} of an external VCO. EN_EXTVCO is used to select the internal or external VCO.

8.3.6 Loop Filter

Loop filter design is critical for achieving low closed loop phase noise. Complete modulator performance data has been measured using integer mode loop filter. The integer mode loop filter was designed considering loop bandwidth 40 kHz and f_{PFD} 2.56 MHz. Phase margin of 60 degrees was considered. Refer to TRF3722EVM User's Guide to obtain the details on TRF3722 loop component calculations. Figure 133 shows integer loop filter.

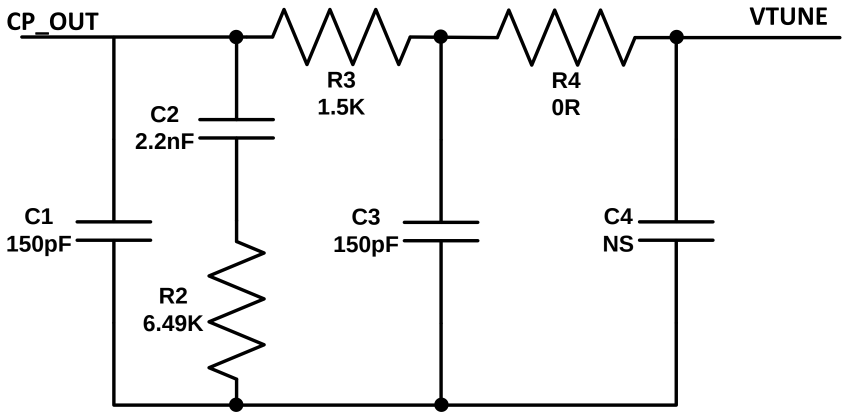


Figure 133. Integer Loop Filter

Feature Description (continued)

Frac-N performance data is obtained using the fractional loop filter shown in Figure 134. 40 kHz loop bandwidth and 15.36 MHz PFD was considered.

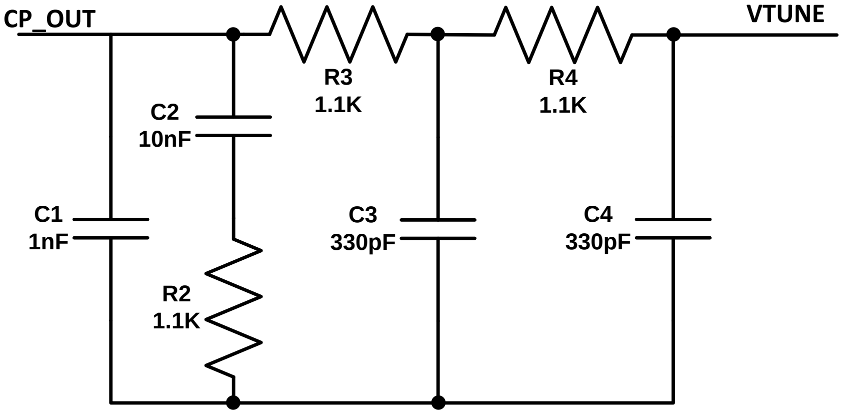


Figure 134. Fractional Loop Filter

8.3.7 Lock Detect

The lock detect signal is generated in the phase frequency detector by comparing the two input signals. When the two compared phase signals remain aligned for several clock cycles, an internal signal goes high. The precision of this comparison is controlled through the LD_ANA_PREC bits. This internal signal is then averaged and compared against a reference voltage to generate the lock detect (LD) signal. The number of averages used is controlled through LD_DIG_PREC. Therefore, when the VCO is frequency locked, LD is high. When the VCO frequency is not locked, LD may pulse high or exhibit periodic behavior.

By default, the internal lock detect signal is made available on the LD terminal. Register bits MUX_CTRL can be used to control a multiplexer to output other diagnostic signals on the LD output.

8.4 Device Functional Modes

8.4.1 Selecting PLL Divider Values

With reference to the PLL architecture illustrated in Figure 132, operation of the PLL requires TX_DIV_SEL / LO_DIV_SEL, PLL_DIV_SEL, RDIV, NINT, NFRAC and PRSC_SEL bits to be calculated.

a. **TX_DIV_SEL / LO_DIV_SEL**

The LO to the integrated modulator (f_{TX}) and additional LO output (f_{LO}) frequency is related to f_{VCO} according to the following:

$f_{TX} = f_{VCO}$ / TX DIV

$f_{LO} = f_{VCO}$ / LO DIV

Where TX DIV and LO DIV are related to TX_DIV_SEL and LO_DIV_SEL as:

TX_DIV_SEL / LO_DIV_SEL	TX_DIV / LO_DIV	FREQUENCY RANGE
TX_DIV_SEL = 0	TX DIV = 1	2050 MHz ≤ f_{TX} ≤ 4100 MHz
TX_DIV_SEL = 1	TX DIV = 2	1025 MHz ≤ f_{TX} ≤ 2050 MHz
TX_DIV_SEL = 2	TX DIV = 4	512.5 MHz ≤ f_{TX} ≤ 1025 MHz
TX_DIV_SEL = 3	TX DIV = 8	256.25 MHz ≤ f_{TX} ≤ 512.5 MHz
LO_DIV_SEL = 0	LO DIV = 1	2050 MHz ≤ f_{LO} ≤ 4100 MHz
LO_DIV_SEL = 1	LO DIV = 2	1025 MHz ≤ f_{LO} ≤ 2050 MHz
LO_DIV_SEL = 2	LO DIV = 4	512.5 MHz ≤ f_{LO} ≤ 1025 MHz
LO_DIV_SEL = 3	LO DIV = 8	256.25 MHz ≤ f_{LO} ≤ 512.5 MHz

b. **PLL_DIV_SEL**

Given f_{VCO}, select PLL_DIV_SEL so that the division ratio PLL DIV limits the input frequency to the prescaler , f_{DMP}, is limited to a maximum of 3000 MHz.

PLL DIV = min(1, 2, 4) such that $f_{DMP} \le 3000$ MHz

PLL DIV is related to PLL_DIV_SEL according to the following equation:

$\text{PLL\_DIV} = 2^{\text{PLL\_DIV\_SEL}}$

This calculation can be restated as Equation 6.

$$\text{PLL DIV} = \text{Ceiling}\left(\frac{\text{LO DIV} \times f_{LO}}{3000\ \text{MHz}}\right) = \text{Ceiling}\left(\frac{\text{TX DIV} \times f_{TX}}{3000\ \text{MHz}}\right) \tag{6}$$

For both integer and fractional mode it is preferable to operate the f_{PFD} at the highest possible frequency determined by the required frequency step of the RFOUT or LO_OUT. In Integer mode, select the maximum f_{PFD} according to Equation 7.

$$f_{PFD} = \frac{f_{VCO,\ Stepsize}}{\text{PLL DIV}} = \frac{f_{TX,\ Stepsize} \times \text{TX DIV}}{\text{PLL DIV}} \tag{7}$$

In Fractional mode, small RF stepsize can be obtained through the fractional divider. In this case, the highest f_{PFD} frequency should be selected according to the reference clock and system requirements.

c. **RDIV, NINT, NFRAC, PRSC_SEL**

The remaing PLL parameters are calculated according to the following equations:

$$\text{RDIV} = \frac{f_{\text{REF}}}{f_{\text{PFD}}}$$

$$\text{NINT} = \text{floor}\left(\frac{f_{\text{VCO}} \text{ x RDIV}}{f_{\text{REF}} \text{ x PLL DIV}}\right)$$

$$\text{NFRAC} = \text{floor}\left[\left(\left(\frac{f_{\text{VCO}} \text{ x RDIV}}{f_{\text{REF}} \text{ x PLL DIV}}\right) - \text{NINT}\right) \text{x } 2^{25}\right]$$

The DMP division ratio (P/P+1) can be set to 4/5 or 8/9 through the PRSC_SEL bit. To allow proper fractional operation, set PRSC_SEL according to:

PRSC_SEL = 0, (P/P+1) = 4/5 for 20 ≤ NINT < 72 in integer mode or 23 ≤ NINT < 75 in fractional mode.

PRSC_SEL = 1, (P/P+1) = 8/9 for NINT ≥ 72 in integer mode or NINT ≥ 75 in fractional mode.

The PRSC_SEL limit at NINT < 75 applies to Fractional mode with third-order modulation. In Integer mode, the PRSC_SEL = 8/9 should be used with NINT as low as 72. The divider block accounts for either value of PRSC_SEL without requiring NINT or NFRAC to be adjusted. Then, calculate the maximum input frequency (f_N) to the digital divider. Use the lower of the possible prescaler divide settings, P = (4,8), as shown by Equation 8.

$$f_N = \frac{f_{\text{VCO}}}{\text{PLL DIV x P}} \tag{8}$$

Verify that the frequency into the digital divider, f_N, is less than or equal to 375 MHz. If f_N exceeds 375 MHz, choose a larger value for PLL_DIV_SEL and recalculate f_{PFD}, RDIV, NINT, NFRAC, and PRSC_SEL.

8.4.2 Setup Example for Integer Mode

Suppose the following operating characteristics fractional example are desired for Integer mode operation:

- f_{REF} = 61.44 MHz (reference input frequency)
- Step at RF = 2.56 MHz (RF channel spacing)
- f_{RF} = 1799.68 MHz (RF frequency)

The VCO range is 2050 MHz to 4100 MHz. Therefore:

- LO DIV = 2 (LO_DIV_SEL = 1)
- f_{VCO} = LO DIV × 1799.68 MHz = 3599.36 MHz

In order to keep the frequency of the prescaler below 3000 MHz:

- PLL_DIV = 2 (PLL_DIV_SEL = 1)

The desired stepsize at RF is 2.56 MHz, so:

- f_{PFD} = 2.56 MHz
- f_{VCO}, stepsize = PLL_DIV × f_{PFD} = 5.12 MHz

Using the reference frequency along with the required f_{PFD} gives:

- RDIV = 24
- NINT = 703

NINT ≥ 75; therefore, select the 8/9 prescaler.

f_N = 3599.36 MHz/(2 × 8) = 224.96 MHz < 375 MHz

This example shows that Integer mode operation gives sufficient resolution for the required stepsize.

8.4.3 Integer and Fractional Mode Selection

The PLL is designed to operate in either Integer mode or Fractional mode. If the desired local oscillator (LO) frequency is an integer multiple of f_{PFD}, then select integer mode otherwise select fractional mode. In Integer mode, the feedback divider ratio is an integer, and the fraction is zero. Thus, bits corresponding to the fractional control in integer mode are *don’t care* and fractional divider functionality is disabled.

In Fractional mode, the accuracy of the final frequency is set by 25-bit resolution. The RF stepsize is $f_{PFD}/2^{25}$ which is less than 1 Hz for f_{PFD} up to 33 MHz. The appropriate fractional control bits in the serial register must be programmed. Optimal performance may require tuning the MOD_ORD, ISOURCE_SINK, and ISOURCE_TRIM values according to the chosen frequency band.

8.4.4 Selecting the VCO and VCO Frequency Control

To achieve a broad frequency tuning range, the TRF3722 integrates multiple VCOs. Each VCO tank uses a bank of coarse tuning capacitor to bring VCO frequency within a few MHz of the desired value. For a given LO frequency an appropriate VCO and capacitor array must be selected. The device integrates logic that automatically selects an appropriate VCO and capacitor array, such that in closed loop $V_{(TUNE)}$ is approximately equal to the open loop calibration reference voltage set by VCO_CAL_REF. An on-chip temperature sensor automatically adjusts this reference voltage so that proper lock can be maintained over the temperature range.

The calibration logic is driven by a CAL_CLK signal which is scaled version of the reference frequency according to CAL_CLK_SEL. For optimum accuracy It is recommended to limit the CAL_CLK frequency to 600 kHz.

When VCO_SEL_MODE is '0', the device automatically selects the VCO and the capacitor array. When VCO_SEL_MODE is '1', the VCO selected by VCO_SEL is used and the logic automatically selects the capacitor array. The VCO and capacitor array settings resulting from the calibration can be read from Register 0 - read back register.

Automatic calibration can be disabled by setting CAL_BYPASS to '1'. In this manual calibration mode, the VCO is selected through register bits VCO_SEL, while the capacitor array is selected through register bits VCO_TRIM. Calibration modes are summarized in Table 3.

Table 3. VCO Calibration Modes

CAL_BYPASS	VCO_SEL_MODE	MAX CYCLES CAL_CLK	VCO	CAPACITOR ARRAY
0	0	46	Automatic	
0	1	34	VCO_SEL	Automatic
1	*don't care*	N/A	VCO_SEL	VCO_TRIM

8.5 Register Maps

Table 4. Serial interface Register Summary

Bit	Register 1	Register 2	Register 3	Register 4	Register 5	Register 6
Bit0	Register Address	Register Address	Register Address	Register Address	Register Address	Register Address
Bit1						
Bit2						
Bit3						
Bit4						
Bit5	RDIV	NINT	NFRAC	PWD_PLL	RSV	RSV
Bit6				PWD_CP	IB_MOD_GM	
Bit7				PWD_VCO		VCO_TRIM
Bit8				PWD_VCO_MUX	IB_MOD_LO	
Bit9				PWD _DIV124		
Bit10				PWD_PRESC	VCO_BIAS	
Bit11				RSV		
Bit12				PWD_OUTBUF		
Bit13				PWD_LO_DIV		EN_LOCKDET
Bit14				PWD_TX_DIV	VCOBUF_BIAS	VCO_TEST_MODE
Bit15				PWD_MOD		CAL_BYPASS
Bit16				EN_EXTVCO	VCOMUX_BIAS	MUX_CTRL
Bit17				RSV		
Bit18	RSV			EN_ISOURCE	OUTBUF_BIAS	
Bit19	REF_INV			LD_ANA_PREC		ISOURCE_SINKB
Bit20	NEG_VCO				RSV	ISOURCE_TRIM
Bit21	ICP	PLL_DIV_SEL		CP_TRISTATE		
Bit22					VCO_CAL_IB	
Bit23		PRSC_SEL		SPEEDUP	VCO_CAL_REF	LO_DIV_SEL
Bit24		RSV		LD_DIG_PREC		
Bit25				MOD_ORD		LO_DIV_BIAS
Bit26	ICPDOUBLE	VCO_SEL			VCO_AMPL_CTRL	
Bit27	CAL_CLK_SEL					TX_DIV_SEL
Bit28		VCO_SEL_MODE		DITH_SEL	VCO_VB_CTRL	
Bit29		CAL_ACC		DEL_SD_CLK		TX_DIV_BIAS
Bit30			RSV		RSV	
Bit31	RSV	EN_CAL		EN_FRAC_MODE	EN_LD_ISOURCE	GAIN_CTRL

8.5.1 Serial interface Register Definition

Table 5. Register 1

Register 1	Bit Name	Reset Value	Description
Bit0	ADDR<0>	1	Register Address Bits
Bit1	ADDR<1>	0	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	
Bit4	ADDR<4>	0	
Bit5	RDIV<0>	1	13-bit Reference Divider Value (Rmin = 1, Rmax = 8191)
Bit6	RDIV<1>	0	
Bit7	RDIV<2>	0	
Bit8	RDIV<3>	0	
Bit9	RDIV<4>	0	
Bit10	RDIV<5>	0	
Bit11	RDIV<6>	0	
Bit12	RDIV<7>	0	
Bit13	RDIV<8>	0	
Bit14	RDIV<9>	0	
Bit15	RDIV<10>	0	
Bit16	RDIV<11>	0	
Bit17	RDIV<12>	0	
Bit18	RSV	0	Reserved
Bit19	REF_INV	0	Invert Reference Clock Polarity; 1 = use falling edge
Bit20	NEG_VCO	1	VCO polarity control; 1 = negative slope (negative Kv)
Bit21	ICP<0>	0	Program charge pump DC current: [00000] = 1.94 mA [11111] = 0.47 mA [01010] = 0.97 mA
Bit22	ICP<1>	1	
Bit23	ICP<2>	0	
Bit24	ICP<3>	1	
Bit25	ICP<4>	0	
Bit26	ICPDOUBLE	0	1 = Set ICP to double the current
Bit27	CAL_CLK_SEL<0>	0	Multiplication or division factor to create VCO calibration clock from the PFD frequency: [0000] = Fastest (Rdiv / 128) [1111] = Slowest (Rdiv x 128), [1000] = Default (1x Rdiv)
Bit28	CAL_CLK_SEL<1>	0	
Bit29	CAL_CLK_SEL<2>	0	
Bit30	CAL_CLK_SEL<3>	1	
Bit31	RSV	0	Reserved

CAL_CLK_SEL[3..0]: Set the frequency divider value used to derive the VCO calibration clock from the reference frequency.

Table 6. CAL_CLK_SEL Scaling Factor Setting

CAL_CLK_SEL	Scaling Factor	CAL_CLK_SEL	Scaling Factor
1111	1/128	0111	NA
1110	1/64	0110	2
1101	1/32	0101	4
1100	1/16	0100	8
1011	1/8	0011	16
1010	1/4	0010	32
1001	1/2	0001	64
1000	1	0000	128

ICP[4..0]: Set the charge pump current.

Table 7. Charge Pump Current Set-Point

ICP[4..0]	Current (mA)	ICP[4..0]	Current (mA)
00 000	1.94	10 000	0.75
00 001	1.76	10 001	0.72
00 010	1.62	10 010	0.69
00 011	1.49	10 011	0.67
00 100	1.38	10 100	0.65
00 101	1.29	10 101	0.63
00 110	1.21	10 110	0.61
00 111	1.14	10 111	0.59
01 000	1.08	11 000	0.57
01 001	1.02	11 001	0.55
01 010	0.97	11 010	0.54
01 011	0.92	11 011	0.52
01 100	0.88	11 100	0.51
01 101	0.84	11 101	0.50
01 110	0.81	11 110	0.48
01 111	0.78	11 111	0.47

Table 8. Register 2

Register 2	Bit Name	Reset Value	Description
Bit0	ADDR<0>	0	Register Address Bits
Bit1	ADDR<1>	1	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	
Bit4	ADDR<4>	0	
Bit5	NINT<0>	0	PLL N-Divider Value
Bit6	NINT<1>	0	
Bit7	NINT<2>	0	
Bit8	NINT<3>	0	
Bit9	NINT<4>	0	
Bit10	NINT<5>	0	
Bit11	NINT<6>	0	
Bit12	NINT<7>	1	
Bit13	NINT<8>	0	
Bit14	NINT<9>	0	
Bit15	NINT<10>	0	
Bit16	NINT<11>	0	
Bit17	NINT<12>	0	
Bit18	NINT<13>	0	
Bit19	NINT<14>	0	
Bit20	NINT<15>	0	
Bit21	PLL_DIV_SEL<0>	1	Select division ratio of divider in front of prescaler [00] = 1X, [01] = div2, [10] = div4
Bit22	PLL_DIV_SEL<1>	0	
Bit23	PRSC_SEL	1	Select precaler modulus: [0] = 4/5, [1] =8/9
Bit24	RSV	0	Reserved
Bit25	RSV	0	
Bit26	VCO_SEL<0>	0	Selects between the four integrated VCOs [00] = lowest frequency, [11] = highest frequency
Bit27	VCO_SEL<1>	1	
Bit28	VCO_SEL_MODE	0	Single VCO auto-calibration mode: [1] = active
Bit29	CAL_ACC<0>	0	Error count during the cap array calibration [00] = 0, [01] = 1/32, [10] = 1/64, [11] =1/128)
Bit30	CAL_ACC<1>	0	
Bit31	EN_CAL	0	Initiate VCO auto-calibration, resets automatically

Table 9. Register 3

Register 3	Bit Name	Reset Value	Description
Bit0	ADDR<0>	1	Register Address Bits
Bit1	ADDR<1>	1	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	
Bit4	ADDR<4>	0	
Bit5	NFRAC<0>	0	Fractional PLL N-Divider 0 to 0.99999 in fractional mode
Bit6	NFRAC<1>	0	
Bit7	NFRAC<2>	0	
Bit8	NFRAC<3>	0	
Bit9	NFRAC<4>	0	
Bit10	NFRAC<5>	0	
Bit11	NFRAC<6>	0	
Bit12	NFRAC<7>	0	
Bit13	NFRAC<8>	0	
Bit14	NFRAC<9>	0	
Bit15	NFRAC<10>	0	
Bit16	NFRAC<11>	0	
Bit17	NFRAC<12>	0	
Bit18	NFRAC<13>	0	
Bit19	NFRAC<14>	0	
Bit20	NFRAC<15>	0	
Bit21	NFRAC<16>	0	
Bit22	NFRAC<17>	0	
Bit23	NFRAC<18>	0	
Bit24	NFRAC<19>	0	
Bit25	NFRAC<20>	0	
Bit26	NFRAC<21>	0	
Bit27	NFRAC<22>	0	
Bit28	NFRAC<23>	0	
Bit29	NFRAC<24>	0	
Bit30	RSV	0	Reserved
Bit31	RSV	0	

Table 10. Register 4

Register 4	Bit Name	Reset Value	Description
Bit0	ADDR<0>	0	Register Address Bits
Bit1	ADDR<1>	0	
Bit2	ADDR<2>	1	
Bit3	ADDR<3>	1	
Bit4	ADDR<4>	0	
Bit5	PWD_PLL	0	Power -down all PLL blocks: (1 = off)
Bit6	PWD_CP	0	Power-down Charge Pump: (1=off)
Bit7	PWD_VCO	0	Power-down VCO: (1=off)
Bit8	PWD_VCO_MUX	0	Power-down VCO Mux blocks: (1=off)
Bit9	PWD _DIV124	0	Power-down the div 1,2,4 in the PLL f/b path: (1=off)
Bit10	PWD_PRESC	0	Power-down Prescaler: (1=off)
Bit11	RSV	1	Reserved
Bit12	PWD_OUTBUF	1	Power-down Ouptut Buffer: (1=off)
Bit13	PWD_LO_DIV	1	Power-down LO divider block: (1=off)
Bit14	PWD_TX_DIV	1	Power-down TX divider block: (1=off)
Bit15	PWD_MOD	1	Power-down modulator block: (1=off)
Bit16	EN_EXTVCO	0	Enable external VCO input buffer: (1 = enabled)
Bit17	RSV	0	Reserved
Bit18	EN_ISOURCE	0	Enable offset current at CP output (frac-n mode only).
Bit19	LD_ANA_PREC<0>	0	Control precision of Analog Lock Detector: [00] = H/H (High), [01] = L/L (Low), [10] = H/L , [11] = L/L
Bit20	LD_ANA_PREC<1>	0	
Bit21	CP_TRISTATE<0>	0	Set the charge pump output in Tristate mode: [00] = Off, [01] = Down, [10] = Up, [11] = Tristate
Bit22	CP_TRISTATE<1>	0	
Bit23	SPEEDUP	0	Enable fast turn on/off time of bias blocks.
Bit24	LD_DIG_PREC	0	Lock detector precision (increases sampling time if set to 1)
Bit25	MOD_ORD<0>	1	Modulator order (1-4). Not used in integer mode (defaul 3rd order + dither)
Bit26	MOD_ORD<1>	0	
Bit27	MOD_ORD<2>	1	
Bit28	DITH_SEL	0	Dither Mode: [0] = pseudo-random, [1] = constant
Bit29	DEL_SD_CLK<0>	0	DS modulator clock delay. Frac-n mode only. [00] = Min delay, [11] = max delay
Bit30	DEL_SD_CLK<1>	1	
Bit31	EN_FRAC_MODE	0	Enable Frac-n mode when set to 1

Table 11. Register 5

Register 5	Bit Name	Reset Value	Description
Bit0	ADDR<0>	1	Register Address Bits
Bit1	ADDR<1>	0	
Bit2	ADDR<2>	1	
Bit3	ADDR<3>	1	
Bit4	ADDR<4>	0	
Bit5	RSV	0	Reserved
Bit6	IB_MOD_GM<0>	0	Adjust modulator bias current gm
Bit7	IB_MOD_GM<1>	1	
Bit8	IB_MOD_LO<0>	0	Adjust modulator BB and LO bias current
Bit9	IB_MOD_LO<1>	1	
Bit10	VCO_BIAS<0>	0	Adjust VCO bias reference current
Bit11	VCO_BIAS<1>	0	
Bit12	VCO_BIAS<2>	0	
Bit13	VCO_BIAS<3>	1	
Bit14	VCOBUF_BIAS<0>	0	Adjust VCO buffer reference current
Bit15	VCOBUF_BIAS<1>	1	
Bit16	VCOMUX_BIAS<0>	0	Adjust VCO Mux reference current
Bit17	VCOMUX_BIAS<1>	1	
Bit18	OUTBUF_BIAS<0>	0	Adjust output buffer current
Bit19	OUTBUF_BIAS<1>	1	
Bit20	RSV	0	Reserved
Bit21	RSV	1	
Bit22	VCO_CAL_IB	0	Bias current for CAL reference voltage: [0] = PTAT, [1] = Constant
Bit23	VCO_CAL_REF<0>	0	VCO calibration reference voltage adjustment [000] = 0.9 V, [111] = 1.4 V [011] = recommended = 1.11 V
Bit24	VCO_CAL_REF<1>	0	
Bit25	VCO_CAL_REF<2>	1	
Bit26	VCO_AMPL_CTRL<0>	0	Adjusts the signal level at the VCO_MUX input: [00] =max, [11] = min
Bit27	VCO_AMPL_CTRL<1>	1	
Bit28	VCO_VB_CTRL<0>	0	Adjusts the VCO core bias voltage: [00] = 1.2 V, [01] = 1.35 V, [10] = 1.5 V, [11] = 1.65 V
Bit29	VCO_VB_CTRL<1>	1	
Bit30	RSV	0	Reserved
Bit31	EN_LD_MON_ISOURCE	1	Enable monitoring of LD to turn on Isource; recommend [0] = Isource ctrl

Table 12. Register 6

Register 6	Bit Name	Reset Value	Description
Bit0	ADDR<0>	0	Register Address Bits
Bit1	ADDR<1>	1	
Bit2	ADDR<2>	1	
Bit3	ADDR<3>	1	
Bit4	ADDR<4>	0	
Bit5	RSV	0	Reserved
Bit6	RSV	0	
Bit7	VCO_TRIM<0>	0	VCO capacitor array control bits; used in manual cal mode
Bit8	VCO_TRIM<1>	0	
Bit9	VCO_TRIM<2>	0	
Bit10	VCO_TRIM<3>	0	
Bit11	VCO_TRIM<4>	0	
Bit12	VCO_TRIM<5>	1	
Bit13	EN_LOCKDET	0	Enable monitor of lock detector output for autocal mode
Bit14	VCO_TEST_MODE	0	Counter mode, measure max and min freq for each VCO
Bit15	CAL_BYPASS	0	Bypass auto-cal; sets VCO_SEL and VCO_TRIM from Serial interface
Bit16	MUX_CTRL<0>	1	Select signal for test output: [001] = LD, [010] = NDIV, [100] = RDIV, [110] = A_counter
Bit17	MUX_CTRL<1>	0	
Bit18	MUX_CTRL<2>	0	
Bit19	ISOURCE_SINKB	0	Offset current polarity
Bit20	ISOURCE_TRIM<0>	0	Adjust Isource bias current in frac-n mode.
Bit21	ISOURCE_TRIM<1>	0	
Bit22	ISOURCE_TRIM<2>	1	
Bit23	LO_DIV_SEL<0>	0	Adjust LO path divider: [00] = Div/1, [01] = Div/2, [10] = Div/4. [11] = Div/8
Bit24	LO_DIV_SEL<1>	0	
Bit25	LO_DIV_BIAS<0>	0	Adjust LO divider bias current: [00] = 25 uA, [01] = 37.5 uA, [10] = 50 uA, [11] = 62.5 uA
Bit26	LO_DIV_BIAS<1>	1	
Bit27	TX_DIV_SEL<0>	0	Adjust TX path divider.
Bit28	TX_DIV_SEL<1>	1	[00] = Div/1, [01] = Div/2, [10] = Div/4. [11] = Div/8
Bit29	TX_DIV_BIAS<0>	0	Adjust TX divider bias current: [00] = 25 uA, [01] = 37.5 uA, [10] = 50 uA, [11] = 62.5 uA
Bit30	TX_DIV_BIAS<1>	1	
Bit31	GAIN_CTRL	0	Modulator gain control: [0] = Default, [1] = High Gain

Table 13. READBACK Mode Summary Serial interface Map

Bit	Register 0		RDBK
Bit0	Register Address		Register Address
Bit1			
Bit2			
Bit3			
Bit4			
Bit5	CHIP_ID		N/C
Bit6			
Bit7	NU		
Bit8			
Bit9			
Bit10			
Bit11			
Bit12	R_SAT_ERR		
Bit13	COUNT	VCO_TRIM	
Bit14			
Bit15			
Bit16			
Bit17			
Bit18			
Bit19			
Bit20			
Bit21		VCO_SEL	
Bit22			
Bit23			
Bit24			
Bit25			
Bit26			
Bit27			MUX_COUNT
Bit28			RB_REG
Bit29			
Bit30			
Bit31	MUX_COUNT		RB_ENABLE

Table 14. Register 0 (Readback Only)

Register 0	Bit Name	Reset Value	Description
Bit0	ADDR<0>	0	Register Address Bits
Bit1	ADDR<1>	0	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	
Bit4	ADDR<4>	0	
Bit5	CHIP_ID<0>	1	Chip ID
Bit6	CHIP_ID<1>	0	
Bit7	NU	x	Not Used
Bit8	NU	x	
Bit9	NU	x	
Bit10	NU	x	
Bit11	NU	x	
Bit12	R_SAT_ERR	x	R-div saturation error for cal
Bit13	COUNT<0>/NU	x	VCO frequency counter high when MUX_COUNT = 0 and VCO_TEST_MODE = 1 VCO frequency counter low when MUX_COUNT = 1 and VCO_TEST_MODE = 1 Autocal results for VCO_TRIM and VCO_SEL when VCO_TEST_MODE = 0
Bit14	COUNT<1>/NU	x	
Bit15	COUNT<2>/VCO_TRIM<0>	x	
Bit16	COUNT<3>/VCO_TRIM<1>	x	
Bit17	COUNT<4>/VCO_TRIM<2>	x	
Bit18	COUNT<5>/VCO_TRIM<3>	x	
Bit19	COUNT<6>/VCO_TRIM<4>	x	
Bit20	COUNT<7>/VCO_TRIM<5>	x	
Bit21	COUNT<8>/VCO_SEL<0>	x	
Bit22	COUNT<9>/VCO_SEL<1>	x	
Bit23	COUNT<10>/VCO_SEL<2>	x	
Bit24	COUNT<11>	x	
Bit25	COUNT<12>	x	
Bit26	COUNT<13>	x	
Bit27	COUNT<14>	x	
Bit28	COUNT<15>	x	
Bit29	COUNT<16>	x	
Bit30	COUNT<17>	x	
Bit31	MUX_COUNT	x	[0] = max freq count, [1] = min freq count

Table 15. Register RDBK (Write Register for Readback)

RDBK	Bit Name	Reset Value	Description
Bit0	ADDR<0>	0	Register Address Bits
Bit1	ADDR<1>	0	
Bit2	ADDR<2>	0	
Bit3	ADDR<3>	1	
Bit4	ADDR<4>	0	
Bit5	N/C	0	
Bit6	N/C	0	
Bit7	N/C	0	
Bit8	N/C	0	
Bit9	N/C	0	
Bit10	N/C	0	
Bit11	N/C	0	
Bit12	N/C	0	
Bit13	N/C	0	
Bit14	N/C	0	
Bit15	N/C	0	
Bit16	N/C	0	
Bit17	N/C	0	
Bit18	N/C	0	
Bit19	N/C	0	
Bit20	N/C	0	
Bit21	N/C	0	
Bit22	N/C	0	
Bit23	N/C	0	
Bit24	N/C	0	
Bit25	N/C	0	
Bit26	N/C	0	
Bit27	MUX_COUNT	0	[0] = max freq count, [1] = min freq count
Bit28	RB_REG<0>	x	Three LSBs of the address for the register that is being read: [001] = Register 1 [110] = Register 6
Bit29	RB_REG<1>	x	
Bit30	RB_REG<2>	x	
Bit31	RB_ENABLE	1	Puts device in Readback mode

8.5.1.1 BIAS SETTINGS

Optimum TRF7322 bias settings used in the performance measurements are shown in Table 16.

Table 16. Register Settings With Optimized Bias Set Used in the Performance Measurement.

REGISTER	BITS	TYPICAL OPERATING MODE [256MHz-2GHz], INT MODE	TYPICAL OPERATING MODE [2GHz - 3GHz], INT MODE	TYPICAL OPERATING MODE [3GHz - 4.1GHz], INT MODE	LOW POWER MODE, INT MODE	FRACTIONAL MODE
REGISTER 1	RDIV	x	x	x	x	x
REGISTER 1	REF_INV	0	0	0	0	0
REGISTER 1	NEG_VCO	1	1	1	1	1
REGISTER 1	ICP	0	0	0	0	0
REGISTER 1	ICPDOUBLE	0	0	0	0	0
REGISTER 1	CAL_CLK_SEL	13	13	13	13	15
REGISTER 2	NINT	x	x	x	x	x
REGISTER 2	PLL_DIV_SEL	x	x	x	x	x
REGISTER 2	PRSC_SEL	x	x	x	x	x
REGISTER 2	VCO_SEL	x	x	x	x	x
REGISTER 2	VCO_SEL_MODE	x	x	x	x	x
REGISTER 2	CAL_ACC	0	0	0	0	0
REGISTER 2	EN_CAL	1	1	1	1	1
REGISTER 3	NFRAC	0	0	0	0	x
REGISTER 4	PWD_PLL	0	0	0	0	0
REGISTER 4	PWD_CP	0	0	0	0	0
REGISTER 4	PWD_VCO	0	0	0	0	0
REGISTER 4	PWD_VCO_MUX	0	0	0	0	0
REGISTER 4	PWD _DIV124	0	0	0	0	0
REGISTER 4	PWD_PRESC	0	0	0	0	0
REGISTER 4	PWD_OUTBUF	0	0	0	1	0
REGISTER 4	PWD_LO_DIV	0	0	0	1	0
REGISTER 4	PWD_TX_DIV	0	0	0	0	0
REGISTER 4	PWD_MOD	0	0	0	0	0
REGISTER 4	EN_EXTVCO	0	0	0	0	0
REGISTER 4	EN_ISOURCE	0	0	0	0	1
REGISTER 4	LD_ANA_PREC	0	0	0	0	3
REGISTER 4	CP_TRISTATE	0	0	0	0	0
REGISTER 4	SPEEDUP	0	0	0	0	0
REGISTER 4	LD_DIG_PREC	0	0	0	0	0
REGISTER 4	MOD_ORD	5	5	5	5	4
REGISTER 4	DITH_SEL	0	0	0	0	0
REGISTER 4	DEL_SD_CLK	2	2	2	2	0
REGISTER 4	EN_FRAC_MODE	0	0	0	0	1
REGISTER 5	IB_MOD_GM	3	3	2	0	3
REGISTER 5	IB_MOD_LO	0	1	0	0	0
REGISTER 5	VCO_BIAS	15	15	15	15	15
REGISTER 5	VCOBUF_BIAS	2	2	2	2	2
REGISTER 5	OUTBUF_BIAS	2	2	2	0	2
REGISTER 5	VCOMUX_BIAS	2	2	2	2	2
REGISTER 5	VCO_CAL_IB	0	0	0	0	0
REGISTER 5	VCO_CAL_REF	3	3	3	3	3
REGISTER 5	VCO_AMPL_CTRL	0	0	0	0	0
REGISTER 5	VCO_VB_CTRL	3	3	3	3	3
REGISTER 5	EN_LD_ISOURCE	0	0	0	0	0

Table 16. Register Settings With Optimized Bias Set Used in the Performance Measurement. (continued)

REGISTER	BITS	TYPICAL OPERATING MODE [256MHz-2GHz], INT MODE	TYPICAL OPERATING MODE [2GHz - 3GHz], INT MODE	TYPICAL OPERATING MODE [3GHz - 4.1GHz], INT MODE	LOW POWER MODE, INT MODE	FRACTIONAL MODE
REGISTER 6	VCO_TRIM	x	x	x	x	x
REGISTER 6	EN_LOCKDET	0	0	0	0	0
REGISTER 6	VCO_TEST_MODE	0	0	0	0	0
REGISTER 6	CAL_BYPASS	0	0	0	0	0
REGISTER 6	MUX_CTRL	1	1	1	1	5
REGISTER 6	ISOURCE_SINKB	0	0	0	0	0
REGISTER 6	ISOURCE_TRIM	4	4	4	4	7
REGISTER 6	LO_DIV_SEL	x	x	x	x	x
REGISTER 6	LO_DIV_BIAS	2	2	2	0	2
REGISTER 6	TX_DIV_SEL	x	x	x	x	x
REGISTER 6	TX_DIV_BIAS	1	1	1	0	1
REGISTER 6	GAIN_CTRL	0	0	0	0	0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

Figure 135 shows a typical application schematic for the TRF3722.

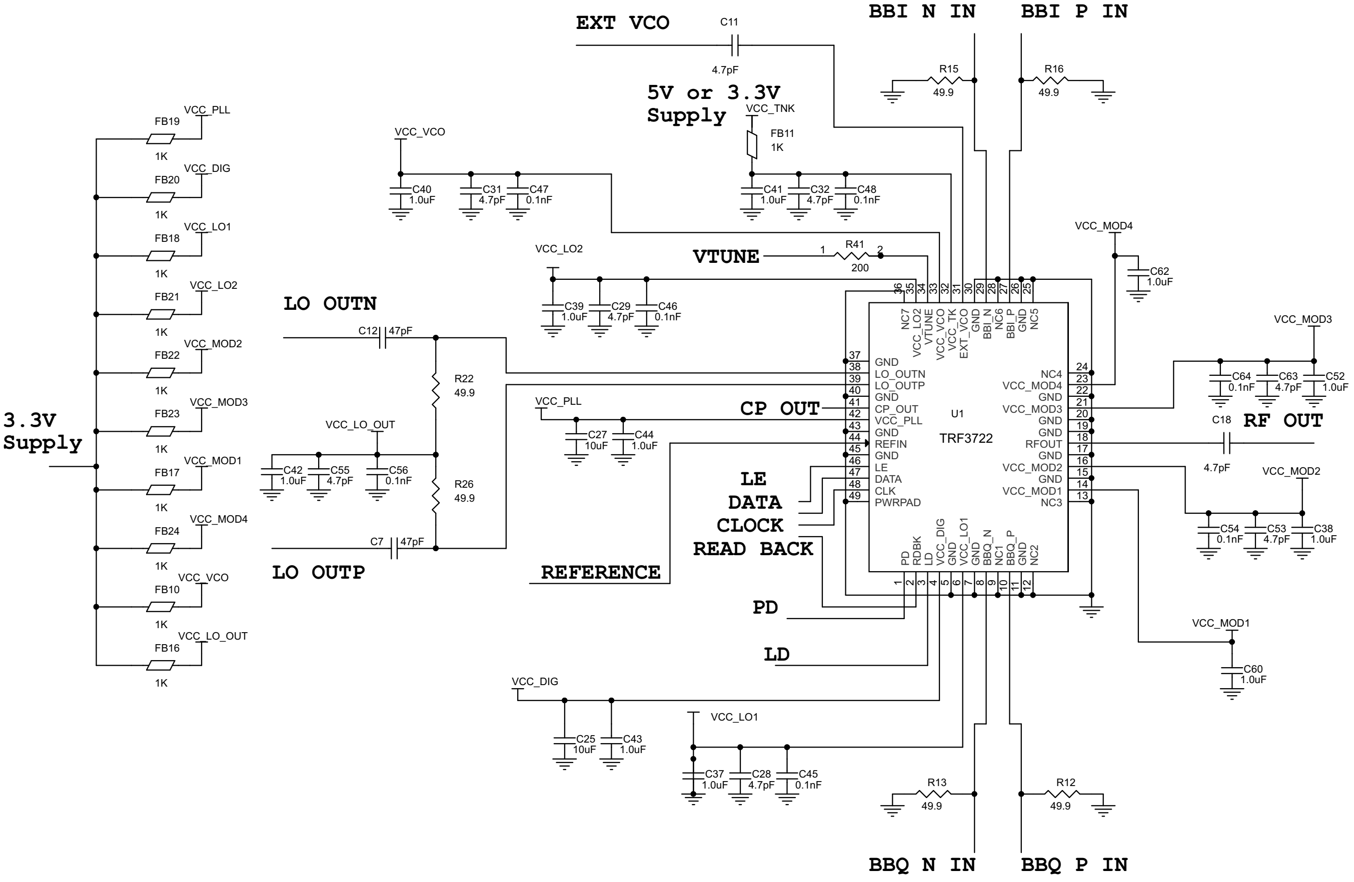


Figure 135. TRF3722 Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

Table 17 lists the pin termination requirements and interfacing for the circuit.

Table 17. Termination Requirements and Interfacing

PIN	NAME	DESCRIPTION
47	DATA	4WI data input: digital input, high impedance
2	RDBK	Readback output; digital output pins can source or sink up to 8 mA of current
3	LD	Lock detector digital output, as configured by MUX_CTRL
8,10,27,29	BBI_P, BBI_N, BBQ_P, BBQ_N	In-phase and quadrature baseband differential baseband signals. Typical 0.25V common mode is needed
18	RFOUT	Modulator RF output: must be ac-coupled and can drive 50 Ω load
31	EXT_VCO	External local oscillator input: high impedance, normally ac-coupled. If unused terminate to 50 ohms load
38,39	LO_OUTP, LO_OUTN	Local oscillator output: open-collector output. A pull-up resistor is LO_OUT required, normally ac-coupled.
44	REFIN	Reference clock input: high impedance, normally ac-coupled
46	LE	Serial interface latch enable: digital input, high impedance
48	CLK	Serial interface clock input: digital input, high impedance
47	DATA	Serial interface data input: digital input, high impedance

9.2.2 Detailed Design Procedures: DAC to Modulator Interface Network

Digital-to-analog converter (DAC) can interface directly with the TRF3722 modulator. The common-mode voltage of the DAC and the modulator baseband inputs should be properly maintained. With the proper interface network, the common-mode voltage of the DAC can be translated to the proper common-mode voltage of the modulator. The TRF3722 common-mode voltage is typically 0.25 V, and is ideally suited to interface with the DAC3482/3484 (DAC348x) and DAC38J8x family. The interface network is shown in Figure 136.

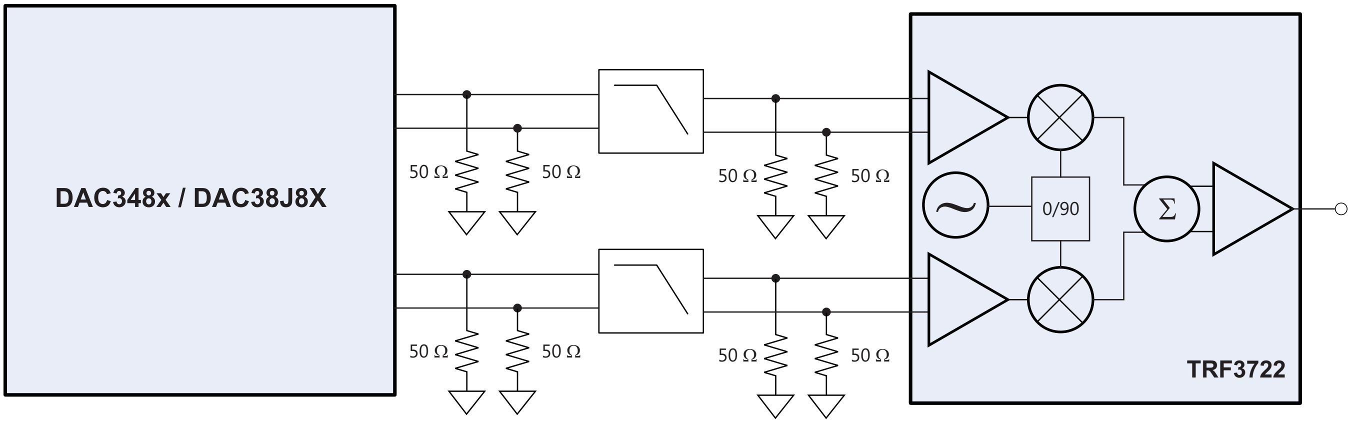


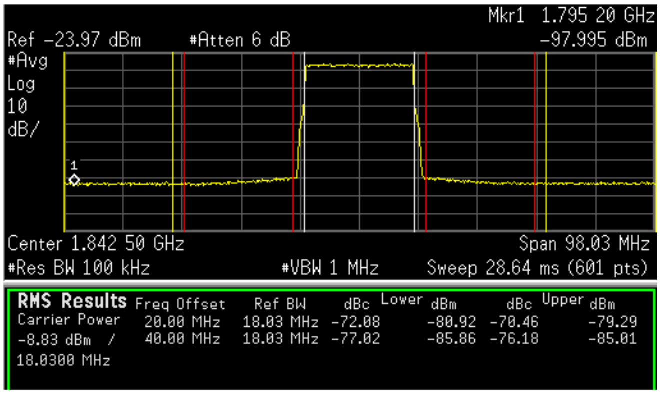
Figure 136. DAC348x Interface with the TRF3722 Modulator

The DAC348x requires a load resistance of 25 Ω per branch to maintain its optimum voltage swing of 1-V_{PP} differential with a 20-mA max current setting. The load of the DAC is separated into two parallel 50-Ω resistors placed on the input and output side of the low-pass filter. This configuration provides the proper resistive load to the DAC while also providing a convenient 50-Ω source and load termination for the filter.

9.2.3 Application Curves: DAC34H84 with TRF3722 Modulator Performance

The cascaded combination of the DAC34H84 and TRF3722 modulator yields excellent system parameters suitable for high-performance applications. Figure 137 and Figure 138 show 152.9 MHz IF adjacent channel power ratio (ACPR) performance.

- Mode integer
- PFD: 3.2 MHz
- Reference: 153.6 MHz
- LO = 1689.6 MHz
- IF = 152.9 MHz
- RF= 1842.5 MHz

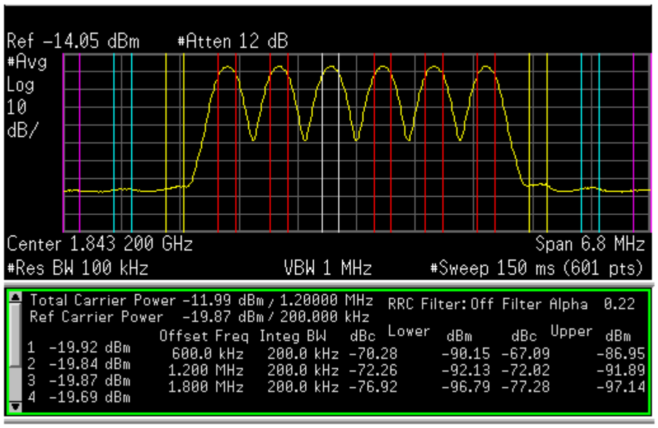


Mkr1 1.795 20 GHz
Ref -23.97 dBm #Atten 6 dB -97.995 dBm
Center 1.842 50 GHz Span 98.03 MHz
#Res BW 100 kHz #VBW 1 MHz Sweep 28.64 ms (601 pts)

RMS Results
Carrier Power
-8.83 dBm /
18.0300 MHz

Freq Offset	Ref BW	Lower dBc	Lower dBm	Upper dBc	Upper dBm
20.00 MHz	18.03 MHz	-72.08	-80.92	-70.46	-79.29
40.00 MHz	18.03 MHz	-77.02	-85.86	-76.18	-85.01

Figure 137. 152.9 MHz IF, DAC34H84 + TRF3722 20 MHz LTE ACPR



Ref -14.05 dBm #Atten 12 dB
Center 1.843 200 GHz Span 6.8 MHz
#Res BW 100 kHz VBW 1 MHz #Sweep 150 ms (601 pts)

Total Carrier Power -11.99 dBm / 1.20000 MHz RRC Filter: Off Filter Alpha 0.22
Ref Carrier Power -19.87 dBm / 200.000 kHz
1 -19.92 dBm
2 -19.84 dBm
3 -19.87 dBm
4 -19.69 dBm

Offset Freq	Integ BW	Lower dBc	Lower dBm	Upper dBc	Upper dBm
600.0 kHz	200.0 kHz	-70.28	-90.15	-67.09	-86.95
1.200 MHz	200.0 kHz	-72.26	-92.13	-72.02	-91.89
1.800 MHz	200.0 kHz	-76.92	-96.79	-77.28	-97.14

Figure 138. 152.9 MHz IF, 6 Carrier MC-GSM DAC34H84 + TRF3722 ACPR Performance

10 Power Supply Recommendations

The TRF3722 is powered by supplying a nominal 3.3 V and 5 V. It can also be powered using only 3.3V supply. Proper RF bypassing should be placed close to each power supply pin. Ground pin connections should have at least one ground via close to each ground pin to minimize ground inductance. The PowerPAD™ must be tied to ground, preferably with the recommended ground via pattern to provide a good thermal conduction path to the alternate side of the board and to provide a good RF ground for the device. (Refer to *Layout Guidelines* section for additional information.)

11 Layout

11.1 Layout Guidelines

Layout of the application board significantly impacts the analog performance of the TRF3722 device. Noise and high-speed signals should be prevented from leaking onto power-supply terminals or analog signals. The TRF3722 device is fitted with a ground slug on the back of the package that must be soldered to the printed circuit board (PCB) ground with adequate ground vias to ensure a good thermal and electrical connection. The ground pins of the device can be directly tied to the ground slug pad for a low-inductance path to ground. Additional ground vias may be added if space allows. Follow these recommendations:

- Place supply decoupling capacitors physically close to the device, on the same side of the board. Isolate supply terminals with a ferrite bead.
- Maintain a continuous ground plane in the vicinity of the device and as return paths for all high-speed signal lines. Place reference plane vias or decoupling capacitors near any signal line reference transition.
- Power planes should not overlap each other or high-speed signal lines.
- Isolate REFIN routing from loop filter lines, control lines, and other high-speed lines.

11.2 Layout Example

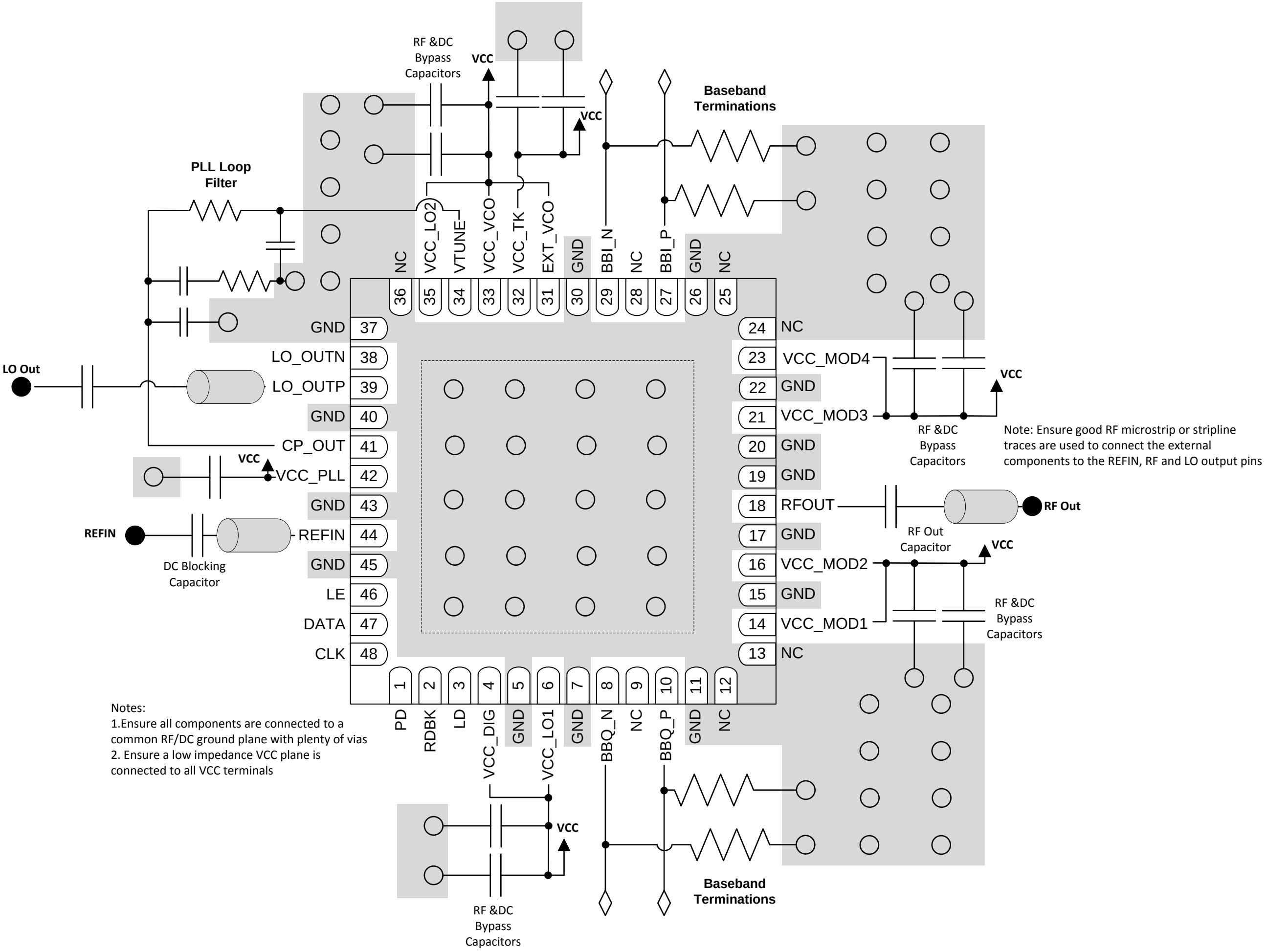


Figure 139. Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF3722IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRF3722 IRGZ	Samples
TRF3722IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRF3722 IRGZ	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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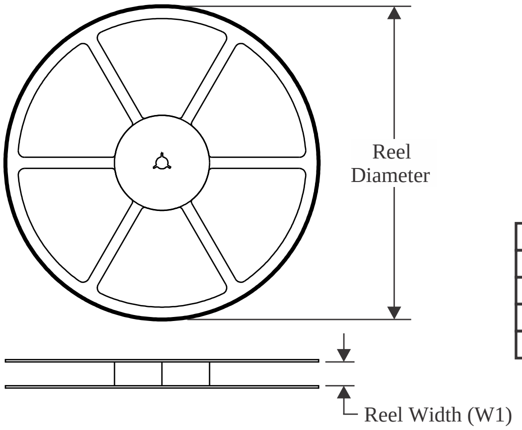
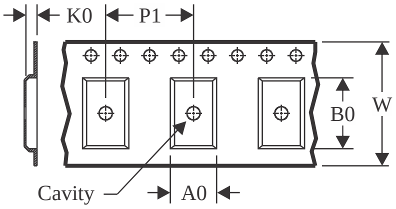
TAPE AND REEL INFORMATION

REEL DIMENSIONS

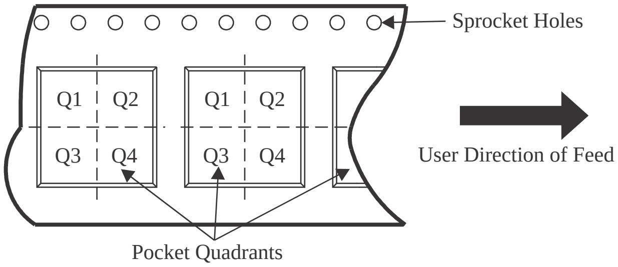


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

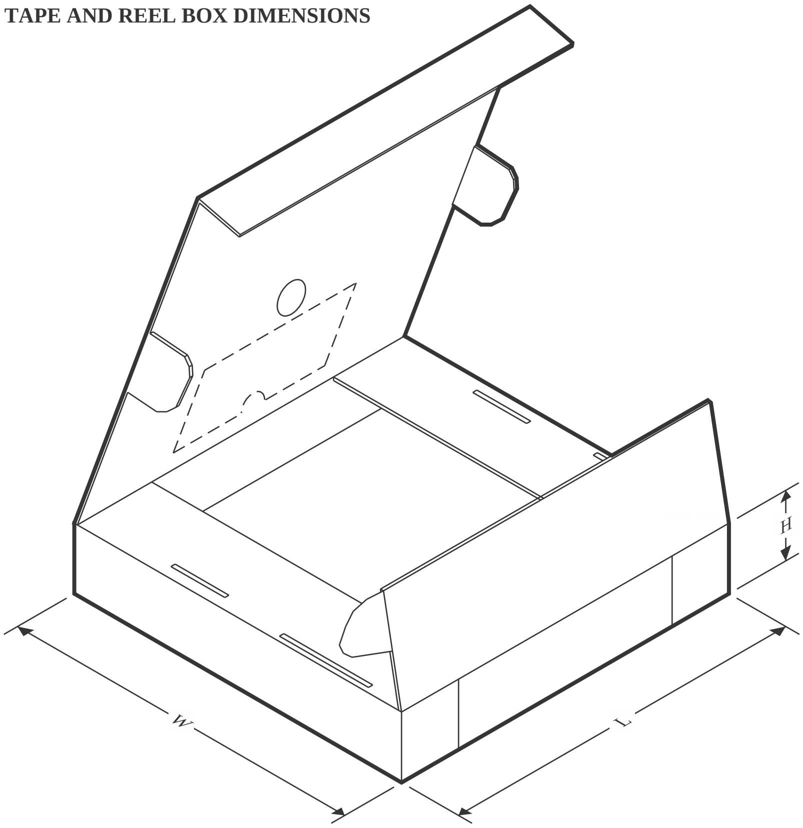
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF3722IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



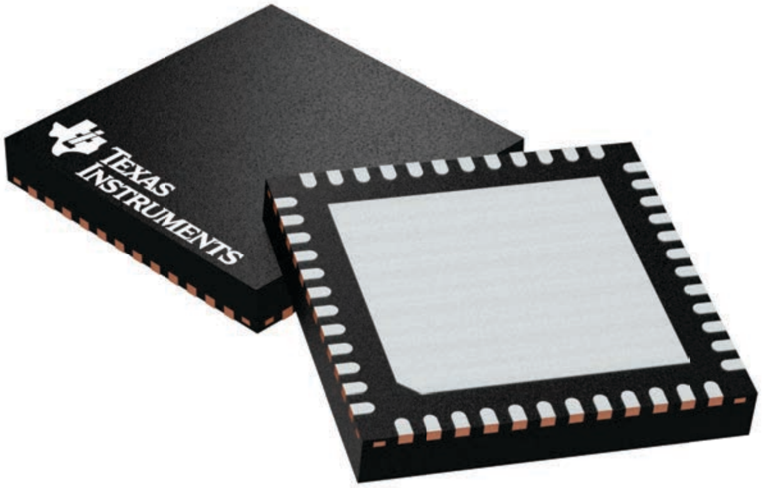
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF3722IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0

GENERIC PACKAGE VIEW

RGZ 48 **VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

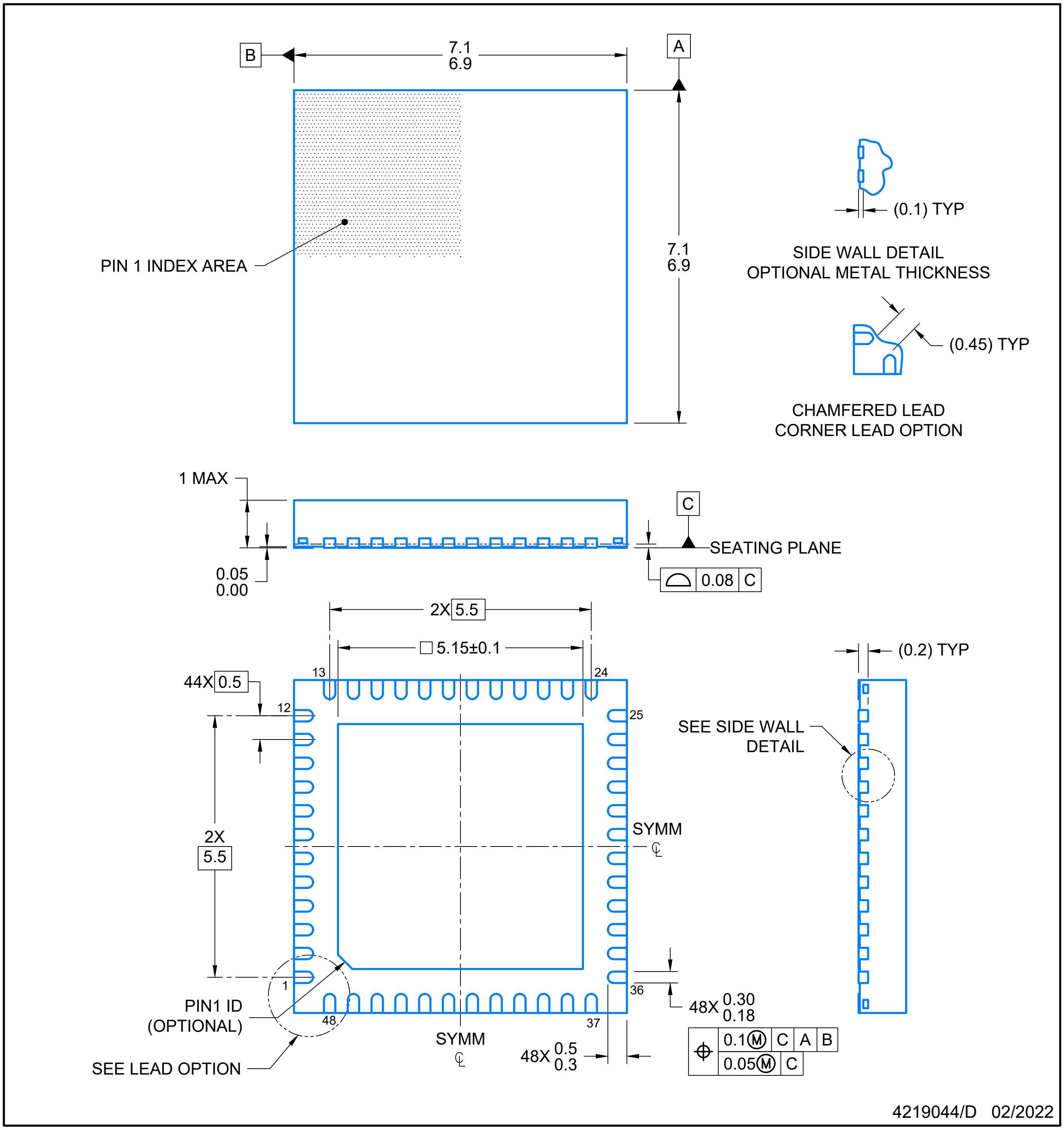
4224671/A

PACKAGE OUTLINE

RGZ0048A

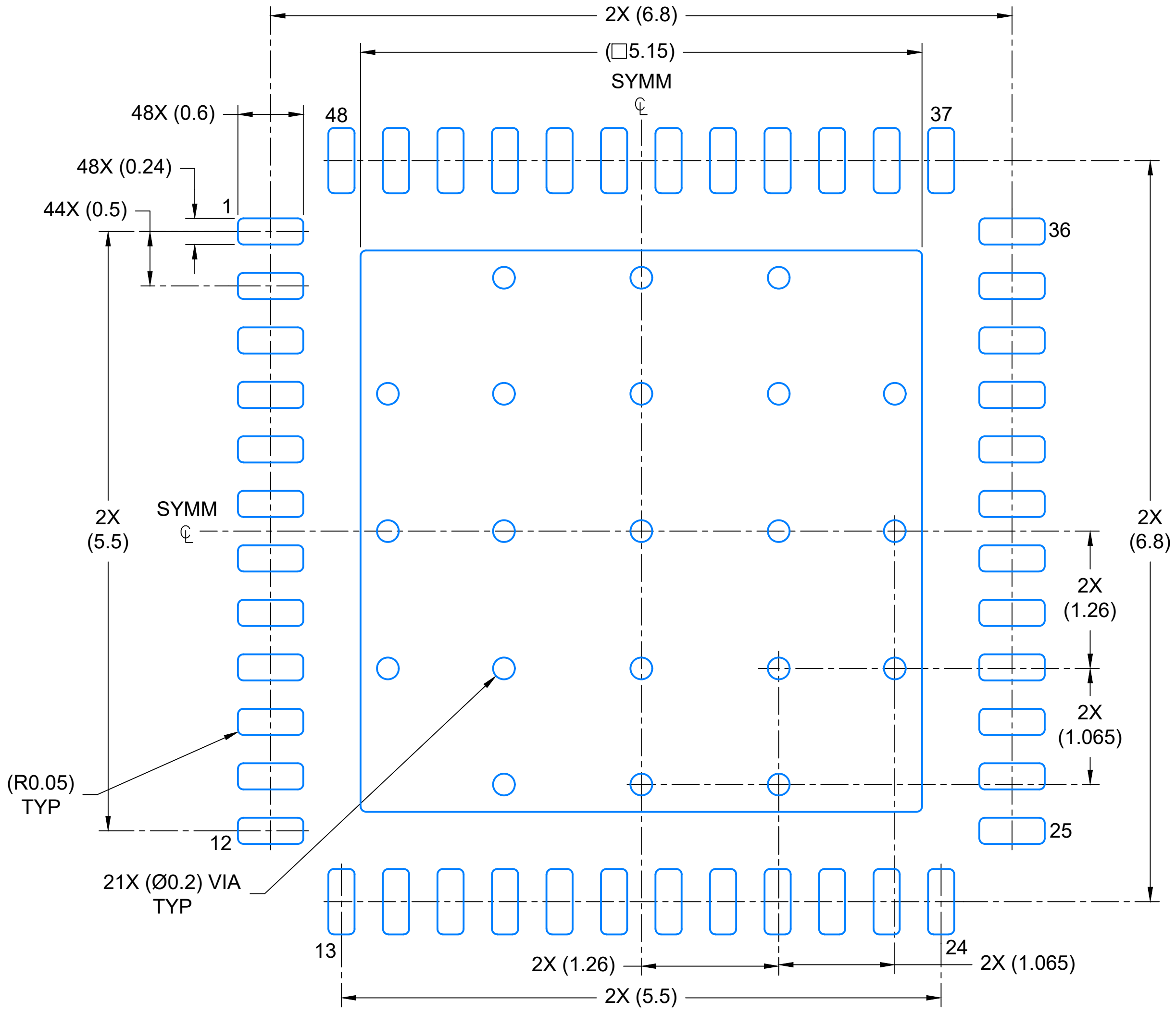
VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD

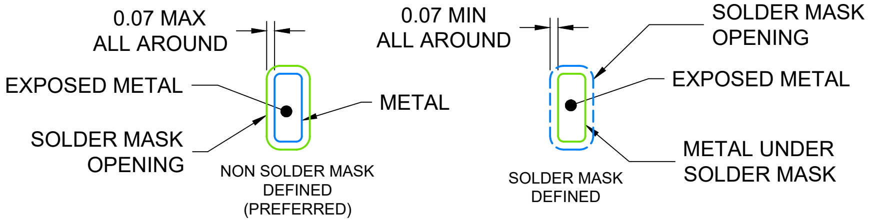


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X

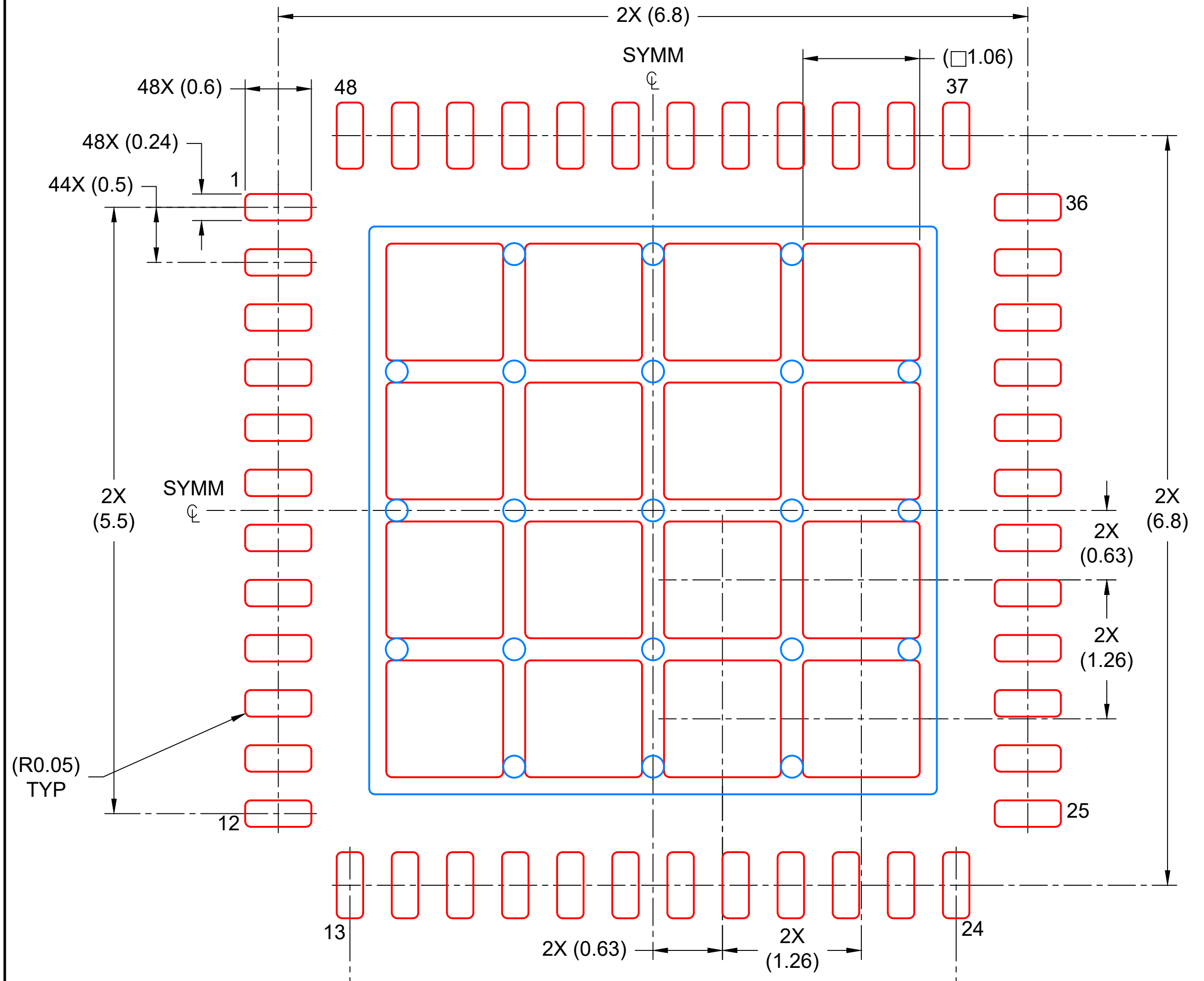


SOLDER MASK DETAILS

4219044/D 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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