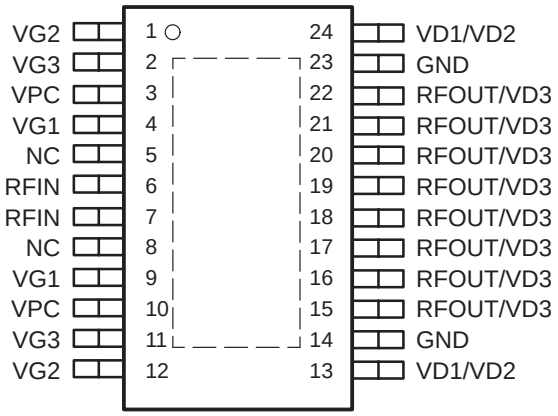
SLWS059B – MAY 1997 – REVISED AUGUST 1998

- **Single Positive Power Supply (No Negative Voltage Required)**
- **Advanced Silicon RFMOS™ Technology**
- **4.8-V Operation for GSM Applications**
- **35-dBm Typical Output Power**
- **30-dB Typical Power Gain**
- **40% Typical PAE with 5-dBm Input Power**
- **45% Typical PAE with 8-dBm Input Power**
- **Output Power Control**
- **Few External Components Required for Operation**
- **Thermally Enhanced Surface-Mount Package for Small Circuit Footprint**
- **Rugged, Sustains 20:1 Load Mismatch**
- **800-MHz to 1000-MHz Wide Operational Frequency Range**
- **Low Standby Current (<10 μA)**

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TRF7610 is a silicon MOSFET power amplifier IC for 900-MHz applications, tailored specifically for global systems for mobile communications (GSM). It uses Texas Instruments RFMOS™ process and consists of a three-stage amplifier with output power control. Few external components are required for operation.

The TRF7610 amplifies the RF signal from a preceding modulator and the upconverter stages in an RF section of a transmitter to a level that is sufficient for connection to the antenna. The RF input port, RFIN, and the RF output port, RFOUT, require simple external matching networks.

A control signal applied to the VPC input can ramp the RF output power up or down to meet ramp and spurious emission specifications for time-division multiple-access (TDMA) systems. The power control signal causes a change in output power as the voltage applied to VPC varies between 0 V and 3 V. With the RF input power applied to RFIN at 5 dBm, adjusting VPC from 0 V to 3 V increases the output power from a typical value of –43 dBm at VPC = 0 V to a typical value of 35 dBm at VPC = 3 V. Forward isolation with the RF input power applied to RFIN at 5 dBm, VPC = 0 V, is typically 48 dB.

The TRF7610 is available in a thermally enhanced, surface-mount, 24-pin PowerPAD™ (PWP) thin-shrink small-outline package (TSSOP). It is characterized for operation from –40°C to 85°C operating free-air temperature. In order to maintain acceptable thermal operating conditions, the device should be operated in pulse applications such as the GSM standard 1/8 duty cycle. The package has a solderable pad that improves the package thermal performance by bonding the pad to an external thermal plane. The pad also acts as a low-inductance electrical path to ground and must be electrically connected to the printed circuit-board (PCB) ground plane as a continuation of the regular package terminals that are designated GND.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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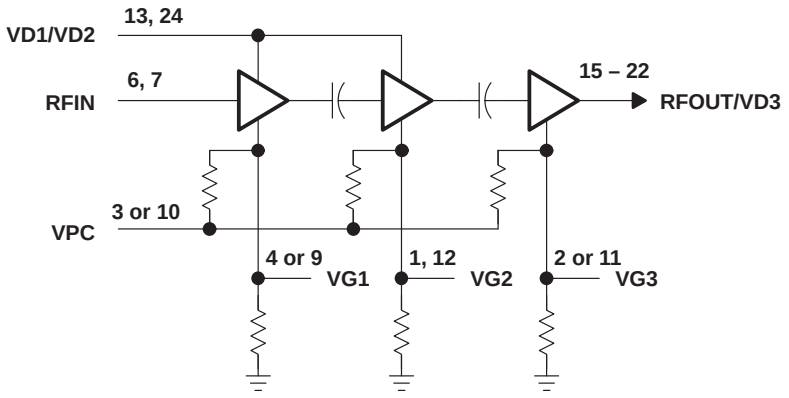
schematic



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	14, 23		Analog ground for all internal circuits. All signals are referenced to the ground terminals.
NC	5, 8		No internal connection. It is recommended that all NC terminals be connected to ground.
RFIN	6, 7	I	RF input. RFIN accepts signals between 800 MHz and 1000 MHz.
RFOUT/VD3	15, 16, 17, 18, 19, 20, 21, 22	I/O	RF output and third-stage drain bias. RFOUT requires an external matching network.
VG1	4, 9	I	First-stage gate bias set by resistor. Either terminal may be used or both may be connected externally.
VG2	1, 12	I	Second-stage gate bias set by resistor. These terminals must be connected externally.
VG3	2, 11	I	Third-stage gate bias set by resistor. Either terminal may be used or both may be connected externally.
VPC	3, 10	I	Voltage power control. VPC is a signal between 0 V and 3 V that adjusts the output power from a typical value of –43 dBm to 35 dBm. Either terminal may be used, or both may be connected externally.
VD1/VD2	13, 24	I	First- and second-stage drain bias. These terminals must be connected externally.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.6 V to 8 V
Input voltage range, VPC . . . . . –0.6 V to 4 V
Input power at RFIN . . . . . 13 dBm
Thermal resistance, junction to case, $R_{\theta JC}$ (see Note 2) . . . . . 3.5°C/W
Junction temperature, $T_J$max . . . . . 150°C
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to GND.
2. No air flow and with infinite heatsink

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage V_{DD} (see Note 1 and Note 3)	3.5	4.8	6	V
Operating free-air temperature, T_A	−40		85	°C
Operating frequency range (see Note 4)	800		1000	MHz

NOTES: 1. Voltage values are with respect to GND.
3 .Performance varies with drain voltage, see Figure 8.
4. External matching network dependent.

electrical characteristics over full range of recommended operating conditions

supply current, V_{DD} = 4.8 V

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{DD} Supply current	Operating at maximum output power	VPC = 3 V		2		A
	Operating with no RF input power	VPC = 0 V		<10		μA

† Typical values are at T_A = 25°C

GSM operation, V_{DD} = 4.8 V, VPC = 3 V, P_I = 5 dBm, T_A = 25°C (unless otherwise noted)‡

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating frequency range			870		925	MHz
Output power		VPC = 3 V	34	35	36	dBm
		VPC = 0 V		−43		
Power added efficiency (PAE)				40%		
		P_I = 8 dBm		45%		
Input return loss (externally matched, small signal)		P_I = −20 dBm		10		dB
Harmonics	$2f_0$	With external matching		−28		dBc
	$3f_0$	With external matching		−40		
Noise power in 30-kHz bandwidth	20 MHz above f_0			−88		dBm
	10 MHz above f_0			−88		
Ruggedness test		Frequency = 900 MHz, Load VSWR = 20:1, All phase angles		§		

‡ Specific applications circuit
§ No degradation in output power after test.

stability, GSM operation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Stability	Output VSWR¶ < 6:1 all phases, V_{DD} < 6 V, P_I = 5 dBm, P_O ≤ 35 dBm, Output frequency band: 200 MHz – 1200 MHz		No parasitic oscillations (all spurious < –70 dBc)		

¶ VSWR = voltage standing wave ratio

switching characteristics

GSM operation

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Switching time, RF output OFF to ON	VPC stepped from 0 V to 3 V		2		μs
t_{off}	Switching time, RF output ON to OFF	VPC stepped from 3 V to 0 V		2		μs

APPLICATION INFORMATION

In all cases, a capacitor must be connected from the positive power supply to ground as close to the terminals as possible for power-supply bypassing. The dc-blocking capacitors are required on the RF input and RF output. A list of components and their functions is shown in Table 1.

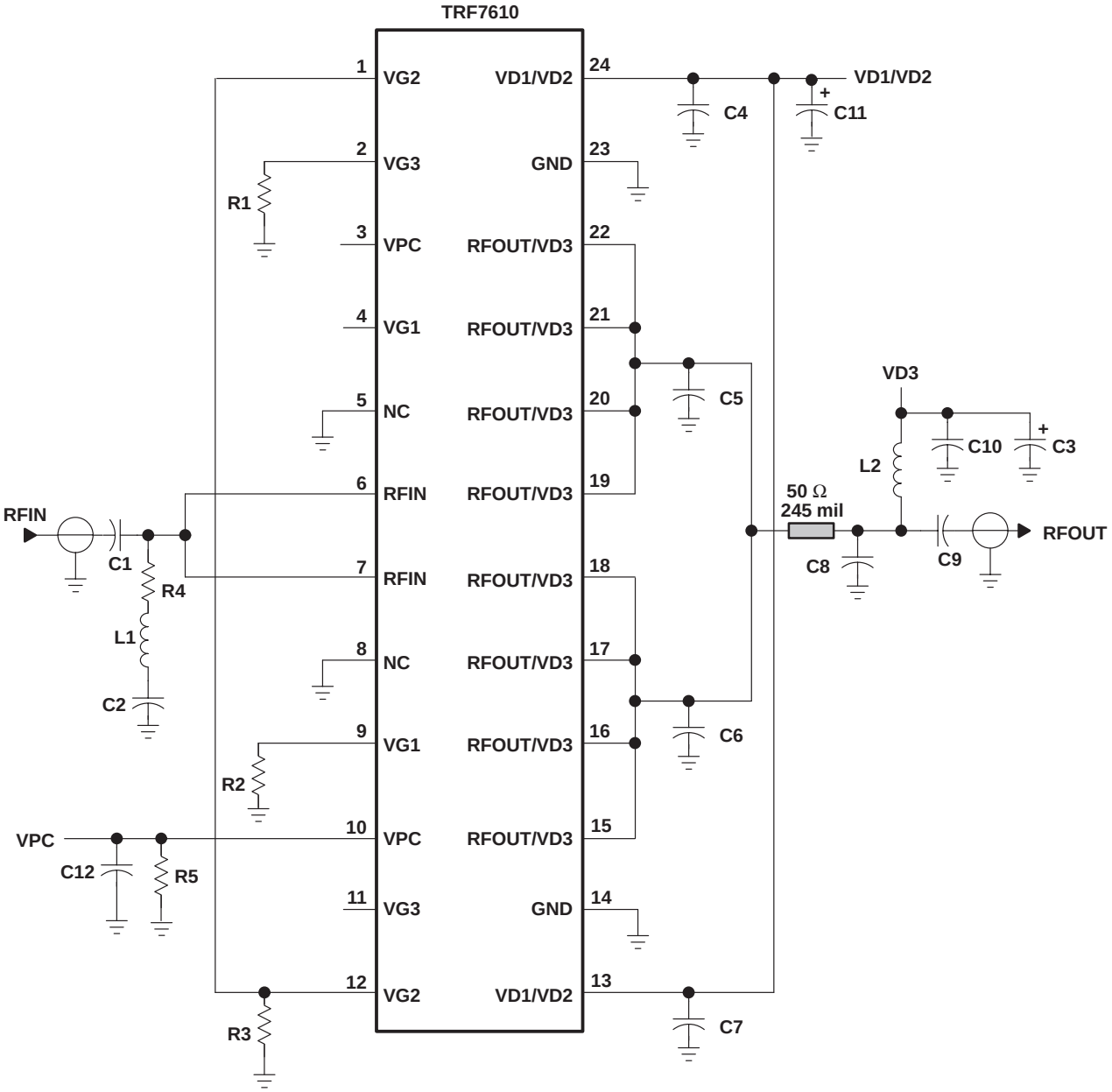


Figure 1. Typical GSM Cellular Telephone Application

Table 1. External Component Selection

COMPONENT DESIGNATION	TYPICAL VALUE	FUNCTION
C1	100 pF	DC blocking capacitor
C2	100 pF	Matching capacitor
C3	330 μF	Drain-bias decoupling capacitor
C4	0.033 μF	Drain-bias decoupling capacitor
C5, C6	22 pF	High-Q matching capacitor
C7	0.033 μF	Drain-bias decoupling capacitor
C8	11 pF	High-Q matching capacitor
C9	100 pF	DC blocking capacitor
C10	100 pF	Drain-bias decoupling capacitor
C11	100 μF	Drain-bias decoupling capacitor
C12	100 pF	Decoupling capacitor
R1	2200 Ω	Gate-bias setting resistor
R2, R3	5100 Ω	Gate-bias setting resistor
R4	3.9 Ω	Matching resistor
R5	51 Ω	Vpc termination resistor
L1	2.7 nH	Matching inductor
L2	18.5 nH high-current inductor or λ/4 microstrip line†	Drain bias inductor

† On a FR4 substrate with $\in_r$ of 4.3, a λ/4 50 Ω line is 40 mm.

design philosophy

The TRF7610 is a three-stage integrated power amplifier for use in cellular phone handsets. The device and applications board are optimized to operate under 900-MHz, 4.8-V GSM conditions. External matching networks provide design flexibility in centering the frequency response from 800 to 1000 MHz. Typical performance at 900 MHz, driven by a 5-dBm GSM signal, is 30 dB of power gain, 35 dBm output power, and 40 percent PAE.

Discrete component selection was made to optimize output power, gain, pulse flatness in the GSM pulse window, and PAE. Where possible, size and cost goals were considered: the smallest, least expensive components available were included in the applications board design. Some of the components, however, were chosen for their ability to increase performance. The following sections explain the design options and compromises to consider when substituting parts of differents types and values.

output matching network

The output matching network provides the majority of the design flexibility. First, the shunt capacitors, C5, C6, and C8 are American Technical Ceramics high-Q capacitors, which increase performance. The ATC capacitors achieve a 0.4-dB increase in output power and a 3-percent increase in PAE compared to the performance achieved using 0402-sized capacitors. However, if size and cost are more important, 0402-sized capacitors can be used, while sacrificing the performance gains achieved using the high-Q capacitors.

Second, the dc bias network on the amplifier output stage, designed using a Coilcraft 18.5 nH high-current inductor (L2), minimizes the board layout area. An alternative to this high-current inductor is a quarter-wave stub with a bias decoupling capacitor to ground (C10, C3). On the FR4 board with $\in_r$ = 4.3, a quarter-wave stub at 900 MHz is 40 mm in length. One advantage that the quarter-wave stub offers over the inductor is improved second harmonic suppression. The inductor offers a much smaller footprint; however, it does sacrifice 10 dB

of second harmonic suppression. The PAE is only slightly affected: it is reduced by approximately 1 percent compared to the quarter-wave stub. The system designer must decide if size or performance is of greatest concern.

The 330 μF bias decoupling capacitors, C3 and C11, provide pulse flatness in the GSM application. These surface mount capacitors provide a gain slope of –0.4 dB over the duration of the GSM duty cycle. If that is not acceptable, the performance can be improved by adding a larger value capacitor in parallel with the two existing capacitors. Measured results, using a standard 4700 μF electrolytic taken from a cellular phone, is –0.1 dB of gain slope for the duration of the GSM duty cycle. Capacitor size considerations must be decided by the system designer.

dc bias network

The dc bias network consists of resistors R1, R2, R3, and R5, which set the gate bias voltage of the device. R1, R2, and R3 are used as voltage divider resistors which set the gate voltages at approximately 1.7 V. Resistor R5 is a 51 Ω termination resistor that is needed only for a 50 Ω pulse generator. When a high-impedance pulse generator is used, the 51 Ω resistor can be omitted as it is not necessary for device function.

TYPICAL CHARACTERISTICS

POWER ADDED EFFICIENCY vs INPUT POWER

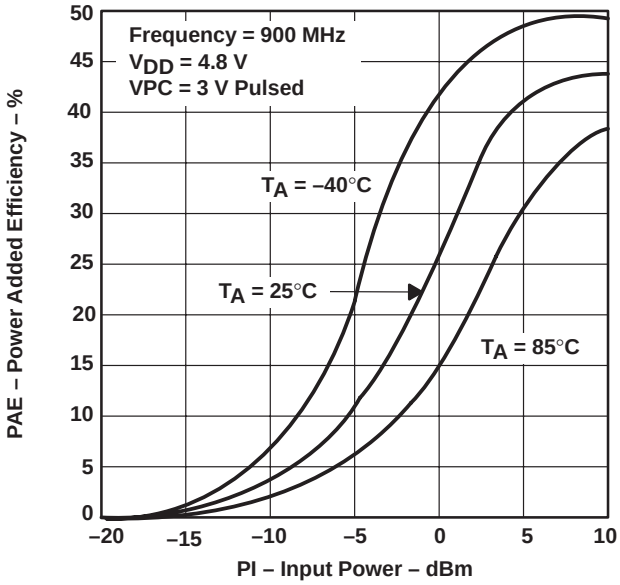


Figure 2

POWER ADDED EFFICIENCY vs FREQUENCY

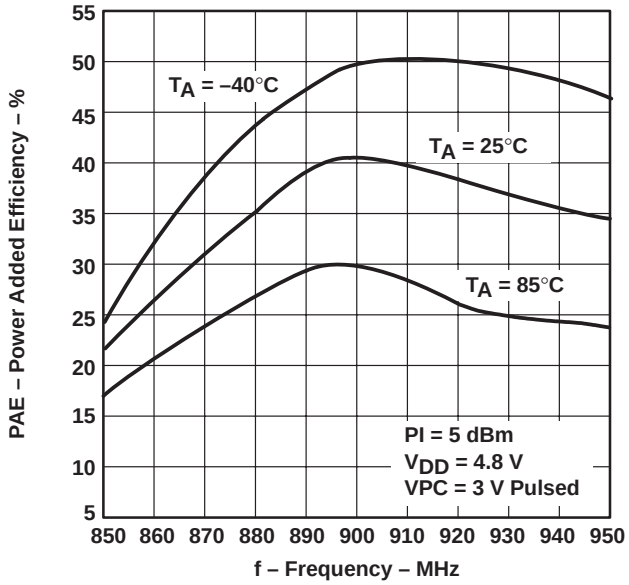


Figure 3

POWER ADDED EFFICIENCY vs DRAIN VOLTAGE

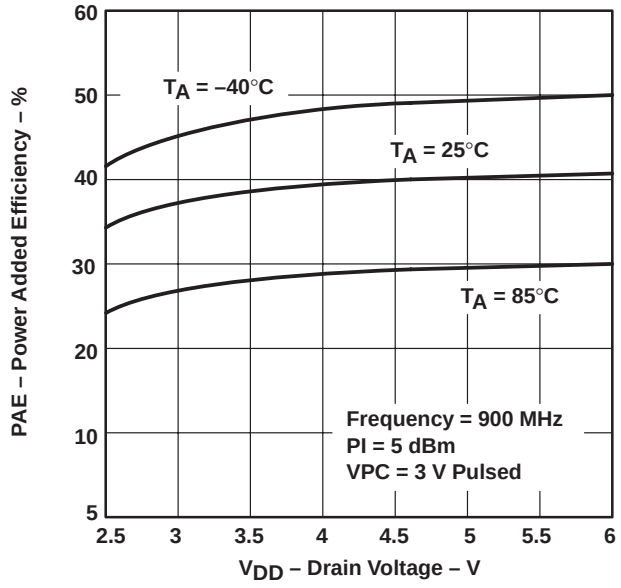


Figure 4

POWER ADDED EFFICIENCY vs POWER CONTROL VOLTAGE

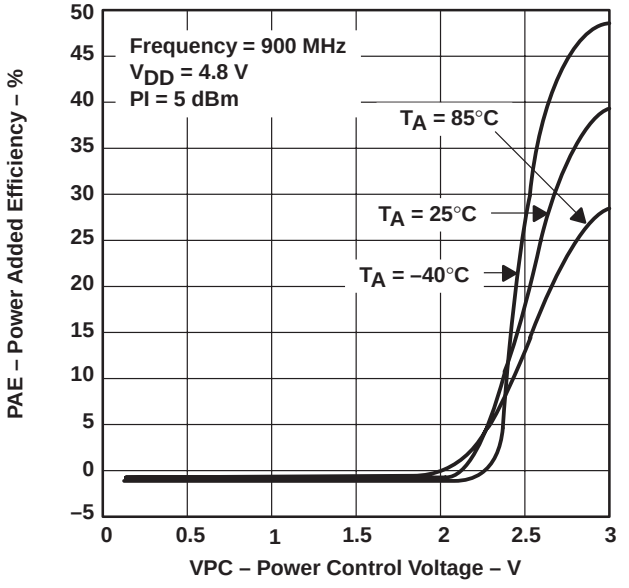


Figure 5

TYPICAL CHARACTERISTICS

OUTPUT POWER vs INPUT POWER

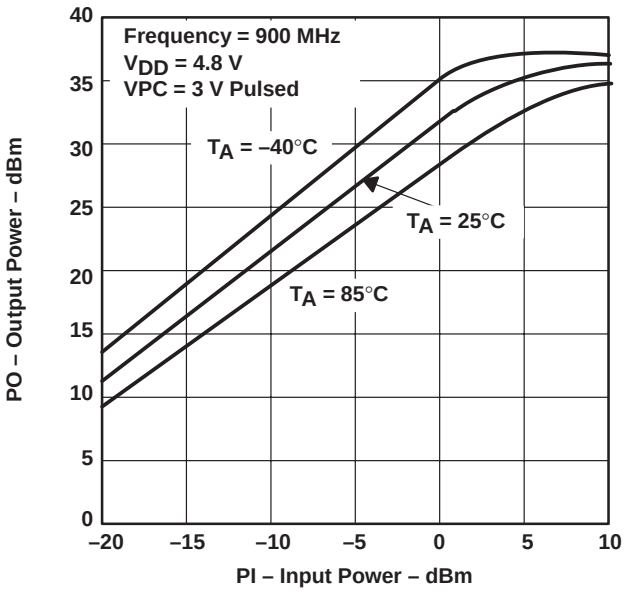


Figure 6

OUTPUT POWER vs FREQUENCY

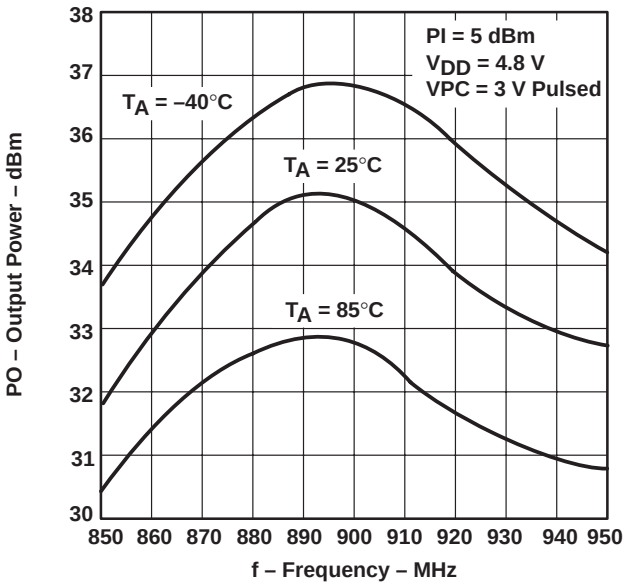


Figure 7

OUTPUT POWER vs DRAIN VOLTAGE

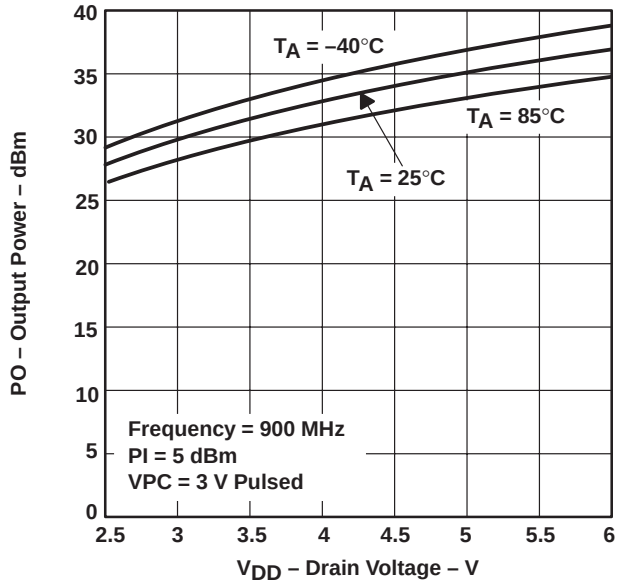


Figure 8

OUTPUT POWER vs POWER CONTROL VOLTAGE

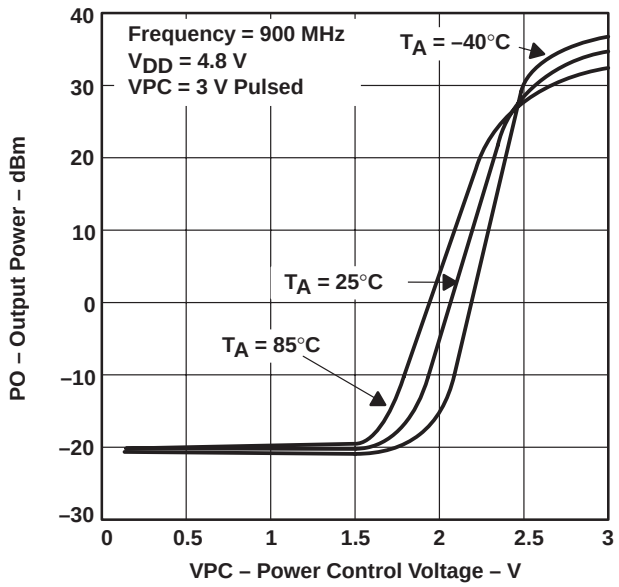


Figure 9

TYPICAL CHARACTERISTICS

**INPUT RETURN LOSS
vs
FREQUENCY**

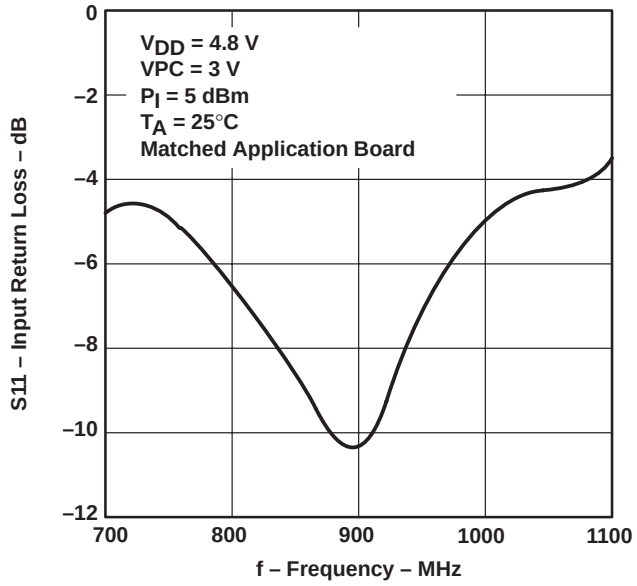


Figure 10

**SMALL SIGNAL GAIN
vs
FREQUENCY**

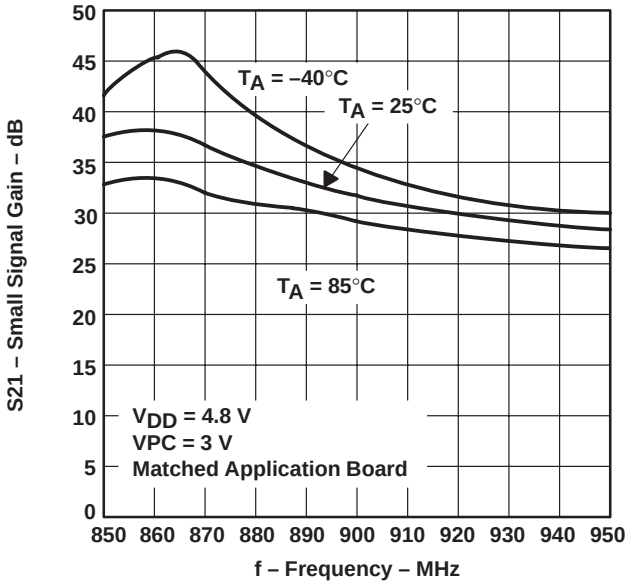
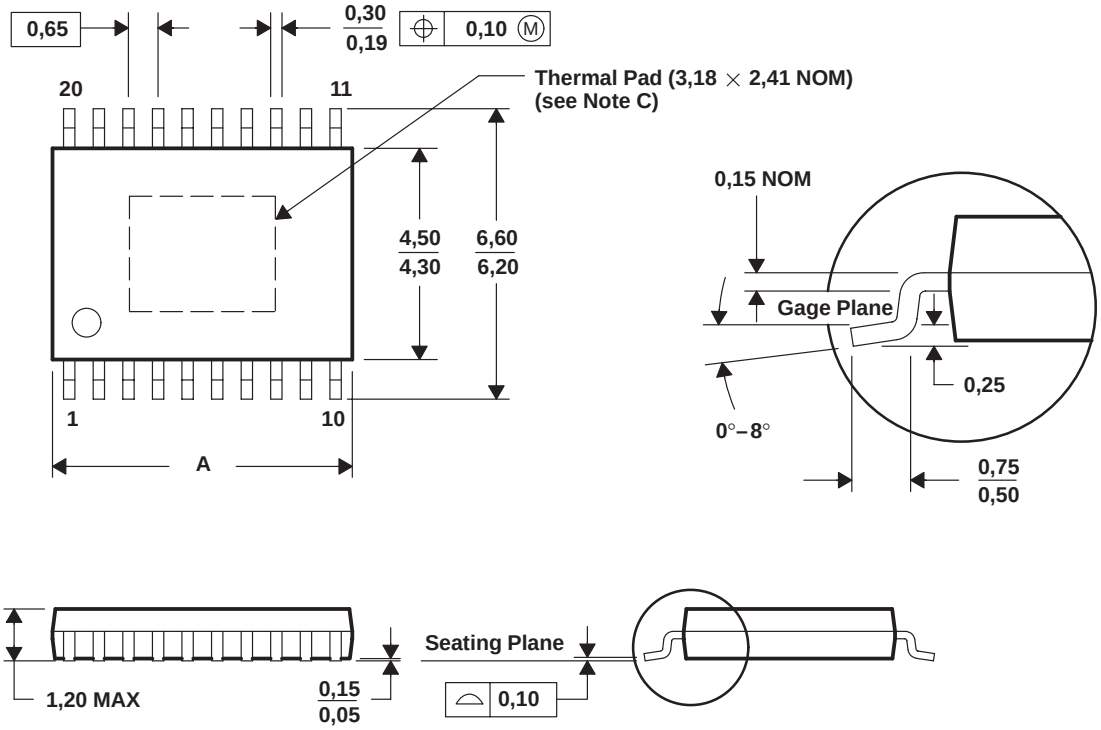


Figure 11

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This solderable pad is electrically and thermally connected to the backside of the die.

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