



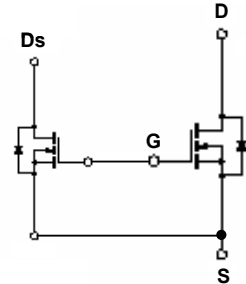
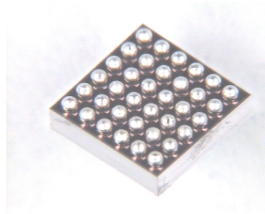
For information only

DC-DC Converter Control and Synchronous AceFET™

TS12N30CS – 30V Single N-Channel 4.5V Specified AceFET™

General Description

Taiwan Semiconductor's new low cost, state of the art AceFET™ lateral MOSFET process technology in chip-scale bondwireless packaging minimizes PCB space and $R_{DS(ON)}$ plus provides an ultra-low $Q_g \times R_{DS(ON)}$ figure of merit.

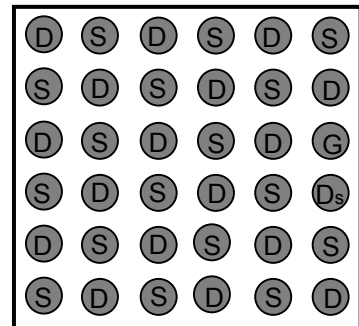


Features

- 12A, 30V $R_{DS(ON)} = 6m\Omega$ at 4.5 Volts
- 12A, 30V $Q_g = 15nC$ at 4.5 Volts
- Low profile package: less than 1mm height when mounted on PCB
- Occupies only 1/3 the area of SO-8.
- Excellent thermal characteristics.
- High power and current handling capability.
- Lead free solder balls available.

AceFET™ for High Frequency DC-DC Converters

Patent Pending



Bottom: Bump Side

Absolute Maximum Ratings

$T_A=25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current	– Continuous	6
		– Pulsed	25
PD	Power Dissipation (Steady State)	2.2	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	56	$^\circ C/W$
$R_{\theta JR}$	Thermal Resistance, Junction-to-Ball	4.5	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.6	



Electrical Characteristics

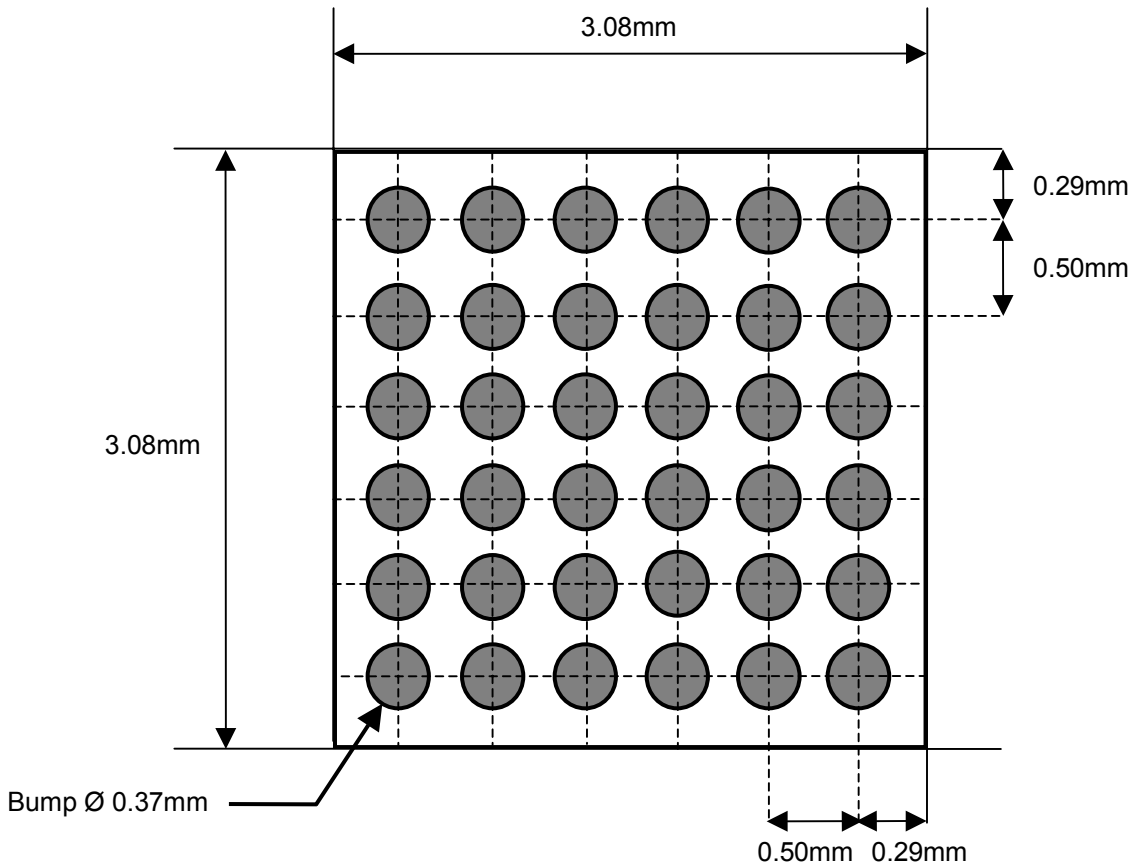
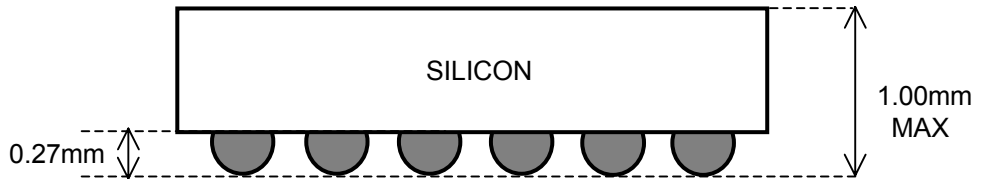
TA=25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ.	Max	Units
BVDSS	Drain-Source Breakdown Voltage	VGS = 0 V, ID= 250 uA	30			V
IGSS	Gate-Body Leakage	VGS = ±12, VDS=0V			±150	nA
IDSS	Zero Gate Voltage Drain Current	Tj = 150°C, VDS =30V , VGS=0 V			250	uA
IDDS	Drain to Drain Sense Leakage	Tj = 150°C, VDS =30V , VGS=0 V			250	uA
RDS (on)	Static Drain-Source On-Resistance	VGS = 4.5 V, ID = 12A		6		mΩ
RDSDS (on)	Drain Sense On-Resistance	VGS = 4.5 V, ID = 0.35A		210		mΩ
VGS (th)	Gate Threshold Voltage	VDS = VGS , ID = 250uA		1.3		V
Qg	Total Gate Charge	VDS = 30V , VGS = 4.5V, ID=12A		15		nC
Rg	Gate Resistance	VDS = 0V , f = 1MHz		0.4		Ohms
Coss	Output Capacitance	VDS = 30V , VGS = 0V, f = 1MHz		650		pF
Ciss	Input Capacitance	VDS = 30V , VGS = 0V, f = 1MHz		1500		pF
Crss	Reverse transfer capacitance	VDS = 30V , VGS = 0V, f = 1MHz		220		pF
trr	Reverse Recovery time Source-Drain Diode	If = 12A , di/dt = 100A / us Tj = 150°C			40	ns
VSD	Forward On-Voltage Source-Drain Diode	Is = 12A, VGS = 0V		0.75		V
ID(on)	On-State Drain Current	VGS = 4.5V , VDS = 1V	25			A
Eas	Avalanche Energy UIS	Single Pulse 10us , VDS> BVDSS	2.5			mJ

TS12N30CS



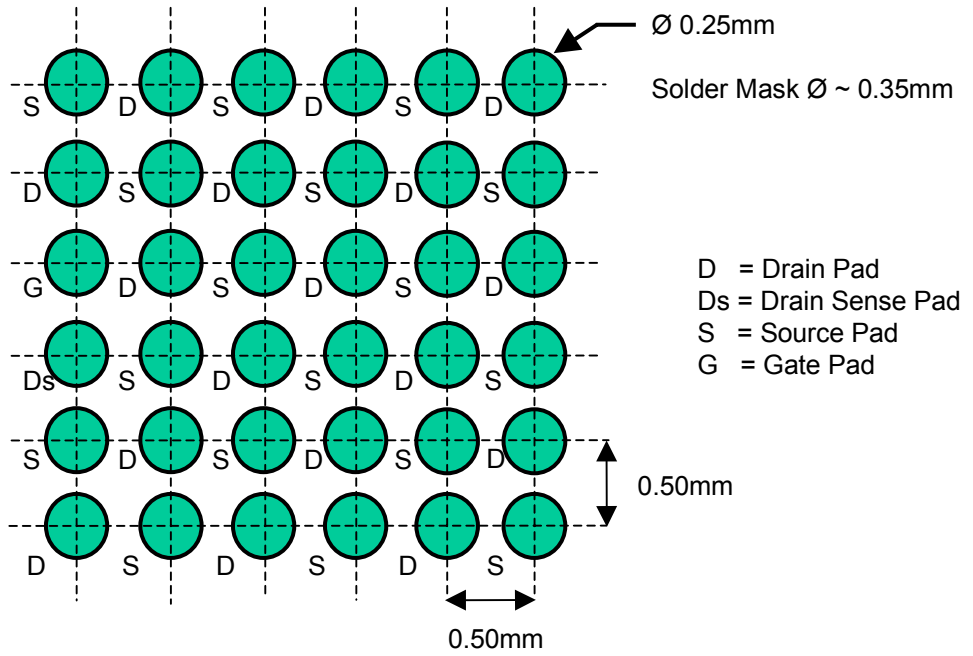
Dimensional Outline and Pad Layout



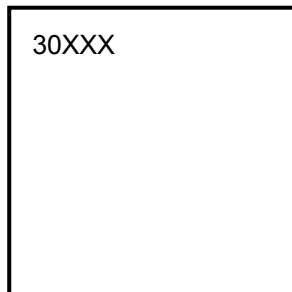
Bumps are Lead Free solder 96.8 Sn / 2.6 Ag / 0.6 Cu



Dimensional Outline and Pad Layout



LAND PATTERN RECOMMENDATION



MARK ON BACKSIDE OF DIE

XXX = Date/Lot Traceability Code