Galvanic Isolated Latching 60V Power Load Switch

TRIUNE PRODUCTS

Features

- Low Quiescent Operating Currents
  - 2uA in OFF state
  - 4uA in ON state
- Scalable galvanic isolation from primary to secondary sides of the device
- Single control signal for on/off input (CLK)
  - Operation from 2.9V to 5.5V compatible with standard microcontrollers
- Switch Characteristics
  - High voltage switch with bi-directional blocking in OFF state
  - Single switch device
  - 60V switch and 110mohm Rdson
  - Up to 4A operating current

Specification

- Junction operating temperature -40 °C to 125 °C
- Packaged in a 20pin QFN (4x4)

Description

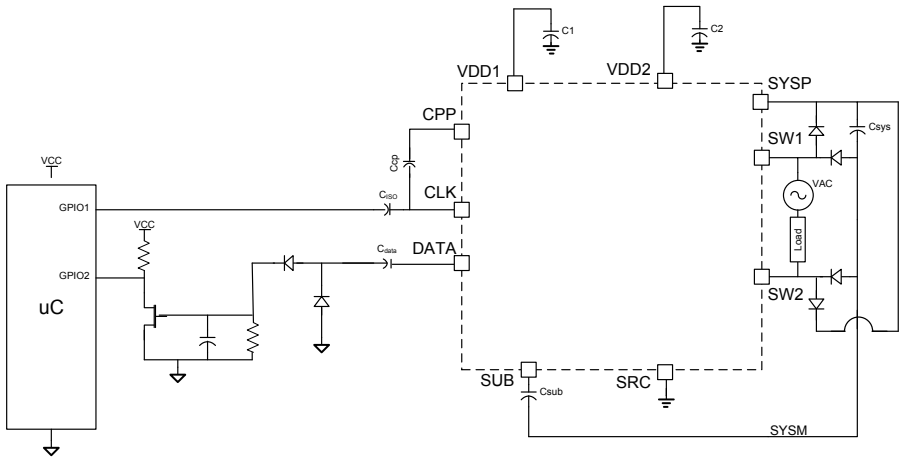
The TS13101 is a galvanically isolated 60V power switch device with bi-directional blocking. The device includes a single integrated 110mOhm high voltage FET allowing high efficiency switching of power loads or other high current applications. The input pin, CLK, controls the turn on/off of the switch. When the correct CLK sequence is provided the switch will latch on and stay on until the turn off sequence is given or a fault is detected.

The TS13101 includes several protection features. Each FET has an integrated over-current shut-down to prevent device damage during short-circuit or other unusually high load conditions. If an over-current event is detected for a time the FET is latched off until the CLK turn off sequence is given. While the CLK pin is active after an over-current event or in the event of an incorrect turn-on sequence, the DATA pin is toggled at ¼ the CLK frequency.

Applications

- Power load/rail switching
- Input supply muxing
- Isolated power supplies
- Solid state relays
- HVAC control

Typical Application Circuit



Pin Description

Pin #	Pin Name	Pin Function	Description
1	SRC	GND	
2	SW2	Switch Output Node 2	
3	SW1	Switch Output Node 1	
4	SW1	Switch Output Node 1	
5	SW2	Switch Output Node 2	
6	SW1	Switch Output Node 1	
7	SW2	Switch Output Node 2	
8	SW2	Switch Output Node 2	
9	DATA	Data Output	AC Coupled Data Output
10	CLK	Clock Input	AC Coupled Clock and Power Input
11	SYSP	Positive System Voltage	
12	CPP	Charge Pump Cap	Additional Cap used for lower voltage Clock drive
13	VDD1	Internal Supply 1	Bypass Capacitor for Internal Supply
14	VDD2	Internal Supply 2	Bypass Capacitor for Internal Supply
15	NC	No Connect	
16	SUB	GND2	
17	NC	No Connect	
18	SW1	Switch Output Node 1	
19	SW1	Switch Output Node 1	
20	SW2	Switch Output Node 2	
PAD	PAD	Power PAD	Must be floating or connected to SUB

Functional Block Diagram

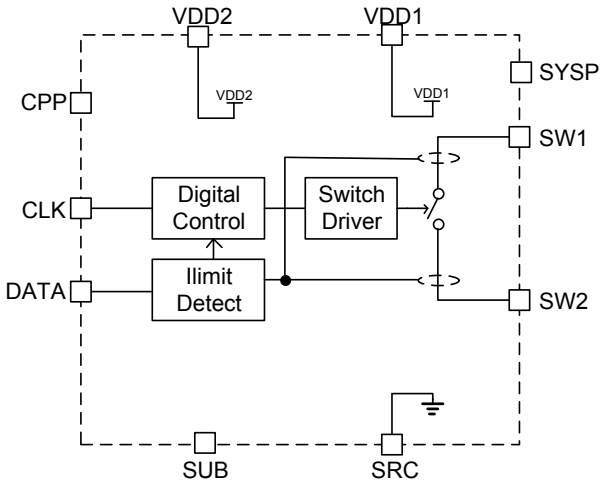


Figure 1: TS13101 Block Diagram

Absolute Maximum Rating

Over operating free–air temperature range unless otherwise noted(1, 2, 3)

Parameter	Range	UNIT
SW1, SW2, SYSP (Peak Voltage)	-60 to 60	V
CLK, CLK2, DATA, VDD1, VDD2, CPP	-0.3 to 5.5	V
SUB	-60 to 0.3	V
Operating Junction Temperature Range, TJ	-40 to 125	°C
Storage Temperature Range, TSTG	-65 to 150	°C
Electrostatic Discharge – Human Body Model	±2k	V
Electrostatic Discharge – Machine Model	+/-200	V
Electrostatic Discharge – IEC Contact (SW1 and SW2 pins)	±8k	V
Electrostatic Discharge – IEC Air Discharge (SW1 and SW2 pins)	±15k	V
Lead Temperature (soldering, 10 seconds)	260	°C

Notes:

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to SRC terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

Thermal Characteristics

Symbol	Parameter	Value	Units
Θ_{JA}	Thermal Resistance Junction to Air (Note 1)	25	°C/W
Θ_{JC}	Thermal Resistance Junction to Case (Note 1)	2.5	°C/W
T_{STG}	Storage Temperature Range	-65 to 150	°C
$T_{J\ MAX}$	Maximum Junction Temperature	150	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes 20LD 4x4 QFN with hi-K JEDEC board and 13.5 inch2 of 1 oz Cu and 4 thermal vias connected to PAD

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VSW	AC Switch Voltage (RMS Voltage)	-36		36	V
CDATA	Data Isolation Capacitor		100		pF
CISO	Clock Isolation Capacitor		680		pF
CCP	Charge Pump Capacitor		100		pF
CVDD1	VDD1 Bypass Capacitor		10		nF
CVDD2	VDD2 Bypass Capacitor		1		uF
CSUB	Sub Capacitor		100		nF
CSYS	System Bypass Capacitor		100		nF
CCLK2	Clock2 Isolation Capacitor		680		pF

Characteristics

Electrical Characteristics, T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage						
V_{CLK}	Clock Drive Voltage				5.5	V
$I_{CLK-NORM}$	Quiescent current	VCLK = 5.0V, FCLK = 500KHz	2.9	15		uA
$I_{CLK-NORM}$	Normal Mode, CLK running	VCLK = 3.0V, FCLK = 1000KHz		50		uA
$I_{CLK-STBY}$	Quiescent current	VCLK = 0V			3	uA
I_{SYSP}	Normal Mode, CLK running	Latch Mode		3	5	uA
VCLK Drive						
F_{CLK}	Clock Frequency to Turn on Switch		300		2000	KHz
F_{DATA}	Data Frequency during Current Shutdown			$F_{CLK}/4$		KHz
$N_{CLKON-INIT}$	Number of CLK pulses to initialize Turn On		3		8	
T_{LOW-ON}	CLK Low time during Turn On Sequence		10		20	uS
N_{CLKON}	CLK Pulses to Turn on SW After T_{LOW-ON}			15		
$T_{FASTOFF-INIT}$	CLK Low time to Initialize Fast Turn-Off		10		20	uS
$N_{CLK-FOEN}$	CLK Pulses to Enable Fast Turn-Off After $T_{FASTOFF-INIT}$		6		13	
$T_{OFF-FAST}$	Time for Turn Off	Fast Mode	4		10	uS
$N_{CLK-OFFDET}$	CLK Pulses to Detect Incorrect Turn-On Sequence	Resets with T_{LOW-ON}		19		
Output Switch						
R_{ON}	On Resistance	T_J=-10C to 65C	75	105	150	mΩ
R_{ON}	On Resistance	T_J=25C	90	105	130	mΩ
I_{OFF}	Off State Leakage				3	uA
$IOUT_{OC}$	Output Over Current Shutdown	T_J=-40C to 125C	4.0		7.2	A
$IOUT_{OC}$	Output Over Current Shutdown	T_J=-10C to 65C	4.4	5.5	6.6	A
OC_{FILT}	Output Over Current Deglitch			25		uS

Application Waveforms

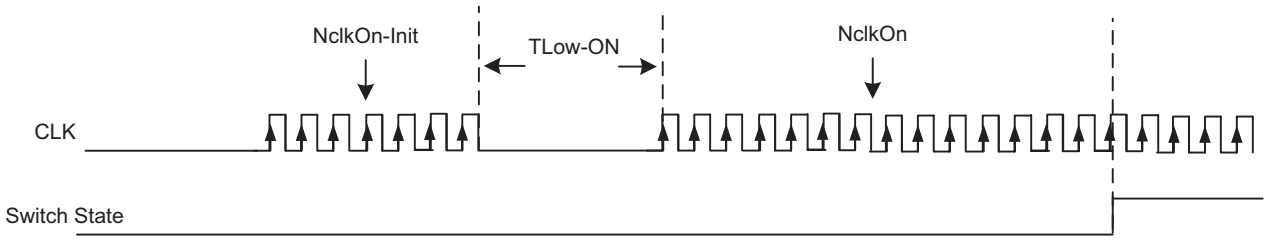


Figure 2: Clock Turn-on Sequence

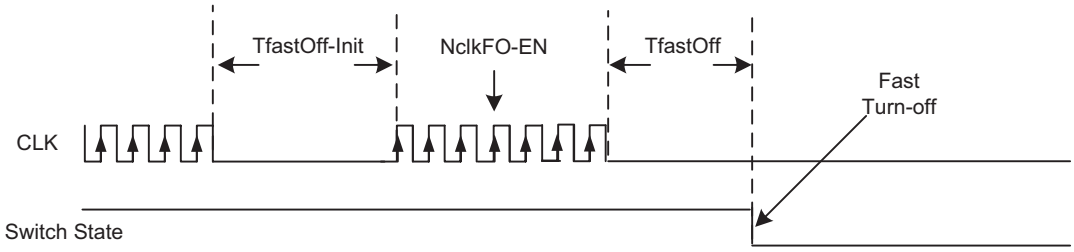


Figure 3: High-speed Turn-off Mode

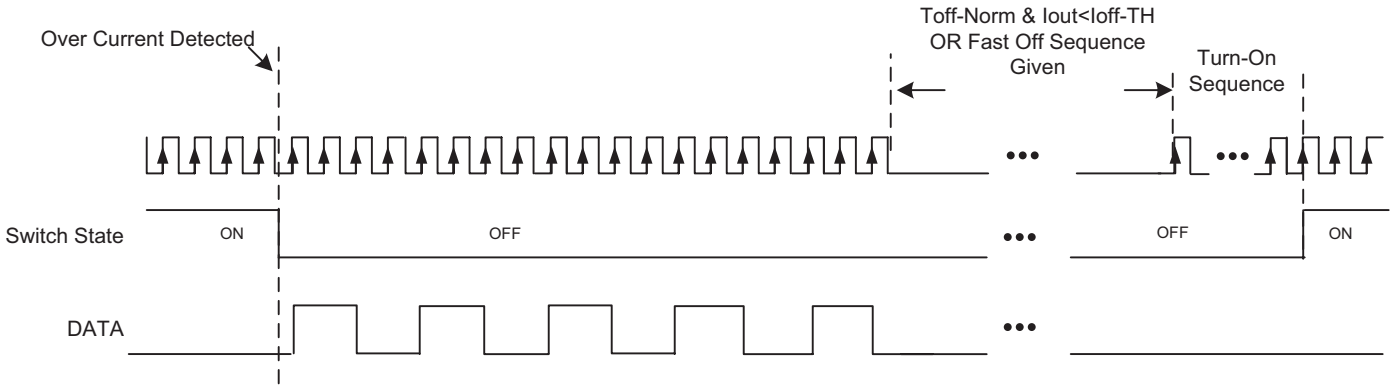


Figure 4: Over-current Shut-down and Restart

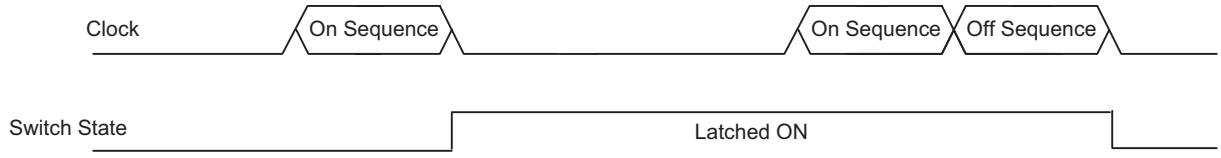
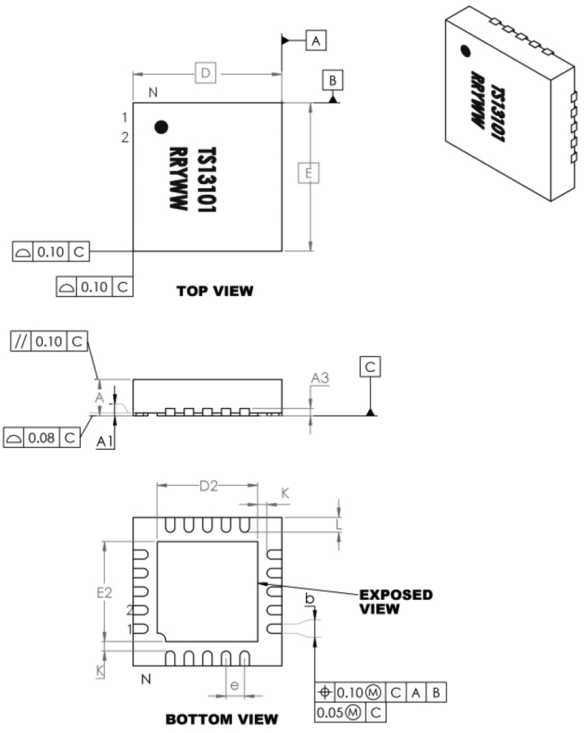


Figure 5: Latch Mode On / Off Sequence

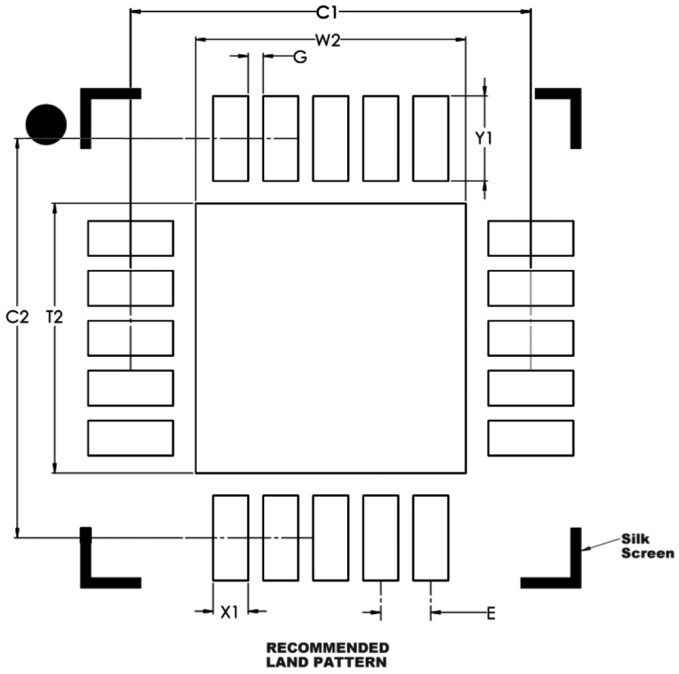
Package Mechanical Drawings



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	2.55	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	2.55	2.70	2.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
RR = Revision number
YWW = Year Calendar Week

Package Mechanical Drawings



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2	-	-	2.70
Optional Center Pad Length	T2	-	-	2.70
Contact Pad Spacing	C1	-	4.00	-
Contact Pad Spacing	C2	-	4.00	-
Contact Pad Width X20	X1	-	-	0.35
Contact Pad Length X20	Y1	-	-	0.35
Distance Between Pads	G	0.15	-	-

Notes:
Dimensions and tolerancing per ASME Y14.5M
REF: Reference Dimension, usually without tolerance, for information only.
BSC: Basic Dimension, Theorically exact value shown with tolerances.

Ordering Information

Part Number	Description
TS13101-QFNR	Latching Galvanic Isolated Switch

RoHS and Reach Compliance

Triune Systems is fully committed to environmental quality. All Triune Systems materials and suppliers are fully compliant with RoHS (European Union Directive 2011/65/EU), REACH SVHC Chemical Restrictions (EC 1907/2006), IPC-1752 Level 3 materials declarations, and their subsequent amendments. Triune Systems maintains certified laboratory reports for all product materials, from all suppliers, which show full compliance to restrictions on the following:

- Cadmium (Cd)
- Chlorofluorocarbons (CFCs)
- Chlorinate Hydrocarbons (CHCs)
- Halons (Halogen free)
- Hexavalent Chromium (CrVI)
- Hydrobromofluorocarbons (HBFCs)
- Hydrochlorofluorocarbons (HCFCs)
- Lead (Pb)
- Mercury (Hg)
- Perfluorocarbons (PFCs)
- Polybrominated biphenyls (PBB)
- Polybrominated Diphenyl Ethers (PBDEs)

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