TS1911

Vision-Clear Video Processor

Product Datasheet

Revision 1.0

2010/07/24

Taiwan Surveillance Semiconductor, Inc.

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Revision Note

Revision	Modification List	Date	Note
1.0	1. First release. 2. Updated sections 9.2.1, 9.2.2 and 9.2.5 VE Control Register Description. 3. Updated section 9.3 Noise Reduction Control Register Description. 4. Updated section 9.9.2 OSD Control Register Description. 5. Reviewed 3.2 Video Processing and Functions section. 6. Added the listing of built-in OSD fixed fonts at Section 3.3. – Font Type.	2010/07/24	
0.7	1. Updated “3.4 Hardware and Physical Implementation” typos. 2. Added in “SPI Master 0 and SPI Master 1 Block Descriptions”. 3. Added in “GPIO Block Registers” Descriptions. 4. Cosmetically touched up all register map tables. 5. Updated PCB Recommended Design section. 6. Added in “I2C Master Block Registers” Descriptions. 7. Removed Register 0xA0 and above descriptions of Page 0x04 as they are intended for internal usage. 8. Added in “CLK_GEN Register” Descriptions. 9. Added in “Electrical Information” section.	2010/05/21	
0.6	1. Updated Application Diagram. 2. Updated Hardware and Physical Implementation – SPI section. 3. Added Turbo 8051 Block Diagram. 4. Updated OSD font border descriptions and limitations in various operation modes. 5. Updated Recommended PCB Design section. 6. Updated Video Processing and Functions section. 7. Added Programmable I2C Slave ID description.	2010/05/03	
0.5	1. Added in Pin Definition section. 2. Added in Chip Package Outline. section. 3. Added in Recommended PCB layout footprint section.	2010/03/29	
0.4	1. Refined Overview 2. Updated font OSD section. 3. Inserted Control Register section. 4. Renewed System Application Diagram.	2010/03/01	
0.3	Changed Title Page.	2010/02/20	
0.2	1. Refined Overview 2. Updated font OSD section. 3. Inserted Control Register section.	2010/02/03	
0.1	First Preliminary Version	2009/12/11	

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TS1911

Vision-Clear Video Processor

1. Overview

The TS1911 is a specially designed 1-channel digital video signal processor for video streams taken under adverse imaging conditions: misty, foggy, low ambient light, harshly backlit from behind targets, and/or other noisy scenes. The TS1911 offers pure ASIC implementation, robust hardware digital signal processing and video enhancement algorisms to optimize video streams from image sensors, thus delivers the best vision-clear video quality with best cost/performance in its class.

TS1911 accepts an ITU-R BT.656 video input and has mist correction (De-Mist^{TM}), Wide Dynamic Range Correction (WDRC^{TM}), and 2D/3D Noise Reduction – improving video quality, video compression efficiency, and visual information interpretation. De-Mist^{TM} is an advanced hardware-based digital image enhancement algorithm that automatically and adaptively adjusts contrast and color of images from particle-obscured scenes (fog, rain, smoke, dust storm, undersea, see-through fabric, etc.). WDRC^{TM} is a state-of-art, hardware-based real time image correction algorithm that widens perceivable luminance range by boosting visibility of dark areas without saturating bright areas – optimized for security system applications in dark or harshly backlit environments. Additionally, the 2D/3D Noise Reduction algorithm reduces image noise in real time – for cleaner image and up to 38% file size reduction for compressed video applications (e.g. MPEG-4).

Designed to be versatile and user-friendly, TS1911 features programmable OSD (on-screen display) functions with the onboard Turbo 8051 microcontroller. The onboard Turbo 8051 controls the core actions of TS1911 and connects to an external ISP FLASH (in-system programming FLASH memory) for maximum programmability. The intuitive and graphical OSD design tool would facilitate and ease the manufacturers for fine tuning application specific user-friendly on-site video parameters adjustment projects.

The TS1911 offers ITU-R BT.656 digital video output, as well as a 10-bit DAC CVBS (NTSC/PAL) video encoder that allows real-time image monitoring through a connected TV or a monitor.

2. Applications

- Outdoor/vehicle security cameras
- Traffic monitoring systems
- Automotive drive recorders
- Building/area security equipment
- Video enhancement devices
- Digital Video Recorders

3. Features

3.1. Input/Output

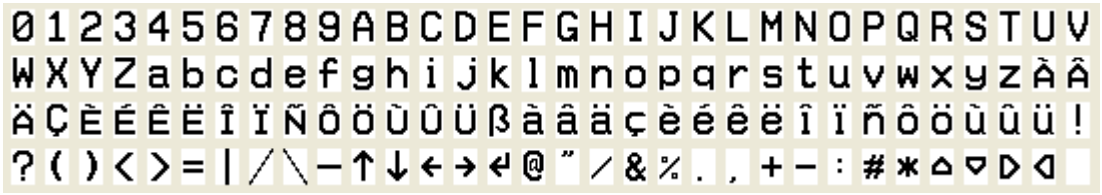
- **Video Input**: 1x ITU-R BT.656
- **Video Output**: 1x ITU-R BT.656, 1x video encoder (with 10-btit DAC)

3.2. Video Processing and Functions

- **De-Mist™**
  - Restores contrast information obscured in foggy conditions
- **WDRC™ (Wide Dynamic Range Correction)**
  - Improves visibility of dark areas without saturating bright areas
- **2D/3D Noise Reduction**
  - Reduces file size by up to 38% for MPEG-4 video recorded in dim and noisy ambiance (compared to NR off).
- **Video Encoder supports NTSC / PAL with One 10-bit CVBS Digital to Analog Converters (DAC)**

3.3. On-Screen Display (OSD) with Graphical User Interface

- **Font size**: 12 (horizontal) x 18 (vertical) pixels
- **Font type**
  - Supports 128 fixed fonts

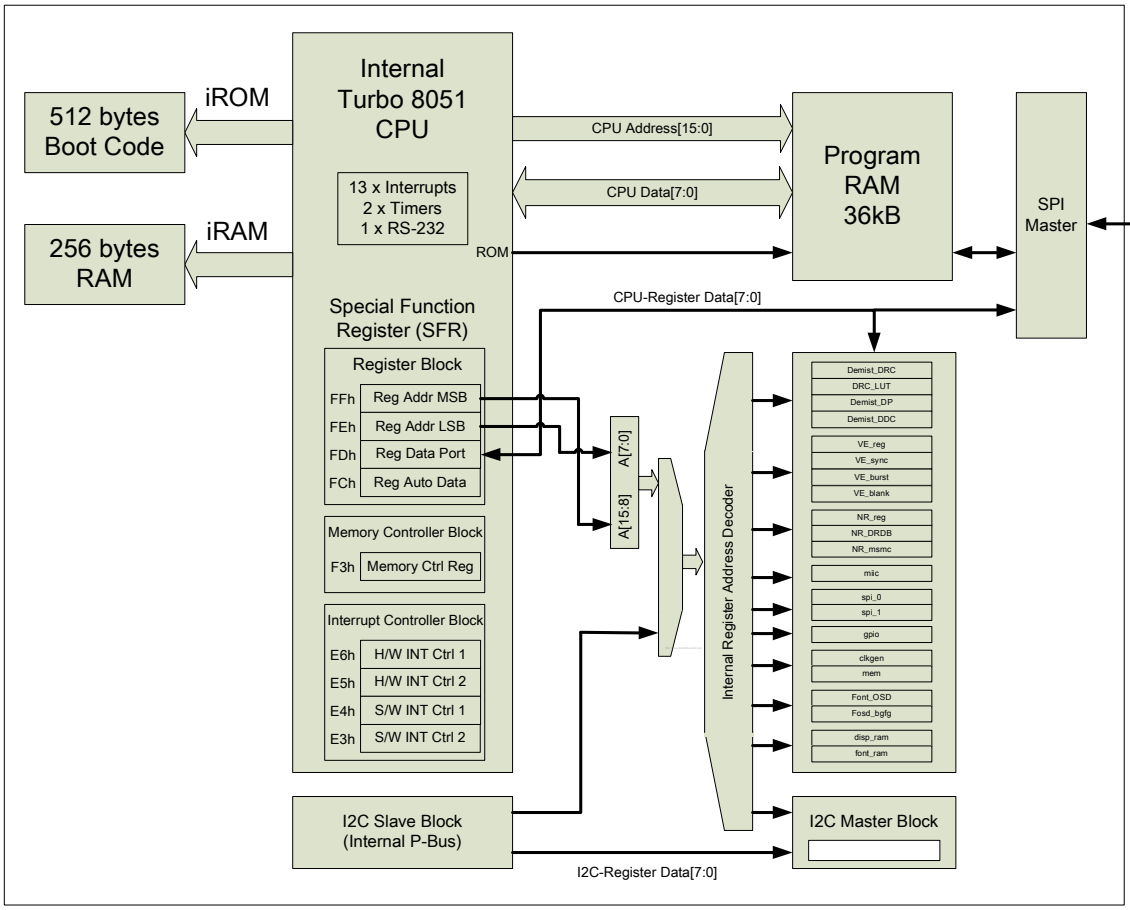


  - Supports 256 programmable fonts*
  - Supports 32 16-color icons**

  (* & **: Due to memory sharing mechanism, implementing OSD icons will decrease the number of available programmable fonts accordingly.)
- **OSD Programmability**
  - Programmable display RAM starting address
  - Programmable on screen display area origin position
  - Programmable chars per line, lines per frame (1~31 x 1~16)
  - Base symbol size: x=12, y=18 (pixels)
  - Global X and Y scale ratio: 1x, 2x, 3x, and 4x for both X and Y
  - Programmable horizontal and vertical space in between adjacent chars (0~12 pixels)
  - Programmable font color
  - Programmable highlighting and blinking (globally enable/disable)
  - Programmable blinking frequency(1~256 fields)
  - Supports up to 480 symbols in display area
  - Stores up to 384 symbols in internal memory(1152x24 ROM + 2304x24 SRAM)
  - Programmable up to 16 foreground and 16 background colors
  - Programmable and individual boundary and shadow control for each OSD window
- **OSD menu size**: 1x, 2x, 3x, or 4x times
- **OSD windowing capability**
  - Supports 3 OSD windows with alpha blending for better user interface experience

3.4. Hardware and Physical Implementation

- **2x SPI (Serial Peripheral Interface) Master**
- **On-chip Turbo 8051 Microcontroller**
  - Fully compatible with standard 8051 CPU instruction set
  - Up to 40Mhz clock rate with 4 clock cycles per instruction
  - 13 Interrupts, 16 General purpose I/O (GPIO) ports, 2 Watch Dog timers
  - Direct interface to external FLASH EEPROM, PROM or ROM without glue logics



- **System PLL** for internal clock signals generation
- **Programmable I2C Slave ID** (default: 0x80)
- **In System Programming (ISP)**
  - Built-in 512Bytes boot code ROM
  - Supported through RS-232 or I2C hardware protocols
- **Design for Testability (DFT)**
  - Memory BIST and dynamic remapping circuit
  - Scan chain & Boundary-Scan (JTAG/IEEE 1149.1)
  - Patent To be determined auto system test/burn-in & color calibration
- **Requires +1.8V (Core) and +3.3V (I/O) power supplies**
- **Package:** 68-pin QFN

4. TS1911 Block Diagram

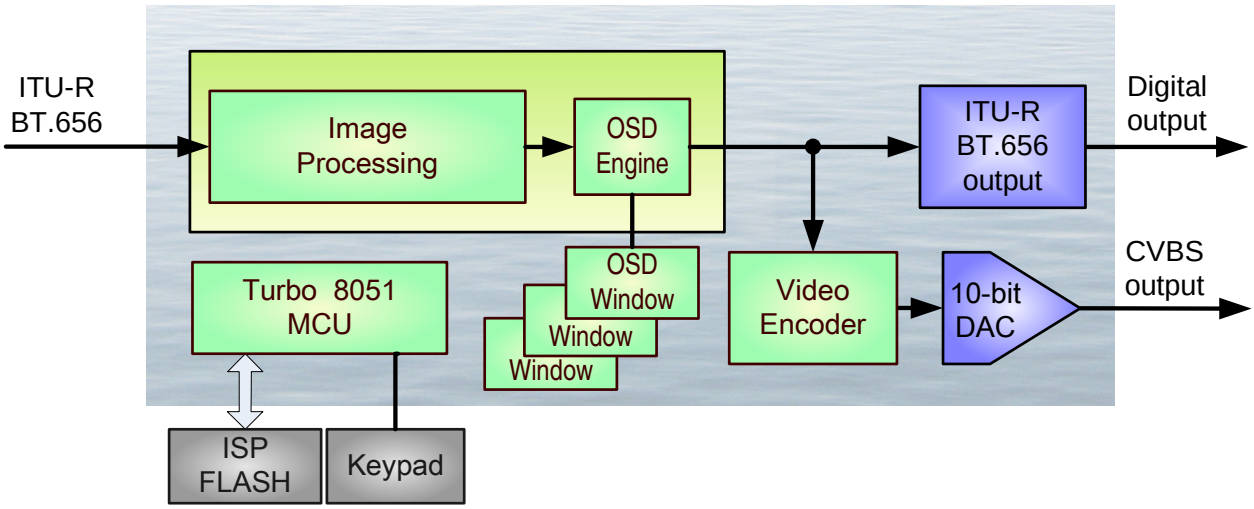


Fig. 4.1: TS1911 Block Diagram

5. TS1911 System Application Diagram

5.1. CCTV Camera Application Diagram

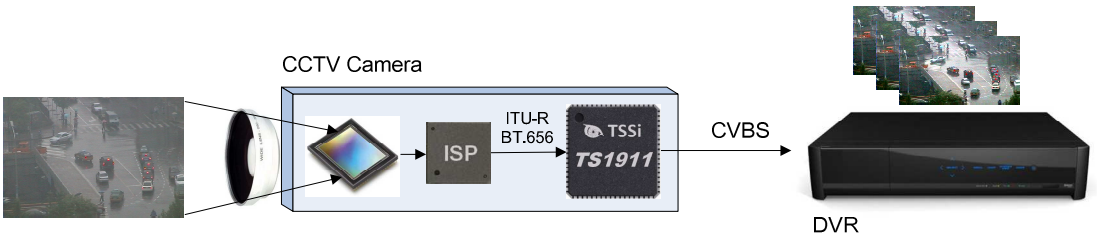


Fig. 5.1: CCTV Camera Application

5.2. IP Camera Application Diagram

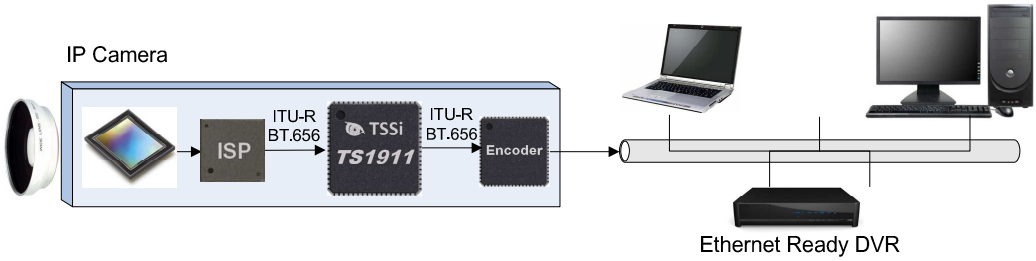
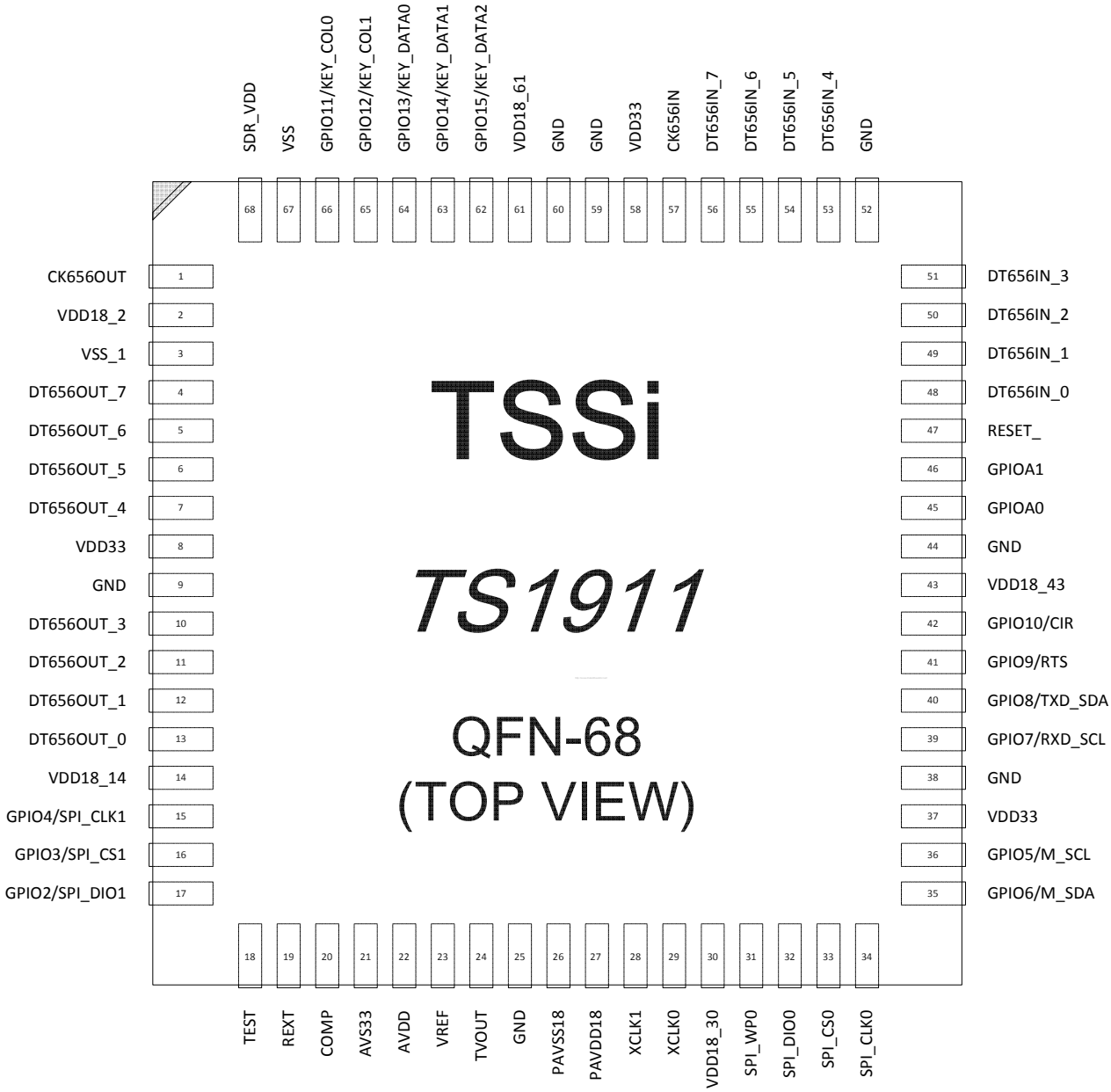


Fig. 5.2: IP Camera Application

6. Pin Information

6.1. Pin Diagram



6.2. Pin Descriptions

Input/Output Pin Types

DI = digital input
DO = digital output
DIO = digital input/output

AI = analog input
AO = analog output
AIO = analog input/output

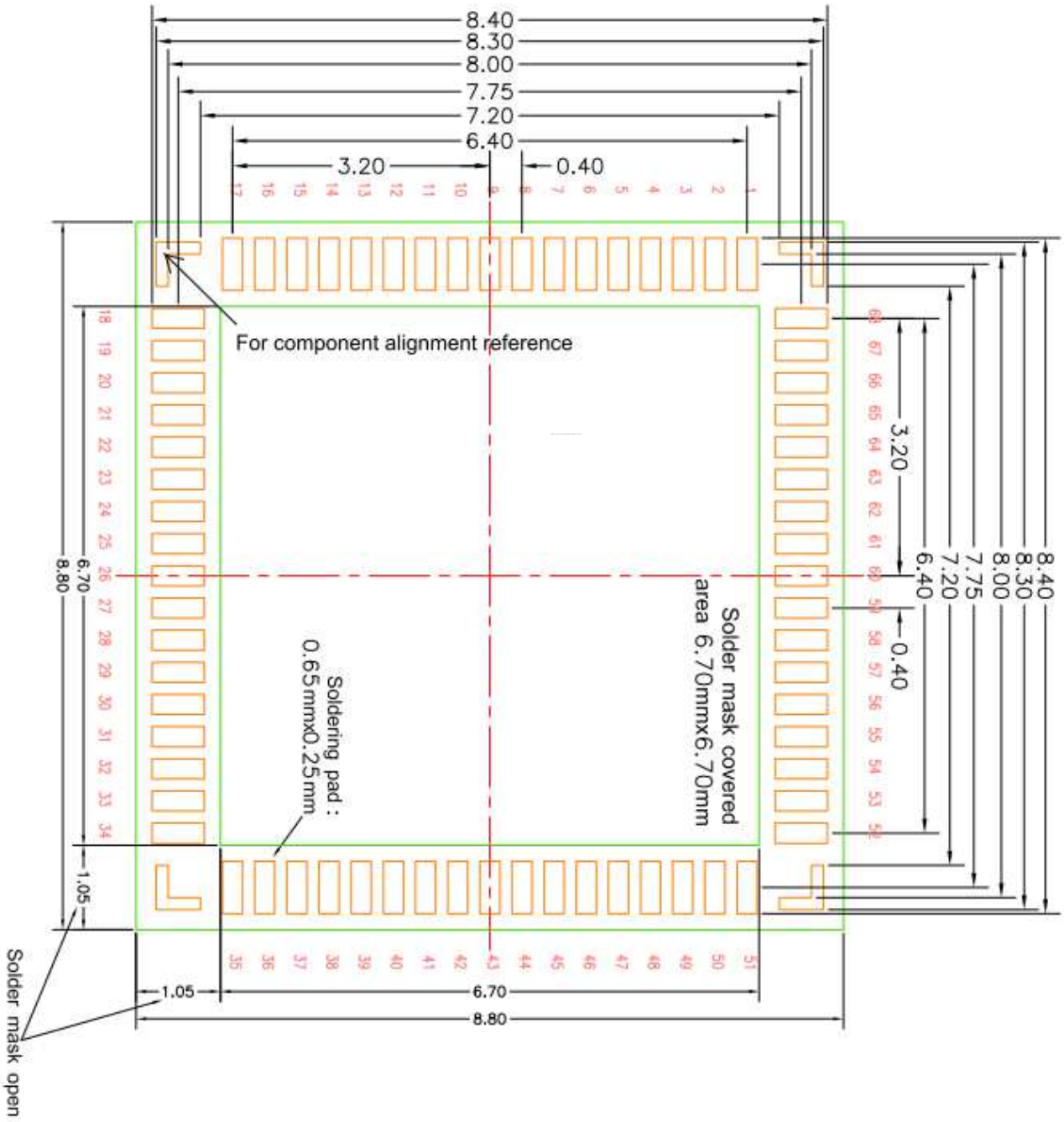
PWR = power
GND = ground

Pin number	Pin Name	I/O	Description
1	CK656OUT	DO	ITU-R BT.656 data out clock
2	VDD18_2	PWR	1.8V digital power supply
3	VSS_1	GND	Ground for SDRAM
4	DT656OUT_7	DO	ITU-R BT.656 data out 7
5	DT656OUT_6	DO	ITU-R BT.656 data out 6
6	DT656OUT_5	DO	ITU-R BT.656 data out 5
7	DT656OUT_4	DO	ITU-R BT.656 data out 4
8	VDD33	PWR	3.3V digital power supply
9	GND	GND	Ground
10	DT656OUT_3	DO	ITU-R BT.656 data out 3
11	DT656OUT_2	DO	ITU-R BT.656 data out 2
12	DT656OUT_1	DO	ITU-R BT.656 data out 1
13	DT656OUT_0	DO	ITU-R BT.656 data out 0
14	VDD18_14	PWR	1.8V digital power supply
15	GPIO4/SPI_CLK1	DO	General purpose IO 4 / SPI 1 Clock
16	GPIO3/SPI_CS1	DO	General purpose IO 3 / SPI 1 Chip Select
17	GPIO2/SPI_DIO1	DO	General purpose IO 2 / SPI 1 Data IO
18	TEST	DIO	Test pin
19	REXT	AIO	DAC External resistor
20	COMP	AI	DAC Compensation
21	AVSS33	GND	Ground of 3.3V analog power supply for TVOUT
22	AVDD	PWR	3.3V analog power supply for TVOUT
23	VREF	AI	DAC Voltage Reference input
24	TVOUT	DO	CVBS (NTSC/PAL) output
25	GND	GND	Ground
26	PAVSS18	GND	Ground of 1.8V analog power supply for PLL
27	PAVDD18	PWR	1.8V analog power supply for PLL
28	XCLK1	DI	Crystal Clock in, 27MHz
29	XCLK0	DO	Crystal Clock out

Pin number	Pin Name	I/O	Description
30	VDD18_30	PWR	1.8V digital power supply
31	SPI_WP0	DO	SPI 0 Write Protect for FLASH
32	SPI_DIO0	DO	SPI 0 Data IO
33	SPI_CS0	DO	SPI 0 Chip Select
34	SPI_CLK0	DO	SPI 0 Serial Clock
35	GPIO6/M_SDA	DO	General purpose IO 6 / I2C Mater SDA
36	GIPO5/M_SCL	DO	General purpose IO 5 / I2C Master SCL
37	VDD33	PWR	3.3V digital power supply
38	GND	GND	Ground
39	GPIO7/RXD_SCL	DIO	General purpose IO 7 / RS-232 RXD / I2C Slave SCL
40	GPIO8/TXD_SDA	DIO	General purpose IO 8 / RS-232 TXD / I2C Slave SDA
41	GPIO9/RTS	DIO	General purpose IO 9 / RS-232 RTS
42	GPIO10/CIR	DIO	General purpose IO 10 / Consumer IR input
43	VDD18_43	PWR	1.8V digital power supply
44	GND	GND	Ground
45	GPIOA0	DIO	General purpose IO 0
46	GPIOA1	DIO	General purpose IO 1
47	RESET_	DI	System reset (active low)
48	DT656IN_0	DI	ITU-R BT.656 data in 0
49	DT656IN_1	DI	ITU-R BT.656 data in 1
50	DT656IN_2	DI	ITU-R BT.656 data in 2
51	DT656IN_3	DI	ITU-R BT.656 data in 3
52	GND	GND	Ground
53	DT656IN_4	DI	ITU-R BT.656 data in 4
54	DT656IN_5	DI	ITU-R BT.656 data in 5
55	DT656IN_6	DI	ITU-R BT.656 data in 6
56	DT656IN_7	DI	ITU-R BT.656 data in 7
57	CK656IN	DI	ITU-R BT.656 data in Clock
58	VDD33	PWR	3.3V digital power supply
59	GND	GND	Ground
60	GND	GND	Ground
61	VDD18_61	PWR	1.8V digital power supply
62	GPIO15/KEY_DATA2	DIO	General purpose IO 15 / Keypad Data 2
63	GPIO14/KEY_DATA1	DIO	General purpose IO 14 / Keypad Data 1
64	GPIO13/KET_DATA0	DIO	General purpose IO 13 / Keypad Data 0

Pin number	Pin Name	I/O	Description
65	GPIO12/KEY_COL1	DIO	General purpose IO 12 / Keypad COL 1
66	GPIO11/KEY_COL0	DIO	General purpose IO 11 / Keypad COL 0
67	VSS	GND	Ground for SDRAM
68	SDR_VDD	PWR	Power supply for SDRAM

6.3. Recommended PCB Design

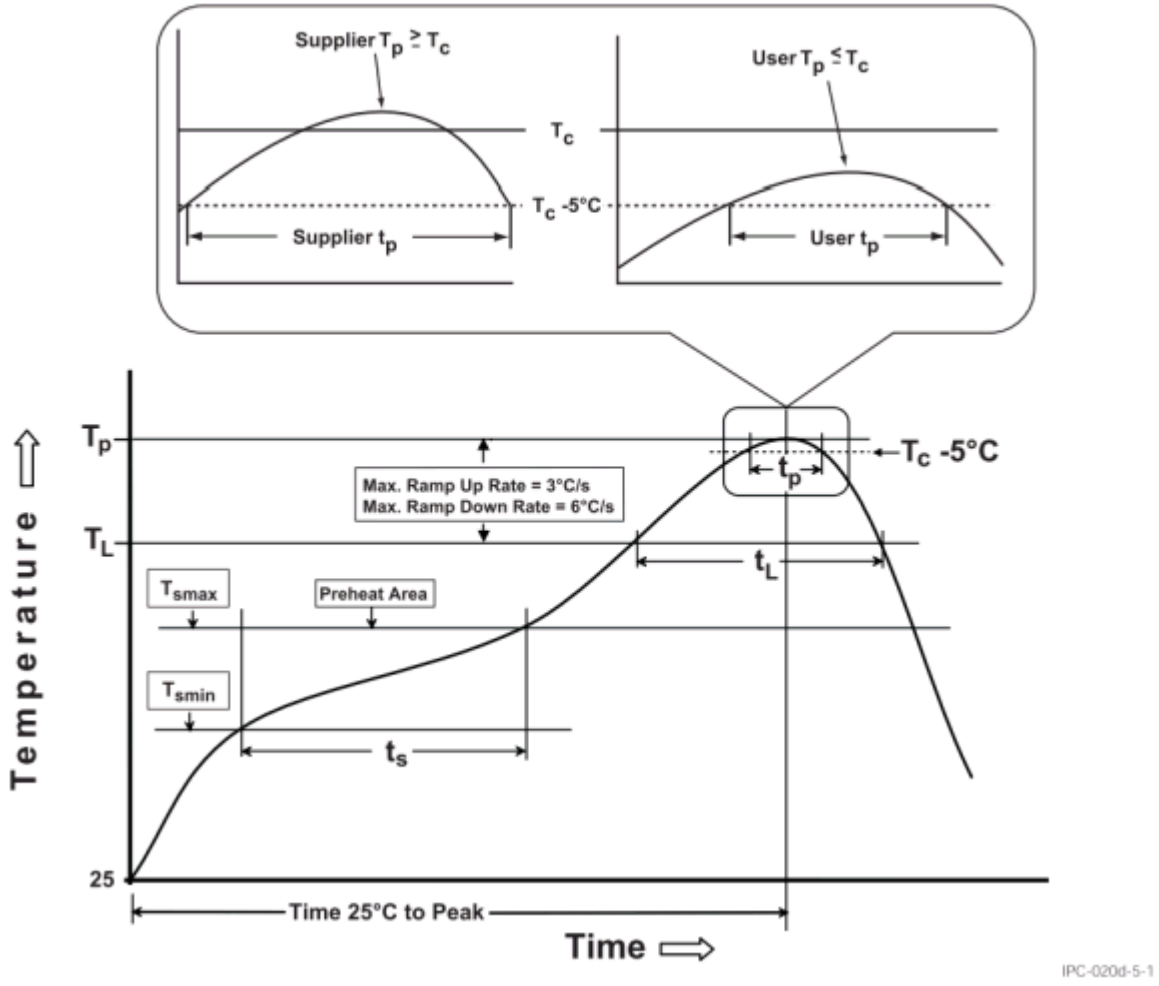


6.4. Recommended Stencil Design

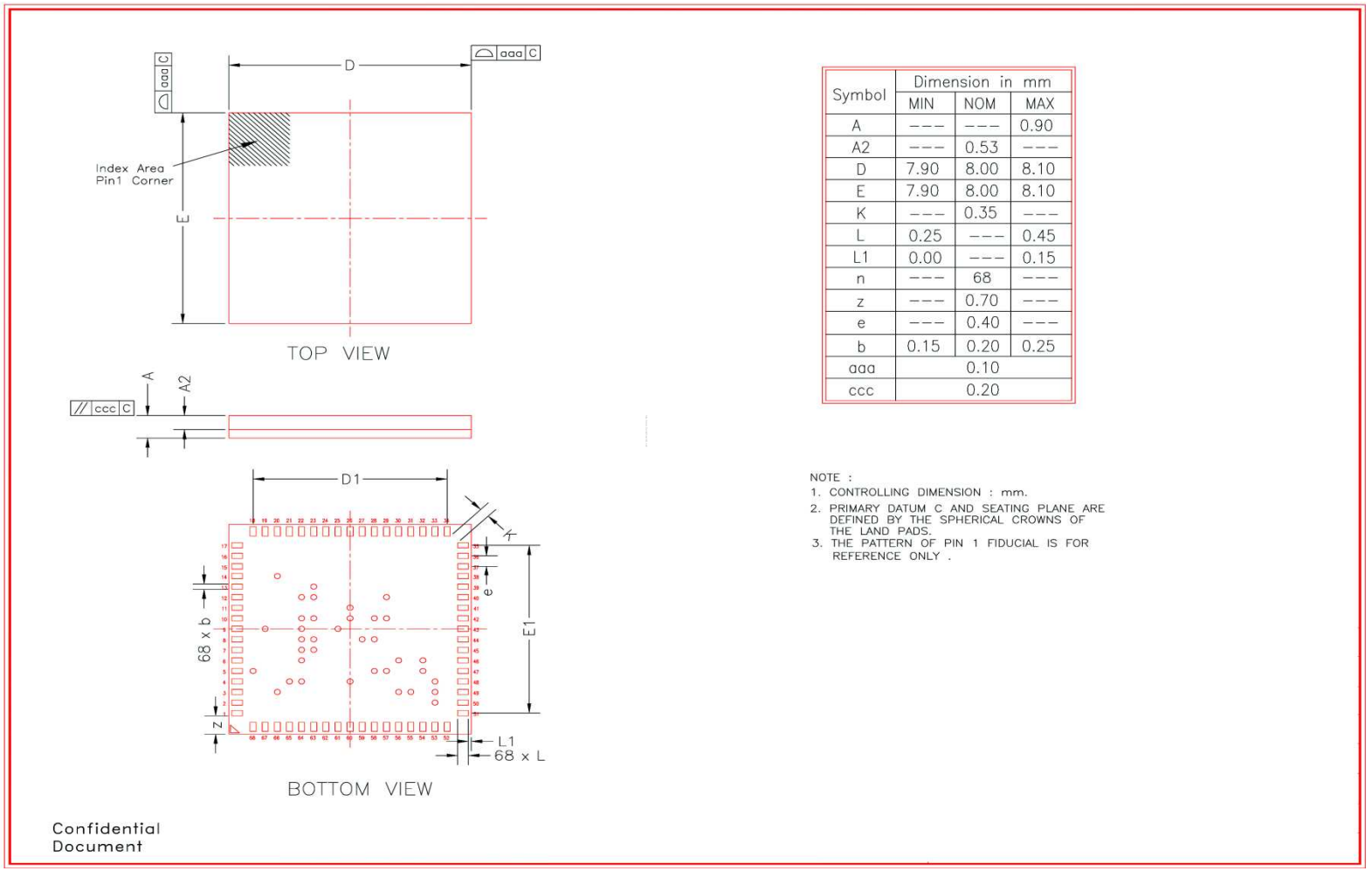
1. A laser-cut, stainless steel stencil with electro polished trapezoidal walls is recommended.
2. A 0.1mm (or less) stencil thickness is recommended.
3. The aperture width may need to be reduced slightly to help prevent solder bridging between adjacent I/O lands. (A 0.5mm x 0.2mm aperture size is recommended).
4. The following 2 parameters must be considered when designing aperture:
   Area Ratio: Area of Aperture open/ Aperture Wall Area=L*W/2T(L+W) > 0.66
   Aspect Ratio: Aperture With/ Stencil Thickness= W/T > 1.5
   where L is the Aperture Length; W is the Aperture Width and T is the Stencil Thickness.

6.5. Reflow Profile

Reflow condition	Parameter
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3 °C/second max.
Preheat - Temperature Min (T_s (min)) - Temperature Max (T_s (max)) - Time (min to max) (t_s)	 150 °C 200 °C 60- 180 seconds
T_s (max) to T_L - Ramp-up Rate	 3 °C/second max.
Time maintained above: - Temperature (T_L) - Time (t_L)	 217°C 60- 150 seconds
Peak Temperature (T_p)	245 +0/-5 °C
Time within 5 °C of actual Peak Temperature (T_p)	10- 30 seconds
Ramp-down Rate	6 °C/second max.
ime 25 °C to Peak Temperature	8 minutes max.



7. Package Dimensions



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	0.90
A2	---	0.53	---
D	7.90	8.00	8.10
E	7.90	8.00	8.10
K	---	0.35	---
L	0.25	---	0.45
L1	0.00	---	0.15
n	---	68	---
z	---	0.70	---
e	---	0.40	---
b	0.15	0.20	0.25
aaa		0.10	
ccc		0.20	

NOTE :
1. CONTROLLING DIMENSION : mm.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE LAND PADS.
3. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

8. Electrical Information

8.1. Voltage, Current, Power Consumption

Parameters at 27M input	Voltage	Current (Typical)	Watt (Typical)
Digital Internal Supply Current (VDD18)	1.8V	64mA	115.2mW
Digital I/O Supply Current (VDD33)	3.3V	10mA	33mW
SDRAM Supply Current (SDVDD33)	3.3V	14mA	46.2mW
DAC Supply Current (DAC33)	3.3V	45mA	148.5mW
8051 MCU (MVDD33)	3.3V	10mA	33mW
PLL Supply Current (PVDD18)	1.8V	5mA	9mW
Total	N/A	121mA	384.9mW

8.2. Recommend Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
VDD18	VDD18	1.71	1.8	1.89	V
VDD33	VDD33	3.13	3.3	3.46	V
Ambient Operating Temperature	TA	0		70	°C

8.3. DC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	VIH	2		5.5	V
Input Low Voltage (TTL)	VIL	-0.3		0.8	V
Input Leakage Current (@VI=2.5V or 0V)	IL			±10	µA
Input Capacitance	CIN		6		pF
Digital Outputs					
Output High Voltage	VOH	2.4			V
Output Low Voltage	VOL			0.4	V
High Level Output Current (@VOH=2.4V)	IOH	6.3	12.8	21.2	mA
Low Level Output Current (@VOL=0.4V)	IOL	4.9	7.4	9.8	mA
Tri-state Output Leakage Current (@VO=2.5V or 0V)	IOZ			±10	µA
Output Capacitance	CO		6		pF
Analog Pin Input Capacitance	CA		6		pF
Supply Current					
Analog Video Supply Current (VDD 18)	IDDV		44		mA
Digital I/O Supply Current (VDD33)	IDDO		25		mA

8.4. Serial Host Interface Timing

Parameter	Symbol	Min	Max	Units
Bus Free Time between STOP and START	tBF	1300		µs
SDA setup time	tsSDA	100		µs
SDA hold time	thSDA	200		µs
Setup time for START condition	tsSTA	600		µs
Setup time for STOP condition	tsSTOP	600		µs
Hold time for START condition	thSTA	600		µs
Rise time for SCL and SDA	tR		300	ns
Fall time for SCL and SDA	tF		300	ns
SCL clock frequency	fSCL		400	kHz

9. Control Register Descriptions

Frequently Used Abbreviations in Register Tables

RW = Read/Write
R = Read Only
CRW = Read/Write requiring the *Clear* action after writing '1' to the register
Bit No. = Bit Number (e.g. [7:0] means Bit 7 through Bit 0 involved)
(N/A) = Not Applicable
Ch. = Channel

Hexadecimal Notation

0xNN (NN is the hexadecimal number; e.g. 0x1F would have a decimal value of 31). For the ease of interpretation through out this document, all register addresses are denoted in UPPER case (e.g. 0xFF), and all data values are denoted in LOWER case (e.g. 0xff).

Binary Number Annotation 'b' (optional)

NNb (the 'b' denotes that the number NN is a binary number; e.g. 0111b would have a decimal value of 7)

9.1. De-Mist and Dynamic Range Correction (DRC) Registers (Page 0x00)

9.1.1. De-Mist and Dynamic Range Correction (DRC) Register Map

Pg. = 0x00	Module = De-Mist and DRC								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x00	reg_drc_updwn_en		reg_drc_lfrgt_en		reg_drc_detail_gain_auto	reg_drc_local_adj_auto	reg_drc_log_en	reg_drc_exp_en	0xff
0x01				drc_black_level					0x10
0x02	drc_lpf_select								0x1b
0x03	drc_local_edge								0x18
0x04	drc_mid_level								0xd7
0x05	drc_local_adj								0x00
0x06	drc_detail_limit								0xff
0x07	drc_detail_gain								0x80
0x08	drc_contrast								0x00
0x09				drc_chroma_422	drc_chroma_gain		drc_curve_sign	drc_line_sign	0x0c
0x0A	drc_saturation								0x00
0x0B				drc_brightness					0x10
0x0C	drc_ll_gain_lmt_y								0x60
0x0D					drc_ll_slope_lmt_y				0x0c
0x0E	drc_ll_gain_lmt_c								0x18
0x0F					drc_ll_slope_lmt_c				0x03
0x10						reg_dem_count_sft			0x02
0x11	reg_dem_high_num								0x54

Pg. = 0x00	Module = De-Mist and DRC								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x12							reg_dem_update_h_sft		0x02
0x13	reg_dem_low_num								0x15
0x14							reg_dem_update_l_sft		0x02
0x15	reg_drc_param_ctrl_auto				reg_drc_param_ctrl				0x8c
0x16					reg_dem_y_slope_ctrl				0x03
0x17				reg_dem_c_gain_slope					0x08
0x18	reg_dem_y_mix_ctrl_auto			reg_dem_y_mix_ctrl					0x90
0x19	reg_dem_c_mix_ctrl_auto			reg_dem_c_mix_ctrl					0x90
0x1A	reg_v_dem_en_c		reg_h_dem_en_c		reg_v_dem_en_y		reg_h_dem_en_y		0xff
0x1B			reg_dem_high_up_const						0x20
0x1C			reg_dem_high_dn_const						0x01
0x1D			reg_dem_low_up_const						0x01
0x1E			reg_dem_low_dn_const						0x20
0x1F	reg_dem_high_coring				reg_dem_low_coring				0x77
0x20		reg_dem_auto_black	reg_dem_auto_satur	reg_dem_auto_const			reg_dem_win_test	reg_dem_update_en	0x71
0x21		reg_dem_win_color							0x50
0x22	reg_dem_black_level								0x00
0x23	reg_dem_max_y_gain								0xff
0x24	reg_dem_max_c_gain								0xff
0x25 ↕ 0x27	Reserved								

Pg. = 0x00	Module = De-Mist and DRC								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x28	reg_dem_win_lt1								0x04
0x29	reg_dem_win_rt1								0x56
0x2A	reg_dem_win_up1								0x04
0x2B	reg_dem_win_dn1								0x1a
0x2C	reg_dem_win_lt2								0x04
0x2D	reg_dem_win_rt2								0x56
0x2E	reg_dem_win_up2								0x04
0x2F	reg_dem_win_dn2								0x1a
0x30	reg_dem_win_lt3								0x04
0x31	reg_dem_win_rt3								0x56
0x32	reg_dem_win_up3								0x04
0x33	reg_dem_win_dn3								0x1a
0x34	reg_dem_win_lt4								0x04
0x35	reg_dem_win_rt4								0x56
0x36	reg_dem_win_up4								0x04
0x37	reg_dem_win_dn4								0x1a
0x38	reg_dem_win_lt5								0x04
0x39	reg_dem_win_rt5								0x56
0x3A	reg_dem_win_up5								0x04
0x3B	reg_dem_win_dn5								0x1a
0x3C	reg_dem_win_lt6								0x04

Pg. = 0x00	Module = De-Mist and DRC								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x3D	reg_dem_win_rt6								0x56
0x3E	reg_dem_win_up6								0x04
0x3F	reg_dem_win_dn6								0x1a
0x40	reg_dem_win_lt7								0x04
0x41	reg_dem_win_rt7								0x56
0x42	reg_dem_win_up7								0x04
0x43	reg_dem_win_dn7								0x1a
0x44	reg_dem_win_lt8								0x04
0x45	reg_dem_win_rt8								0x56
0x46	reg_dem_win_up8								0x04
0x47	reg_dem_win_dn8								0x1a
0x48	reg_dem_win_en								0x01
0x49	reg_dem_win_xor								0x00
0x4A ↕ 0x4F	Reserved								

9.1.2. De-Mist and Dynamic Range Correction (DRC) Register Description

Pg. = 0x00	Module = De-Mist and DRC						
Register Address	Register Name	Width	Bit	Default Value	Access	Description	Category
0x00	reg_drc_exp_en	1	[0]	0x1	RW	DRC exponential block enable	DRC
	reg_drc_log_en	1	[1]	0x1	RW	DRC Logarithm block enable	
	reg_drc_local_adj_auto	1	[2]	0x1	RW	auto local adjust function enable	
	reg_drc_detail_gain_auto	1	[3]	0x1	RW	auto detail gain	
	reg_drc_lfrgt_en	2	[5:4]	0x3	RW	[5] Left DRC ON [4] Right DRC ON	
	reg_drc_updwn_en	2	[7:6]	0x3	RW	[7] Up DRC ON [6] Down DRC ON	
0x01	drc_black_level	5	[4:0]	0x10	RW	DRC black level of log2 unit	
	Reserved	3	[7:5]				
0x02	drc_lpf_select	8	[7:0]	0x1b	RW	DRC low-pass filter selection of luma level estimation	
0x03	drc_local_edge	8	[7:0]	0x18	RW	DRC local edge of luma level estimation	
0x04	drc_mid_level	8	[7:0]	0xd7	RW	DRC middle level of Luma Tone Mapping unit	
0x05	drc_local_adj	8	[7:0]	0x00	RW	DRC local adjust of Luma Tone Mapping unit	
0x06	drc_detail_limit	8	[7:0]	0xff	RW	DRC detail limit of adjustment unit	
0x07	drc_detail_gain	8	[7:0]	0x80	RW	DRC detail gain of adjustment unit	
0x08	drc_contrast	8	[7:0]	0x00	RW	DRC Luma adjustment - contrast of adjustment unit	
0x09	drc_line_sign	1	[0]	0x0	RW	DRC line sign bit of Luma Tone Mapping unit	
	drc_curve_sign	1	[1]	0x0	RW	DRC curve sign bit of Luma Tone Mapping unit	
	drc_chroma_gain	2	[3:2]	0x3	RW	DRC chroma gain of adjustment unit	
	drc_chroma_422	1	[4]	0x0	RW	DRC chroma even/odd pixel control	
	Reserved	3	[7:5]				
0x0A	drc_saturation	8	[7:0]	0x00	RW	DRC saturation of adjustment unit	
0x0B	drc_brightness	5	[4:0]	0x10	RW	DRC brightness for luma of Exponential unit	
	Reserved	3	[7:5]				
0x0C	drc_ll_gain_lmt_y	8	[7:0]	0x60	RW	DRC luma LL gain limit of adjustment unit	
0x0D	drc_ll_slope_lmt_y	4	[3:0]	0xc	RW	DRC luma LL slop limit of adjustment unit	
	Reserved	4	[7:4]				
0x0E	drc_ll_gain_lmt_c	8	[7:0]	0x18	RW	DRC chroma LL gain limit of adjustment unit	
0x0F	drc_ll_slope_lmt_c	4	[3:0]	0x3	RW	DRC chroma LL slop limit of adjustment unit	
	Reserved	4	[7:4]				

Pg. = 0x00	Module = De-Mist and DRC						
Register Address	Register Name	Width	Bit	Default Value	Access	Description	Category
0x10	reg_dem_count_sft	3	[2:0]	0x2	RW	Demist pixel counter shift value	De-Mist
	Reserved	5	[7:3]				
0x11	reg_dem_high_num	8	[7:0]	0x54	RW	Demist number of pixels above luma high limit	
0x12	reg_dem_update_h_sft	2	[1:0]	0x2	RW	Demist luma high limit shift value	
	Reserved	6	[7:2]				
0x13	reg_dem_low_num	8	[7:0]	0x15	RW	Demist number of pixels below luma low limit	
0x14	reg_dem_update_l_sft	2	[1:0]	0x2	RW	Demist luma low limit shift value	
	Reserved	6	[7:2]	0x00			
0x15	reg_drc_param_ctrl	4	[3:0]	0xc	RW	DRC manual parameter control value	
	Reserved	3	[6:4]	0x0			
	reg_drc_param_ctrl_auto	1	[7]	0x1	RW	DRC auto parameter control enable	
0x16	reg_dem_y_slope_ctrl	4	[3:0]	0x3	RW	Demist luma bright slope control	
	Reserved	4	[7:4]	0x0			
0x17	reg_dem_c_gain_slope	5	[4:0]	0x08	RW	Demist chroma dark gain slope control	
	Reserved	3	[7:5]	0x0			
0x18	reg_dem_y_mix_ctrl	5	[4:0]	0x10	RW	Demist manual luma mix control value	
	Reserved	2	[6:5]	0x0			
	reg_dem_y_mix_ctrl_auto	1	[7]	0x1	RW	Demist auto luma mix control enable	
0x19	reg_dem_c_mix_ctrl	5	[4:0]	0x10	RW	Demist manual chroma mix control value	
	Reserved	2	[6:5]	0x0			
	reg_dem_c_mix_ctrl_auto	1	[7]	0x1	RW	Demist auto chroma mix control enable	
0x1A	reg_h_dem_en_y	2	[1:0]	0x3	RW	[1] Left Demist Luma ON [0] Right Demist Luma ON	
	reg_v_dem_en_y	2	[3:2]	0x3	RW	[1] Up Demist Luma ON [0] Down Demist Luma ON	
	reg_h_dem_en_c	2	[5:4]	0x3	RW	[1] Left Demist Chroma ON [0] Right Demist Chroma ON	
	reg_v_dem_en_c	2	[7:6]	0x3	RW	[1] Up Demist Chroma ON [0] Down Demist Chroma ON	
0x1B	reg_dem_high_up_const	6	[5:0]	0x20	RW	Demist luma high limit upward time constant	
	Reserved	2	[7:6]	0x0			
0x1C	reg_dem_high_dn_const	6	[5:0]	0x01	RW	Demist luma high limit downward time constant	
	Reserved	2	[7:6]	0x0			
0x1D	reg_dem_low_up_const	6	[5:0]	0x01	RW	Demist luma low limit upward time constant	
	Reserved	2	[7:6]	0x0			
0x1E	reg_dem_low_dn_const	6	[5:0]	0x20	RW	Demist luma low limit downward time constant	
	Reserved	2	[7:6]	0x0			

Pg. = 0x00	Module = De-Mist and DRC						
Register Address	Register Name	Width	Bit	Default Value	Access	Description	Category
0X1F	reg_dem_low_coring	4	[3:0]	0x7	RW	Demist luma low limit variation coring	
	reg_dem_high_coring	4	[7:4]	0x7	RW	Demist luma high limit variation coring	
0x20	reg_dem_update_en	1	[0]	0x1	RW	Demist measurement update enable	
	reg_dem_win_test	1	[1]	0x0	RW	Demist measure window testing	
	Reserved	2	[3:2]	0x0			
	reg_dem_auto_const	1	[4]	0x1	RW	Demist auto contrast enable	
	reg_dem_auto_satur	1	[5]	0x1	RW	Demist auto saturation enable	
	reg_dem_auto_black	1	[6]	0x1	RW	Demist auto black level enable	
	Reserved	1	[7]	0x0			
0x21	reg_dem_win_color	7	[6:0]	0x50	RW	Demist measure window color for testing	
	Reserved	1	[7]	0x0			
0x22	reg_dem_black_level	8	[7:0]	0x00	RW	Demist manual black level	
0x23	reg_dem_max_y_gain	8	[7:0]	0xff	RW	Demist maximum luma gain (manual contrast)	
0x24	reg_dem_max_c_gain	8	[7:0]	0xff	RW	Demist maximum chroma gain (manual saturation)	
0x25	Reserved						
0x26	Reserved						
0x27	Reserved						
0x28	reg_dem_win_lt1	8	[7:0]	0x04	RW	Demist measure window 1 left border	
0x29	reg_dem_win_rt1	8	[7:0]	0x56	RW	Demist measure window 1 right border	
0x2A	reg_dem_win_up1	8	[7:0]	0x04	RW	Demist measure window 1 up border	
0x2B	reg_dem_win_dn1	8	[7:0]	0x1a	RW	Demist measure window 1 down border	
0x2C	reg_dem_win_lt2	8	[7:0]	0x04	RW	Demist measure window 2 left border	
0x2D	reg_dem_win_rt2	8	[7:0]	0x56	RW	Demist measure window 2 right border	
0x2E	reg_dem_win_up2	8	[7:0]	0x04	RW	Demist measure window 2 up border	
0x2F	reg_dem_win_dn2	8	[7:0]	0x1a	RW	Demist measure window 2 down border	
0x30	reg_dem_win_lt3	8	[7:0]	0x04	RW	Demist measure window 3 left border	
0x31	reg_dem_win_rt3	8	[7:0]	0x56	RW	Demist measure window 3 right border	
0x32	reg_dem_win_up3	8	[7:0]	0x04	RW	Demist measure window 3 up border	
0x33	reg_dem_win_dn3	8	[7:0]	0x1a	RW	Demist measure window 3 down border	
0x34	reg_dem_win_lt4	8	[7:0]	0x04	RW	Demist measure window 4 left border	
0x35	reg_dem_win_rt4	8	[7:0]	0x56	RW	Demist measure window 4 right border	
0x36	reg_dem_win_up4	8	[7:0]	0x04	RW	Demist measure window 4 up border	
0x37	reg_dem_win_dn4	8	[7:0]	0x1a	RW	Demist measure window 4 down border	
0x38	reg_dem_win_lt5	8	[7:0]	0x04	RW	Demist measure window 5 left border	

Pg. = 0x00	Module = De-Mist and DRC						
Register Address	Register Name	Width	Bit	Default Value	Access	Description	Category
0x39	reg_dem_win_rt5	8	[7:0]	0x56	RW	Demist measure window 5 right border	
0x3A	reg_dem_win_up5	8	[7:0]	0x04	RW	Demist measure window 5 up border	
0x3B	reg_dem_win_dn5	8	[7:0]	0x1a	RW	Demist measure window 5 down border	
0x3C	reg_dem_win_lt6	8	[7:0]	0x04	RW	Demist measure window 6 left border	
0x3D	reg_dem_win_rt6	8	[7:0]	0x56	RW	Demist measure window 6 right border	
0x3E	reg_dem_win_up6	8	[7:0]	0x04	RW	Demist measure window 6 up border	
0x3F	reg_dem_win_dn6	8	[7:0]	0x1a	RW	Demist measure window 6 down border	
0x40	reg_dem_win_lt7	8	[7:0]	0x04	RW	Demist measure window 7 left border	
0x41	reg_dem_win_rt7	8	[7:0]	0x56	RW	Demist measure window 7 right border	
0x42	reg_dem_win_up7	8	[7:0]	0x04	RW	Demist measure window 7 up border	
0x43	reg_dem_win_dn7	8	[7:0]	0x1a	RW	Demist measure window 7 down border	
0x44	reg_dem_win_lt8	8	[7:0]	0x04	RW	Demist measure window 8 left border	
0x45	reg_dem_win_rt8	8	[7:0]	0x56	RW	Demist measure window 8 right border	
0x46	reg_dem_win_up8	8	[7:0]	0x04	RW	Demist measure window 8 up border	
0x47	reg_dem_win_dn8	8	[7:0]	0x1a	RW	Demist measure window 8 down border	
0x48	reg_dem_win_en	8	[7:0]	0x01	RW	Demist measure window enable bits	
0x49	reg_dem_win_xor	8	[7:0]	0x00	RW	Demist measure window exclude bits	
0x50	dem_high_limit	8	[7:0]		R	Demist luma high limit readback	
0x51	dem_low_limit	8	[7:0]		R	Demist luma low limit readback	
0x52	drc_param_ctrl_r	4	[3:0]		R	DRC parameter control readback	
	Reserved	4	[7:4]				
0x53	drc_mix_ctrl_r	5	[4:0]		R	DRC mix control readback	
	Reserved	3	[7:5]				
0x54	dem_gain_val_r	8	[7:0]		R	Demist gain value readback	

9.2. VE Control Registers (Page 0x04)

9.2.1. VE Control Register Map (NTSC)

Pg. = 0x04	Module = VE Control								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x32	regn_vwidth[7:0]								0xf0
0x33					regn_vwidth[11:8]				0x00
0x34	regn_enc656_vtotal [7:0]								0x0d
0x35						regn_enc656_vtotal [10:8]			0x02
0x36 ↕ 0x3E	Reserved								
0x3F	update_n								0x00

9.2.2. VE Control Register Map (PAL)

Pg. = 0x04	Module = VE Control								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x72	regp_vwidth[7:0]								0x20
0x73					regp_vwidth[11:8]				0x01
0x74	regp_enc656_vtotal[7:0]								0x71
0x75						regp_enc656_vtotal[10:8]			0x02
0x76 ↕ 0x7E	Reserved								
0x7F	upate_p								0x00

9.2.3. VE Control Register Map (Control)

Pg. = 0x04	Module = VE Control								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x80				reg_sw_rst		reg_clkin_pol	reg_clkout_pol	reg_ck656_o_pol	0x10
0x81							reg_ve_pal_manual_en	reg_ve_pal_mode_auto	0x01
0x82								reg_power_down	0x00

9.2.4. VE Control Register Map (ITU-R BT.656)

Pg. = 0x04	Module = VE Control								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x90	regn_v656_hs_dly[7:0]								0x80
0x91					regn_v656_hs_dly[11:8]				0x00
0x92	regp_v656_hs_dly[7:0]								0x76
0x93					regp_v656_hs_dly[11:8]				0x00
0x94	reg_v656_vs_dly[7:0]								0x04
0x95					reg_v656_vs_dly[11:8]				0x00
0x96	reg_v656_de_dly[7:0]								0x00
0x97	reg_v656_de_wid[7:0]								0xd0
0x98	reg_v656_de_wid[11:8]				reg_v656_de_dly[11:8]				0x20
0x99	reg_v656_hs_wid[7:0]								0x0a
0x9A	reg_v656_vs_wid[7:0]								0x01
0x9B	reg_v656_vs_wid[11:8]				reg_v656_hs_wid[11:8]				0x00
0x9C	reg_v656_f0_dly								
0x9D	reg_v656_f1_dly								
0x9E	Reserved								
0x9F	update_656								0x00

9.2.5. VE Control Register Description

Pg. = 0x04	Module = VE Control						
Register Address	Register Name	Width	Bit	Access	Default Value	Description	Category
0x32	regn_vwidth[7:0]	8	[7:0]	RW	0xf0	NTSC vertical active line width[7:0]	NTSC
0x33	regn_vwidth[11:8]	4	[3:0]	RW	0x0	NTSC vertical active line width[11:8]	
	Reserved	4	[7:4]				
0x34	regn_enc656_vtotal[7:0]	8	[7:0]	RW	0x0d	NTSC total line width[7:0]	
0x35	regn_enc656_vtotal[10:8]	3	[2:0]	RW	0x2	NTSC total line width[10:8]	
	Reserved	5	[7:3]				
0x3f	Reserved	7	[6:0]				
	update_n	1	[7]	RW	0x0	NTSC parameters update	
0x72	regp_vwidth[7:0]	8	[7:0]	RW	0x20	PAL vertical active line width[7:0]	PAL
0x73	regp_vwidth[11:8]	4	[3:0]	RW	0x1	PAL vertical active line width[11:8]	
	Reserved	4	[7:4]				
0x74	regp_enc656_vtotal[7:0]	8	[7:0]	RW	0x71	PAL total line width[7:0]	
0x75	regp_enc656_vtotal[10:8]	3	[2:0]	RW	0x2	PAL total line width[10:8]	
	Reserved	5	[7:3]				
0x7F	Reserved	7	[6:0]				
	update_p	1	[7]	RW	0x0	PAL parameters update	
0x80	reg_ck656_o_pol	1	[0]	RW	0x0	656 out polarity	Control
	reg_clkout_pol	1	[1]	RW	0x0	clock out polarity	
	reg_clkin_pol	1	[2]	RW	0x0	clock in polarity	
	Reserved	1	[3]				
	reg_sw_rst	1	[4]	RW	0x1	software reset (active low)	
	Reserved	3	[7:5]				
0x81	reg_ve_pal_mode_auto	1	[0]	RW	0x1	pal mode auto detection enable	
	reg_ve_pal_manual_en	1	[1]	RW	0x0	pal mode manual enable	
	Reserved	6	[7:2]				
0x82	reg_power_down	1	[0]	RW	0x0	power down enable	
	Reserved	7	[7:1]				
0x83 ~ 0x8F	Reserved						

Pg. = 0x04	Module = VE Control						
Register Address	Register Name	Width	Bit	Access	Default Value	Description	Category
0x90	regn_v656_hs_dly[7:0]	8	[7:0]	RW	0x80	NTSC ITU-R BT.656 hsync delay[7:0]	656
0x91	regn_v656_hs_dly[11:8]	4	[3:0]	RW	0x0	NTSC ITU-R BT.656 hsync delay[11:8]	
	Reserved	4	[7:4]				
0x92	regp_v656_hs_dly[7:0]	8	[7:0]	RW	0x76	PAL ITU-R BT.656 hsync delay[7:0]	
0x93	regp_v656_hs_dly[11:8]	4	[3:0]	RW	0x0	PAL ITU-R BT.656 hsync delay[11:8]	
	Reserved	4	[7:4]				
0x94	reg_v656_vs_dly[7:0]	8	[7:0]	RW	0x04	ITU-R BT.656 vsync delay[7:0]	
0x95	reg_v656_vs_dly[11:8]	4	[3:0]	RW	0x0	ITU-R BT.656 vsync delay[11:8]	
	Reserved	4	[7:4]				
0x96	reg_v656_de_dly[7:0]	8	[7:0]	RW	0x00	ITU-R BT.656 hde delay[7:0]	
0x97	reg_v656_de_wid[7:0]	8	[7:0]	RW	0xd0	ITU-R BT.656 hde delay width [7:0]	
0x98	reg_v656_de_dly[11:8]	4	[3:0]	RW	0x0	ITU-R BT.656 hde delay[11:8]	
	reg_v656_de_wid[11:8]	4	[7:4]	RW	0x2	ITU-R BT.656 hde delay width [11:8]	
0x99	reg_v656_hs_wid[7:0]	8	[7:0]	RW	0x0a	ITU-R BT.656 hsync width[7:0]	
0x9A	reg_v656_vs_wid[7:0]	8	[7:0]	RW	0x01	ITU-R BT.656 vsync width[7:0]	
0x9B	reg_v656_hs_wid[11:8]	4	[3:0]	RW	0x0	ITU-R BT.656 hsync width[11:8]	
	reg_v656_vs_wid[11:8]	4	[7:4]	RW	0x0	ITU-R BT.656 vsync width[11:8]	
0x9C	reg_v656_f0_dly	8	[7:0]	RW	0x00	ITU-R BT.656 field 0 delay[7:0]	
0x9D	reg_v656_f1_dly	8	[7:0]	RW	0x00	ITU-R BT.656 field 1 delay[7:0]	
0x9F	update_656	1	[8]	RW	0x0	ITU-R BT.656 update	
	Reserved	7	[6:0]				

9.3. Noise Reduction Control Registers (Page 0x09)

9.3.1. Noise Reduction Control Register Map

Pg. = 0x09	Module = Noise Reduction								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0xC8	reg_split_scn_cnt[7:0]								0x68
0xC9	reg_split_scn_cnt[10:8]								0x01
0xCA			reg_split_scn_ctrl		reg_3D_nr_enable				0x30
0xCB	reg_s_nr_y_pxl_en[7:0]								0xff
0xCC			reg_s_nr_y_pxl_en[13:8]						0x3f
0xCF	reg_dnr_auto								0x80

9.3.2. Noise Reduction Control Register Description

Pg. = 0x09	Module = Noise Reduction					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0xC8	reg_split_scn_cnt[7:0]	8	[7:0]	RW	0x68	Split screen count value [7:0]
0xC9	Reserved	5	[4:0]	RW		
	reg_split_scn_cnt[10:8]	3	[7:5]	RW	0x2	Split screen count value [10:8]
0xCA	reg_3D_nr_enable	4	[3:0]	RW	0x0	3D NR Enable [SNRY:SNRC:TNRY:TNRC]
	reg_split_scn_ctrl	2	[5:4]	RW	0x3	Split screen control [right:left]
	Reserved	1	[6]			
	Reserved	1	[7]			
0xCB	reg_s_nr_y_pxl_en[7:0]	8	[7:0]	RW	0xff	SNR luma pixel enable[7:0]
0xCC	reg_s_nr_y_pxl_en[13:8]	6	[5:0]	RW	0x3f	SNR luma pixel enable[13:8]
	Reserved	2	[7:6]			
0xCD	reg_s_nr_c_pxl_en	5	[4:0]	RW	0x1f	SNR chroma pixel enable
	reg_t_nr_y_mc_en	1	[5]	RW	0x1	TNR luma motion compensate enable
	Reserved	1	[6]			
	Reserved	1	[7]			
0xCF	Reserved	4	[3:0]			
	Reserved	3	[6:4]			
	reg_dnr_auto	1	[7]	RW	0x1	Auto DNR enable

9.4. I2C Master Block Registers (Page 0x0B)

9.4.1. I2C Master Block Register Map

Pg. = 0x0B	Module = I2C Master								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x00	I2CM_SCLC								0x00
0x01	I2C_SID							I2CM_RWC	0x00
0x02	I2CM_WR_ADDR_4_READ	I2CM_SEND_START							0x00
0x03	I2CM_AD								0x00
0x04	I2CM_START	I2CM_BURST_EN	I2CM_FINISH	I2CM_OK2READ	I2CM_FAIL	I2CM_MODE		I2CM_PIN_CTL	0x00
0x05									
0x06									
0x07	**I2CM_DIR_SCL_IN***			**I2CM_DIR_SCL_OUT#**	**I2CM_DIR_SDA_IN**			**I2CM_DIR_SDA_OUT**	0xff

9.4.2. I2C Master Block Register Description

Pg. = 0x0B	Module = I2C Master					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x00	I2CM_SCLC	8	[7:0]	RW	0x00	I2C Master Serial Clock Speed Control. Serial Clock Speed = [XCLK] / (Register's decimal value * 2) Recommended initial value = 87h = 135d (Serial Clock Speed = 27MHz / (135 x 2) = 100Kbps)
0x01	I2CM_RWC	1	[0]	RW	0x0	I2C Master Block Slave Device Read Write Control bit. 1b: I2C Read Command 0b: I2C Write Command
	I2CM_SID	7	[7:1]	RW	0x00	I2C Master Block Slave Device ID
0x02	Reserved	6	[5:0]			
	I2CM_SEND_START	1	[6]	RW	0x0	I2C Master restart or finish before read operation. 1b : Restart before read operation 0b : Finish before read operation
	I2CM_WR_ADDR_4_READ	1	[7]	RW	0x0	I2C Master "address write" before read operation. 1b : Address write before read operation 0b : No address write before read operation
0x03	I2CM_AD	8	[7:0]	RW	0x00	I2C Master Slave Device Sub-Register's Data

Pg. = 0x0B	Module = I2C Master					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x04	I2CM_PIN_CTL	1	[0]	RW	0x0	I2C Master pin direct control enable 1b : Direct control by 0b : Disable direct control
	I2CM_MODE	2	[2:1]	RW	0x0	I2C Master Mode Select: 00b: Standard mode. ~100Kbps – 50/50 Duty Cycle 01b: Fast Mode. ~400Kbps – 50/50 Duty Cycle 10b: High Speed Mode. Up to 3.4Mbps – 50/50 Duty Cycle 11b: High Speed Mode Up to 3.4Mbps – 1:2 Duty Cycle
	I2CM_FAIL	1	[3]	RW	0x0	I2C Master Fail to Receive Acknowledgement from Slave Device 0b: ACK received from slave device. 1b: No ACK received from slave device
	I2CM_OK2READ	1	[4]	RW	0x0	I2C Master Block finishes acquiring read data; I2C Master will set this bit to '1'. The CPU needs to clear this bit.
	I2CM_FINISH	1	[5]	RW	0x0	I2C Master Block Finish Read/Write Data Indicator. After the I2C Master block finish Read/Write the data, I2C Master will set this bit and CPU needs to clear this bit.
	I2CM_BURST_EN	1	[6]	RW	0x0	I2C Master Block Read Burst Control Enable 1b : Enable 0b : Disable
	I2CM_START	1	[7]	RW	0x0	I2C Master Block Start Sending Data Indicator. After the MCU writes the first data into I2C Master block, the I2CM_START will be pulled high ("1b") by MCU to indicate the start of I2C bus toggling. Once it is done, the MCU will set the I2CM_START to low ("0b").
0x05	Reserved	8	[7:0]			
0x06	Reserved	8	[7:0]			
0x07	I2CM_DIR_SDA_OUT	1	[0]	W	0x0	I2C Master SDA Direction OUT
	Reserved	2	[2:1]			
	I2CM_DIR_SDA_IN	1	[3]	R	0x1	I2C Master SDA Direction IN (Default)
	I2CM_DIR_SCL_OUT	1	[4]	W	0x0	I2C Master SCL Direction OUT
	Reserved	2	[6:5]			
	I2CM_DIR_SCL_IN	1	[7]	R	0x1	I2C Master SCL Direction IN (Default)

9.5. SPI Master 0 Block Registers (Page 0x0C)

9.5.1. SPI Master 0 Block Register Map

Pg. = 0x0C	Module = SPI Master 0								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x00	SPI_START_0	SPI_CS_POL_0	SPI_SCLK_IDLE_POL_0	SPI_SCLK_PHASE_0	SPI_SCLK_DIV_SEL_0				0x00
0x01	SPI_TBYTE_CNT_0								0x00
0x02	SPI_RBYTE_CNT_0								0x00
0x03	**SPI_REC_DATA_0***								
	SPI_TRAN_DATA_0#								
0x04					SPI_INT_MASK_0				0x00
0x05					SPI_INT_SET_0				0x00
0x06					SPI_INT_STATUS_0				0x00
0x07								SPI_WP	0x00
0x08 ~ 0xFF	Reserved								

9.5.2. SPI Master 0 Block Register Description

Pg. = 0x0C	Module = SPI Master 0					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x00	SPI_SCLK_DIV_SEL_0	4	[3:0]	RW	0x0	SCLK divider selection. 0000b: divided by 2 0001b: divided by 4 0010b: divided by 8 0011b: divided by 16 0100b: divided by 32 0101b: divided by 64 0110b: divided by 128 0111b: divided by 256 1000b: divided by 512 1001b: divided by 1024 1010b: divided by 2048 1011b: divided by 4096 1100b: divided by 8192 All the others: divided by 2
	SPI_SCLK_PHASE_0	1	[4]	RW	0x0	SCLK phase.
	SPI_SCLK_IDLE_POL_0	1	[5]	RW	0x0	SCLK idle polarity.
	SPI_CS_POL_0	1	[6]	RW	0x0	CS polarity.
	SPI_START_0	1	[7]	RW	0x0	Write '1' to start SPI transmission. It will be reset to '0' after every transmission.
0x01	SPI_TBYTE_CNT_0	8	[7:0]	RW	0x00	SPI transmit byte count.
0x02	SPI_RBYTE_CNT_0	8	[7:0]	RW	0x00	SPI expected receive byte count.
0x03	SPI_REC_DATA_0	8	[7:0]	R		SPI received data.
	SPI_TRAN_DATA_0	8	[7:0]	W		SPI transmit data.
0x04	SPI_INT_MASK_0	4	[3:0]	RW	0x0	SPI interrupt mask. [3]: write fifo full [2]: write fifo empty [1]: read fifo full [0]: read fifo empty
	Reserved	4	[7:4]			

Pg. = 0x0C	Module = SPI Master 0					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x05	SPI_INT_SET_0	4	[3:0]	RW	0x0	SPI interrupt polarity set. [3]: write fifo full [2]: write fifo empty [1]: read fifo full [0]: read fifo empty
	Reserved	4	[7:4]			
0x06	SPI_INT_STATUS_0	4	[3:0]	RW	0x0	SPI interrupt status. [3]: write fifo full [2]: write fifo empty [1]: read fifo full [0]: read fifo empty
	Reserved	4	[7:4]			
0x07	SPI_WP	1	[0]	RW	0x0	SPI write protection direct control.
	Reserved	7	[7:1]			

9.6. SPI Master 1 Block Registers (Page 0x0D)

9.6.1. SPI Master 1 Block Register Map

Pg. = 0x0D	Module = SPI Master 1								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x00	SPI_START_1	SPI_CS_POL_1	SPI_SCLK_IDLE_POL_1	SPI_SCLK_PHASE_1	SPI_SCLK_DIV_SEL_1				0x00
0x01	SPI_TBYTE_CNT_1								0x00
0x02	SPI_RBYTE_CNT_1								0x00
0x03	**SPI_REC_DATA_1***								
	SPI_TRAN_DATA_1#								
0x04					SPI_INT_MASK_1				0x00
0x05					SPI_INT_SET_1				0x00
0x06					SPI_INT_STATUS_1				0x00
0x07 ~ 0xFF	Reserved								

9.6.2. SPI Master 1 Block Register Description

Pg. = 0x0D	Module = SPI Master 1					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x00	SPI_SCLK_DIV_SEL_1	4	[3:0]	RW	0x0	SCLK divider selection. 0000b: divided by 2 0001b: divided by 4 0010b: divided by 8 0011b: divided by 16 0100b: divided by 32 0101b: divided by 64 0110b: divided by 128 0111b: divided by 256 1000b: divided by 512 1001b: divided by 1024 1010b: divided by 2048 1011b: divided by 4096 1100b: divided by 8192 All the others: divided by 2
	SPI_SCLK_PHASE_1	1	[4]	RW	0x0	SCLK phase.
	SPI_SCLK_IDLE_POL_1	1	[5]	RW	0x0	SCLK idle polarity.
	SPI_CS_POL_1	1	[6]	RW	0x0	CS polarity.
	SPI_START_1	1	[7]	RW	0x0	Write ‘1’ to start SPI transmission. It will be reset to ‘0’ after every transmission.
0x01	SPI_TBYTE_CNT_1	8	[7:0]	RW	0x00	SPI transmit byte count.
0x02	SPI_RBYTE_CNT_1	8	[7:0]	RW	0x00	SPI expected receive byte count.
0x03	SPI_REC_DATA_1	8	[7:0]	R		SPI received data.
	SPI_TRAN_DATA_1	8	[7:0]	W		SPI transmit data.
0x04	SPI_INT_MASK_1	4	[3:0]	RW	0x0	SPI interrupt mask. [3]: write fifo full [2]: write fifo empty [1]: read fifo full [0]: read fifo empty
	Reserved	4	[7:4]			

Pg. = 0x0D	Module = SPI Master 1					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x05	SPI_INT_SET_1	4	[3:0]	RW	0x0	SPI interrupt polarity set. [3]: write fifo full [2]: write fifo empty [1]: read fifo full [0]: read fifo empty
	Reserved	4	[7:4]			
0x06	SPI_INT_STATUS_1	4	[3:0]	RW	0x0	SPI interrupt status. [3]: write fifo full [2]: write fifo empty [1]: read fifo full [0]: read fifo empty
	Reserved	4	[7:4]			

9.7. GPIO Block Registers (Page 0x0E)

Registers for General Purpose Input/Output blocks are listed in this section.

9.7.1. GPIO Port Configuration

The following table shows the GPIO pin configuration:

GPIO Port I/O Pad Name	Configured As		
	IN	OUT	Type
GPIOA0	-	SPI_CS1	O
GPIOA1	-	SPI_CS1	O
GPIO2	SPI_DIO1		I/O
GPIO3	-	SPI_CS1	O
GPIO4	-	SPI_CLK1	O
GPIO5	M_SCL		I/O
GPIO6	M_SDA		I/O
GPIO7	RXD_SCL	-	I
GPIO8	-	TXD_SDA	O
GPIO9	-	RTS	O
GPIO10	CIR	-	I
GPIO11	-	KB_COL0	O
GPIO12	-	KB_COL1	O
GPIO13	KB_DATA0	-	I
GPIO14	KB_DATA1	-	I
GPIO15	KB_DATA2	-	I

9.7.2. GPIO Block Register Map

Pg. = 0x0E	Module = GPIO								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x00	CIR_IN_POLARITY	CIR_DF_EN	CIR_EN	RS485_EN	RS232_EN	M_I2C_EN	SPI1_EN	KB_EN	0Xbf
0x01	CIR_MODE		CIR_CLK_DIVIDER						0x90
0x02	**CIR_COUNT_MAX***				**CIR_COUNT_MIN**				
0x03	**CIR_D0[7:0]**								
0x04	**CIR_D1[7:0]**								
0x05	**CIR_D2[7:0]**								
0x06	**CIR_D3[7:0]**								
0x07	**CIR_D4[7:0]**								
0x08	**CIR_D5[7:0]**								
0x09	**CIR_REPEAT**	**CIR_READY**	**CIR_BIT_COUNT[5:0]**						
0x0A	CIR_PON_D0[7:0]								0x00
0x0B	CIR_PON_D1[7:0]								0x00
0x0C	CIR_PON_D2[7:0]								0x00
0x0D	CIR_PON_D3[7:0]								0x00
0x0E	CIR_PON_D4[7:0]								0x00
0x0F	CIR_PON_D5[7:0]								0x00
0x10	KB_SCAN_LOW				KB_SCAN_HIGH				0xaa
0x11		**KEY_COL1_DATA[2:0]***				**KEY_COL0_DATA[2:0]**			
0x12	GPIOA_MODE[7:0]								0x00
0x13	GPIOA_MODE[15:8]								0x00

Pg. = 0x0E	Module = GPIO								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x14	GPIOA_DATA[7:0]								0x00
0x15	GPIOA_DATA[15:8]								0x00
0x16	GPIOA_INT_MSK[7:0]								0x00
0x17	GPIOA_INT_MSK[15:8]								0x00
0x18	GPIOA_INT_POL[7:0]								0x00
0x19	GPIOA_INT_POL[15:8]								0x00
0x1A	**GPIOA_INT_REQ[7:0]**								
0x1B	**GPIOA_INT_REQ[15:8]**								
0x1C	**GPIOA_INT_INP[7:0]**								
0x1D	**GPIOA_INT_INP[15:8]**								
0x1E						SPI_CS_EN[1:0]		RS485_RTS_POL	0x00

9.7.3. GPIO Block Register Description

Pg. = 0x0E	Module = GPIO					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x00	KB_EN	1	[0]	RW	0x1	Scan Key Matrix & GPIO pin MUX selection control 1 : Enable Scan Key Matrix controller 0 : Disable Scan Key Matrix controller, the Scan Key Matrix controller pins become GPIO Port bit [15:11].
	SPI1_EN	1	[1]	RW	0x1	SPI Master 1 & GPIO pin MUX selection control 1 : Enable SPI Master 1 0 : Disable SPI Master 1, the SPI Master 1 pins become GPIO Port bit [4:2].
	M_I2C_EN	1	[2]	RW	0x1	I2C Master & GPIO pin MUX selection control 1: Select I2C Master 0: Disable I2C Master, the I2C Master pins become GPIO Port bit [6:5].
	RS232_EN	1	[3]	RW	0x1	RS232 pin MUX selection control 1: Enable TXD/RXD, 0: Disable TXD/RXD, the TXD/RXD pins become GPIO Port bit [8:7].
	RS485_EN	1	[4]	RW	0x1	RTS pin MUX selection control 1: Enable RTS. 0: Disable RTS, the RTS pin becomes GPIO Port bit[9].
	CIR_EN	1	[5]	RW	0x1	CIR function Enable 1: Enable CIR block, which sets the CIR pin for CIR input only. 0: Disable CIR block, the CIR pin becomes GPIO Pot bit[10].
	CIR_DF_EN	1	[6]	RW	0x0	CIR Digital Filter Enable 1: Enable the carrier frequency filter function in CIR block. 0: Disable the carrier frequency filter function in CIR block.
	CIR_IN_POLARITY	1	[7]	RW	0x1	CIR input polarity selection
0x01	CIR_CLK_DIVIDER	6	[5:0]	RW	0x10	CIR Clock divider value. Used to divide the input slow clock to generate the 8X sample clock.
	CIR_MODE	2	[7:6]	RW	0x2	CIR Mode control register 00: Bypass raw data mode 01: Philip PC-5 mode, 1.8ms bit rate, Manchester coding 10: NEC mode, 1.12ms logic 0, 2.24ms logic 1 11: Sony mode, 1.2 ms high logic 1, 600 us logic 0,

Pg. = 0x0E	Module = GPIO					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x02	CIR_COUNT_MIN	4	[3:0]	RW	0x0	Minimum clock count for one period
	CIR_COUNT_MAX	4	[7:4]	RW	0x0	Maximum clock count for one period
0x03	CIR_D0[7:0]	8	[7:0]	R		CIR received byte 0
0x04	CIR_D1[7:0]	8	[7:0]	R		CIR received byte 1
0x05	CIR_D2[7:0]	8	[7:0]	R		CIR received byte 2
0x06	CIR_D3[7:0]	8	[7:0]	R		CIR received byte 3
0x07	CIR_D4[7:0]	8	[7:0]	R		CIR received byte 4
0x08	CIR_D5[7:0]	8	[7:0]	R		CIR received byte 5
0x09	CIR_BIT_COUNT[5:0]	6	[5:0]	R		CIR received valid bit count
	CIR_READY	1	[6]	R		CIR ready status bit
	CIR_REPEAT	1	[7]	R		CIR repeat status bit
0x0A	CIR_PON_D0[7:0]	8	[7:0]	RW	0x00	CIR power switch code byte 0
0x0B	CIR_PON_D1[7:0]	8	[7:0]	RW	0x00	CIR power switch code byte 1
0x0C	CIR_PON_D2[7:0]	8	[7:0]	RW	0x00	CIR power switch code byte 2
0x0D	CIR_PON_D3[7:0]	8	[7:0]	RW	0x00	CIR power switch code byte 3
0x0E	CIR_PON_D4[7:0]	8	[7:0]	RW	0x00	CIR power switch code byte 4
0x0F	CIR_PON_D5[7:0]	8	[7:0]	RW	0x00	CIR power switch code byte 5
0x10	KB_SCAN_HIGH	4	[3:0]	RW	0xa	Keyboard scan high duration control
	KB_SCAN_LOW	4	[7:4]	RW	0xa	Keyboard scan low duration control
0x11	KB_COL0_DATA[2:0]	3	[2:0]	R		Key data input from Column 0 (Controlled by KBCOL0)
	Reserved	1	[3]			
	KB_COL1_DATA[2:0]	3	[6:4]	R		Key data input from Column 1 (Controlled by KBCOL1)
	Reserved	1	[7]			
0x12	GPIOA_MODE[7:0]	8	[7:0]	RW	0x00	Control GPIO I/O Mode bit [7:0] 1b: Output Mode 0b: Input Mode
0x13	GPIOA_MODE[15:8]	8	[7:0]	RW	0x00	Control GPIO I/O Mode bit [15:8] 1b: Output Mode 0b: Input Mode
0x14	GPIOA_DATA[7:0]	8	[7:0]	RW	0x00	GPIOA data [7:0] Write : output data Read : GPIO pin status (input data)

Pg. = 0x0E	Module = GPIO					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x15	GPIOA_DATA[15:8]	8	[7:0]	RW	0x00	GPIOA data [15:8] Write : output data Read : GPIO pin status (input data)
0x16	GPIOA_INT_MSK[7:0]	8	[7:0]	RW	0x00	GPIOA Interrupt mask [7:0] 1b: Interrupt un-masked 0b: Interrupt masked
0x17	GPIOA_INT_MSK[15:8]	8	[7:0]	RW	0x00	GPIOA Interrupt mask [15:8] 1b: Interrupt un-masked 0b: Interrupt masked
0x18	GPIOA_INT_POL[7:0]	8	[7:0]	RW	0x00	GPIOA Interrupt polarity [7:0] 1b: low level interrupt 0b: high level interrupt
0x19	GPIOA_INT_POL[15:8]	8	[7:0]	RW	0x00	GPIOA Interrupt polarity [15:8] 1b: low level interrupt 0b: high level interrupt
0x1A	GPIOA_INT_REQ[7:0]	8	[7:0]	R		GPIOA Interrupt Request Status [7:0] 1b: Interrupt request 0b: no interrupt request
0x1B	GPIOA_INT_REQ[15:8]	8	[7:0]	R		GPIOA Interrupt Request Status [15:8] 1b: Interrupt request 0b: no interrupt request
0x1C	GPIOA_INT_INP[7:0]	8	[7:0]	R		GPIOA Interrupt un-Masked Request Status [7:0] 1b: Interrupt request 0b: no interrupt request
0x1D	GPIOA_INT_INP[15:8]	8	[7:0]	R		GPIOA Interrupt un-Masked Request Status [15:8] 1b: Interrupt request 0b: no interrupt request
0x1E	RS485_RTS_POL	1	[0]	RW	0x0	Set RTS output polarity
	SPI_CS_EN[1:0]	2	[2:1]	RW	0x0	SPI_CS & GPIO pin MUX selection control [1] : Redirect SPI_CS1 to GPIO1 [0] : Redirect SPI_CS1 to GPIO0
	Reserved	5	[7:3]			

9.8. CLK_GEN Registers (Page 0x0F)

9.8.1. CLK_GEN Register Map

Pg. = 0x0F	Module = clk_gen								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x00	memclk_o_pol	cpu_clk_sel	dac_clk_pol	dac_clk_sel	ck656_out_pol	656_out_sel	ck656_pol	ck656_sel	0x00
0x01	mem_clk_div				cpu_clk_div				0x28
0x02	tm_1ms_cnt[7:0]								0xbc
0X03	tm_1ms_cnt[15:8]								0x34
0X04	pll_m[8]						pll_bypass	pll_pwd	0x00
0X05	pll_m[7:0]								0x26
0X06				pll_n					0x04
0x07 ~ 0x0C	Reserved								
0X0D								mem_ref_sel	0x00

9.8.2. CLK_GEN Register Description

Pg. = 0x0F	Module = clk_gen					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x00	ck656_sel	1	[0]	RW	0x0	656 clock selection 1: xclk 0: 656 clk input
	ck656_pol	1	[1]	RW	0x0	656 polarity 1: invert 0: normal
	ck656_out_sel	1	[2]	RW	0x0	656 out clock selection 1: xclk 0: 656 clock input
	ck656_out_pol	1	[3]	RW	0x0	656 out clock polarity 1: invert 0: normal
	dac_clk_sel	1	[4]	RW	0x0	DAC clock selection 1: xclk 0: 656 clock input
	dac_clk_pol	1	[5]	RW	0x0	DAC clock polarity 1: invert 0: normal
	cpu_clk_sel	1	[6]	RW	0x0	CPU clock selection 1: cpu_clk_div 0: xclk
	memclk_o_pol	1	[7]	RW	0x0	Memory clock polarity 1: invert 0: normal

Pg. = 0x0F	Module = clk_gen					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x01	cpu_clk_div	4	[3:0]	RW	0x8	CPU clock divider 0000b: divided by 1 0001b: divided by 1.5 0010b: divided by 2 0011b: divided by 3 0100b: divided by 4 0101b: divided by 5 0110b: divided by 6 0111b: divided by 7 1000b: divided by 8 1001b: divided by 9 1010b: divided by 10 1011b: divided by 11 1100b: divided by 12 1101b: divided by 13 1110b: divided by 14 1111b: divided by 15
	mem_clk_div	4	[3:0]	RW	0x2	Memory clock divider 0000b: divided by 1 0001b: divided by 1.5 0010b: divided by 2 0011b: divided by 3 0100b: divided by 4 0101b: divided by 5 0110b: divided by 6 0111b: divided by 7 1000b: divided by 8 1001b: divided by 9 1010b: divided by 10 1011b: divided by 11 1100b: divided by 12 1101b: divided by 13 1110b: divided by 14 1111b: divided by 15

Pg. = 0x0F	Module = clk_gen					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x02	tm_1ms_cnt[7:0]	8	[7:0]	RW	0xbc	Timer counter in 1 mS resolution current value [7:0]
0x03	tm_1ms_cnt[15:8]	8	[7:0]	RW	0x34	Timer counter in 1 mS resolution current value [15:8]
0x04	pll_pwd	1	[0]	RW	0x0	PLL power down
	pll_bypass	1	[1]	RW	0x0	PLL bypass
	Reserved	5	[6:2]	RW		
	pll_m[8]	1	[7]	RW	0x0	See TS1911 Application Note – PLL Clock Calculation for more information.
0x05	pll_m[7:0]	8	[7:0]	RW	0x26	See TS1911 Application Note – PLL Clock Calculation for more information.
0x06	pll_n	5	[4:0]	RW	0x04	See TS1911 Application Note – PLL Clock Calculation for more information.
	Reserved	3	[7:5]	RW		
0x07 ↕ 0x0C	Reserved					
0c0D	mem_ref_sel	2	[1:0]	RW	0x0	Memory refresh interval 00b: xclk / 256 01b: xclk / 512 10b: xclk /1024 11b: xclk / 2048
	Reserved	6	[7:2]			

9.9. On-Screen Display (OSD) Control Registers (Page 0x11)

9.9.1. On-Screen Display (OSD) Control Register Map

Pg. = 0x11	Module = OSD								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x00									
0x01	bl_sel								0x40
0x02						trans_ind_ctrl	trans_en		0x00
0x03			Win3_boundary_sel		Win2_boundary_sel		Win1_boundary_sel		0xc0
0x04				Win1_shadow_sel[4]	Win1_shadow_sel[3]	Win1_shadow_sel[2]	Win1_shadow_sel[1]	Win1_shadow_sel[0]	0x00
0x05	trans_color1[7:0]								0x80
0x06	trans_color1[15:8]								0x80
0x07	trans_color1[23:16]								0xb5
0x08	trans_color0[7:0]								0x80
0x09	trans_color2[15:8]								0x80
0x0A	trans_color2[23:16]								0xeb
0x0B	bg_color[7:0]								0x80
0x0C	bg_color[15:8]								0x80
0x0D	bg_color[23:16]								0x10
0x0E	alphaB1				alphaB0				0xff
0x0F									
0x10			win1_hl_en	win1_bl_en	win1_intl_mode	win1_gap_disp	win1_en_disp	win1_en	0x04
0x11							win1_h_size		0x01

Pg. = 0x11	Module = OSD								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x12					win1_h_gap				0x00
0x13	win1_h_str[7:0]								0x48
0x14						win1_h_str[10:8]			0x00
0x15				win1_h_fonts					0x18
0x16							win1_v_size		0x00
0x17					win1_v_gap				0x00
0x18	win1_v_str[7:0]								0x0c
0x19						win1_v_str[10:8]			0x00
0x1A					win1_v_fonts				0x0c
0x1B	win1_dram_start_addr[7:0]								0x00
0x1C								win1_dram_start_addr[8]	0x00
0x1D					win1_gap_color				0x00
0x1E									0x00
0x1F	update_win1								0x00
0x20			win2_hl_en	win2_bl_en	win2_intl_mode	win2_gap_disp	win2_en_disp	win2_en	0x04
0x21							win2_h_size		0x01
0x22					win2_h_gap				0x00
0x23	win2_h_str[7:0]								0x00
0x24						win2_h_str[10:8]			0x00
0x25				win2_h_fonts					0x18
0x26							win2_v_size		0x00

Pg. = 0x11	Module = OSD								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x27					win2_v_gap				0x00
0x28	win2_v_str[7:0]								0x00
0x29						win2_v_str[10:8]			0x00
0x2A					win2_v_fonts				0x0c
0x2B	win2_dram_start_addr[7:0]								0xf0
0x2C								win2_dram_start_addr[8]	0x00
0x2D					win2_gap_color				0x00
0x2E	alphaB3				alphaB2				0xff
0x2F	update_win2								0x00
0x30			win3_hl_en	win3_bl_en	win3_intl_mode	win3_gap_disp	win3_en_disp	win3_en	0x04
0x31							win3_h_size		0x01
0x32					win3_h_gap				0x00
0x33	win3_h_str[7:0]								0x00
0x34						win3_h_str[10:8]			0x00
0x35				win3_h_fonts					0x18
0x36							win3_v_size		0x00
0x37					win3_v_gap				0x00
0x38	win3_v_str[7:0]								0x00
0x39						win3_v_str[10:8]			0x00
0x3A					win3_v_fonts				0x0c
0x3B	win3_dram_start_addr[7:0]								0x68

Pg. = 0x11	Module = OSD								
Address	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Default**
0x3C								win3_dram_start_addr[8]	0x01
0x3D					win3_gap_color				0x00
0x3E	alphaB5				alphaB4				0xff
0x3F	update_win3								0x00
0x40				Win2_shadow_sel[4]	Win2_shadow_sel[3]	Win2_shadow_sel[2]	Win2_shadow_sel[1]	Win2_shadow_sel[0]	0x00
0x41				Win3_shadow_sel[4]	Win3_shadow_sel[3]	Win3_shadow_sel[2]	Win3_shadow_sel[1]	Win3_shadow_sel[0]	0x00

9.9.2. On-Screen Display (OSD) Control Register Description

Pg. = 0x11	Module = OSD					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x00	Reserved	8	[7:0]			
0x01	bl_sel	8	[7:0]	RW	0x40	blinking duration select, unit is field
0x02	trans_en	2	[1:0]	RW	0x0	transparent function enable: 0x0 : all OSD data will do alpha blending with image. 0x1 : OSD color matched register 0x05~0x07 will be 100% transparent. The other colors will do alpha blending with image. 0x2 : OSD color matched register 0x08~0x0A will do alpha blending with image. Other colors will show on screen without any alpha blending. 0x3 : OSD color matched register 0x05~0x07 will be 100% transparent. OSD color matched register 0x08~0x0A will do alpha blending with image. All other OSD data will show on screen without any alpha blending.
	trans_ind_ctrl	1	[2]	RW	0x0	0x1: each window FG/BG using individual alpha blending parameters, trans_en[1:0] will be ignored. 0x0: all alpha blending parameters will use reg0e[3:0].
	Reserved	5	[7:3]			
0x03	win1_boundary_sel	2	[1:0]	RW	0x0	[0]: window 1 boundary color in edge of foreground region [1]: window 1 boundary color in edge of background region
	win2_boundary_sel	2	[3:2]	RW	0x0	[0]: window 2 boundary color in edge of foreground region [1]: window 2 boundary color in edge of background region
	win3_boundary_sel	2	[5:4]	RW	0x0	[0]: window 3 boundary color in edge of foreground region [1]: window 3 boundary color in edge of background region
	Reserved	2	[7:6]			
0x04	win1_shadow_sel[0]	1	[0]	RW	0x00	window 1 display shadow on **bottom right** edge of fonts
	win1_shadow_sel[1]	1	[1]	RW	0x0	window 1 display shadow on **bottom left** edge of fonts
	win1_shadow_sel[2]	1	[2]	RW	0x0	window 1 display shadow on **bottom** edge of fonts
	win1_shadow_sel[3]	1	[3]	RW	0x0	window 1 display shadow on **left** edge of fonts
	win1_shadow_sel[4]	1	[4]	RW	0x0	window 1 display shadow on **right** edge of fonts
	Reserved	3	[7:5]			
0x05	trans_color1[7:0]	8	[7:0]	RW	0x80	transparent color1 V data
0x06	trans_color1[15:8]	8	[7:0]	RW	0x80	transparent color1 U data
0x07	trans_color1[23:16]	8	[7:0]	RW	0xb5	transparent color1 Y data
0x08	trans_color2[7:0]	8	[7:0]	RW	0x80	transparent color2 V data
0x09	trans_color2[15:8]	8	[7:0]	RW	0x80	transparent color2 U data
0x0A	trans_color2[23:16]	8	[7:0]	RW	0xeb	transparent color2 Y data
0x0B	bd_color [7:0]	8	[7:0]	RW	0x80	boundary and shadow color V
0x0C	bd_color [15:8]	8	[7:0]	RW	0x80	boundary and shadow color U

Pg. = 0x11	Module = OSD					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x0D	bd_color[23:16]	8	[7:0]	RW	0x10	boundary and shadow color Y
0x0E	alphaB0	4	[3:0]	RW	0xf	alpha blending ratio, used as window 1 BG when reg02[2] is 1
	alphaB1	4	[7:4]	RW	0xf	alpha blending ratio for window 1 FG when reg02[2] is 1
0x0F	Reserved	8	[7:0]			
0x10	win1_en	1	[0]	RW	0x0	window 1 enable
	win1_en_disp	1	[1]	RW	0x0	window 1 display enable **Note: Window 1 overlays window 2, window 2 overlays window 3.**
	win1_gap_disp	1	[2]	RW	0x1	window 1 gap display enable
	Reserved	1	[3]			
	win1_bl_en	1	[4]	RW	0x0	window 1 blinking enable
	win1_hl_en	1	[5]	RW	0x0	window 1 highlight enable
	Reserved	2	[7:6]			
0x11	win1_h_size	2	[1:0]	RW	0x1	window 1 font horizontal size 00: x1 01: x2 10: x3 11: x4
	Reserved	6	[7:2]			
0x12	win1_h_gap	4	[3:0]	RW	0x0	window 1 horizontal gap width
	Reserved	4	[7:4]			
0x13	win1_h_str[7:0]	8	[7:0]	RW	0x48	window 1 horizontal start location[7:0]
0x14	win1_h_str[10:8]	3	[2:0]	RW	0x0	window 1 horizontal start location[10:8]
	Reserved	5	[7:3]			
0x15	win1_h_fonts	5	[4:0]	RW	0x18	window 1 fonts # in horizontal(number of chars in a line) **Note: Max fonts per line is 31.**
	Reserved	3	[7:5]			
0x16	win1_v_size	2	[1:0]	RW	0x0	window 1 font vertical size 00: x1 01: x2 10: x3 11: x4 **Note: In interlace mode, vertical x2, x3, x4 are not supported.**
	Reserved	6	[7:2]			
0x17	win1_v_gap	4	[3:0]	RW	0x0	window 1 vertical gap width
	Reserved	4	[7:4]			

Pg. = 0x11	Module = OSD					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x18	win1_v_str[7:0]	8	[7:0]	RW	0x0c	window 1 font vertical start location[7:0] **Note: Vertical position must be a non-zero value in progressive mode.**
0x19	win1_v_str[10:8]	3	[2:0]	RW	0x0	window 1 font vertical start location[10:8]
	Reserved	5	[7:3]			
0x1A	win1_v_fonts	4	[3:0]	RW	0xc	window 1 fonts # in vertical (number of rows) **Note: Max lines per frame is 15.**
	Reserved	4	[7:4]			
0x1B	win1_dram_start_addr[7:0]	8	[7:0]	RW	0x00	window 1 display ram starting address[7:0]
0x1C	win1_dram_start_addr[8]	1	[0]	RW	0x0	window 1 display ram starting address[8]
	Reserved	7	[7:1]			
0x1D	win1_gap_color	4	[3:0]	RW	0x0	window 1 gap color, shared with BGRAM
	Reserved	4	[7:4]			
0x1E	Reserved	8	[7:0]			
0x1F	Reserved	7	[6:0]			
	upate_win1	1	[7]	RW	0x0	window 1 shadow register update
0x20	win2_en	1	[0]	RW	0x0	window 2 enable
	win2_en_disp	1	[1]	RW	0x0	window 2 display enable **Note: Window 1 overlays window 2, window 2 overlays window 3.**
	win2_gap_disp	1	[2]	RW	0x1	window 2 gap display enable
	Reserved	1	[3]			
	win2_bl_en	1	[4]	RW	0x0	window 2 blinking enable
	win2_hl_en	1	[5]	RW	0x0	window 2 highlight enable
	Reserved	3	[7:6]			
0x21	win2_h_size	2	[1:0]	RW	0x1	window 2 font horizontal size 00: x1 01: x2 10: x3 11: x4
	Reserved	6	[7:2]			
0x22	win2_h_gap	4	[3:0]	RW	0x0	window 2 horizontal gap width
	Reserved	4	[7:4]			
0x23	win2_h_str[7:0]	8	[7:0]	RW	0x00	window 2 horizontal start location[7:0]
0x24	win2_h_str[10:8]	3	[2:0]	RW	0x0	window 2 horizontal start location[10:8]
	Reserved	5	[7:3]			

Pg. = 0x11	Module = OSD					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x25	win2_h_fonts	5	[4:0]	RW	0x18	window 2 fonts # in horizontal(number of chars in a line) **Note: Max fonts per line is 31.**
	Reserved	3	[7:5]			
0x26	win2_v_size	2	[1:0]	RW	0x0	window 2 font vertical size 00: x1 01: x2 10: x3 11: x4 **Note: In interlace mode, vertical x2, x3, x4 are not supported.**
	Reserved	6	[7:2]			
0x27	win2_v_gap	4	[3:0]	RW	0x0	window 2 vertical gap width
	Reserved	4	[7:4]			
0x28	win2_v_str[7:0]	8	[7:0]	RW	0x00	window 2 font vertical start location[7:0] **Note: Vertical position must be a non-zero value in progressive mode.**
0x29	win2_v_str[10:8]	3	[2:0]	RW	0x0	window 2 font vertical start location[10:8]
	Reserved	5	[7:3]			
0x2A	win2_v_fonts	4	[3:0]	RW	0xc	window 2 fonts # in vertical (number of rows) **Note: Max lines per frame is 15.**
	Reserved	4	[7:4]			
0x2B	win2_dram_start_addr[7:0]	8	[7:0]	RW	0xf0	window 2 display ram starting address[7:0]
0x2C	win2_dram_start_addr[8]	1	[0]	RW	0x0	window 2 display ram starting address[8]
	Reserved	7	[7:1]			
0x2D	win2_gap_color	4	[3:0]	RW	0x0	window 2 gap color, shared with BGRAM
	Reserved	4	[7:4]			
0x2E	alphaB2	4	[3:0]	RW	0xf	alpha blending ratio, used as window 2 BG when reg02[2] is 1
	alphaB3	4	[7:4]	RW	0xf	alpha blending ratio for window 2 FG when reg02[2] is 1
0x2F	Reserved	7	[6:0]			
	upate_win2	1	[7]	RW	0x0	window 2 shadow register update

Pg. = 0x11	Module = OSD					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x30	win3_en	1	[0]	RW	0x0	window 3 enable
	win3_en_disp	1	[1]	RW	0x0	window 3 display enable **Note: Window 1 overlays window 2, window 2 overlays window 3.**
	win3_gap_disp	1	[2]	RW	0x1	window 3 gap display enable
	Reserved	1	[3]			
	win3_bl_en	1	[4]	RW	0x0	window 3 blinking enable
	win3_hl_en	1	[5]	RW	0x0	window 3 highlight enable
	Reserved	3	[7:6]			
0x31	win3_h_size	2	[1:0]	RW	0x1	window 3 font horizontal size 00: x1 01: x2 10: x3 11: x4
	Reserved	6	[7:2]			
0x32	win3_h_gap	4	[3:0]	RW	0x0	window 3 horizontal gap width
	Reserved	4	[7:4]			
0x33	win3_h_str[7:0]	8	[7:0]	RW	0x00	window 3 horizontal start location[7:0]
0x34	win3_h_str[10:8]	3	[2:0]	RW	0x0	window 3 horizontal start location[10:8]
	Reserved	5	[7:3]			
0x35	win3_h_fonts	5	[4:0]	RW	0x18	window 3 fonts # in horizontal(number of chars in a line) **Note: Max fonts per line is 31.**
	Reserved	3	[7:5]			
0x36	win3_v_size	2	[1:0]	RW	0x0	window 3 font vertical size 00: x1 01: x2 10: x3 11: x4 **Note: In interlace mode, vertical x2, x3, x4 are not supported.**
	Reserved	6	[7:2]			
0x37	win3_v_gap	4	[3:0]	RW	0x0	window 3 vertical gap width
	Reserved	4	[7:4]			
0x38	win3_v_str[7:0]	8	[7:0]	RW	0x00	window 3 font vertical start location[7:0] **Note: Vertical position must be a non-zero value in progressive mode.**
0x39	win3_v_str[10:8]	3	[2:0]	RW	0x0	window 3 font vertical start location[10:8]
	Reserved	5	[7:3]			

Pg. = 0x11	Module = OSD					
Register Address	**Register Name**	**Width**	**Bit**	**Access**	**Default Value**	**Description**
0x3A	win3_v_fonts	4	[3:0]	RW	0xc	window 3 fonts # in vertical (number of rows) **Note: Max lines per frame is 15.**
	Reserved	4	[7:4]			
0x3B	win3_dram_start_addr[7:0]	8	[7:0]	RW	0x68	window 3 display ram starting address[7:0]
0x3C	win3_dram_start_addr[8]	1	[0]	RW	0x1	window 3 display ram starting address[8]
	Reserved	7	[7:1]			
0x3D	win3_gap_color	4	[3:0]	RW	0x0	window 3 gap color, shared with BGRAM
	Reserved	4	[7:4]			
0x3E	alphaB4	4	[3:0]	RW	0xf	alpha blending ratio, used as window 3 BG when reg02[2] is 1
	alphaB5	4	[7:4]	RW	0xf	alpha blending ratio for window 3 FG when reg02[2] is 1
0x3F	Reserved	7	[6:0]			
	upate_win3	1	[7]	RW	0x0	window 3 shadow register update
0x40	win2_shadow_sel[0]	1	[0]	RW	0x0	window 2 display shadow on **bottom right** edge of fonts
	win2_shadow_sel[1]	1	[1]	RW	0x0	window 2 display shadow on **bottom left** edge of fonts
	win2_shadow_sel[2]	1	[2]	RW	0x0	window 2 display shadow on **bottom** edge of fonts
	win2_shadow_sel[3]	1	[3]	RW	0x0	window 2 display shadow on **left** edge of fonts
	win2_shadow_sel[4]	1	[4]	RW	0x0	window 2 display shadow on **right** edge of fonts
	Reserved	3	[7:5]			
0x41	win3_shadow_sel[0]	1	[0]	RW	0x0	window 3 display shadow on **bottom right** edge of fonts
	win3_shadow_sel[1]	1	[1]	RW	0x0	window 3 display shadow on **bottom left** edge of fonts
	win3_shadow_sel[2]	1	[2]	RW	0x0	window 3 display shadow on **bottom** edge of fonts
	win3_shadow_sel[3]	1	[3]	RW	0x0	window 3 display shadow on **left** edge of fonts
	win3_shadow_sel[4]	1	[4]	RW	0x0	window 3 display shadow on **right** edge of fonts
	Reserved	3	[7:5]			

9.9.3. Display RAM Format

Bit	[19]	[18:10]	[9]	[8]	[7:4]	[3:0]
Function	fnt_en	fnt_index	hl_en	bl_en	fgcolor	bgcolor
Description	Font display. 0: disable 1: enable	index to font RAM. The unit is the font number. 0~127: using fonts in ROM 128~255: using icon display 256~511: using internal SRAM fonts	High lighting. 0: disable 1: enable	Blinking. 0: disable 1: enable	index of FGRAM	index to BGRAM

9.9.4. Font ROM Format

12x18 font (total 128 fonts, from 0 to 127)

Font Index	Offset	Bit		
		[23:16]	[15:8]	[7: 0]
Font 0	0	F0L1[11:4]	F0L1[3:0],F0L0[11:8]	F0L0[7:0]
	1	F0L3[11:4]	F0L3[3:0],F0L2[11:8]	F0L2[7:0]
	2	F0L5[11:4]	F0L5[3:0],F0L4[11:8]	F0L4[7:0]
	…			
	8	F0L17[11:4]	F0L17[3:0]F0L16[11:8]	F0L16[7:0]
Font 1	9	F1L1[11:4]	F1L1[3:0]F1L0[11:8]	F1L0[7:0]
↕	…			
Font 127	1151	F127L17[11:4]	F127L17[3:0],F127L16[11:8]	F127L16[7:0]

9.9.5. Font RAM Format

12x18 font (total 256 fonts, from 256 to 511)

Font Index	Offset	Bit		
		[23:16]	[15:8]	[7: 0]
Font 256	0	F256L1[11:4]	F256L1[3:0]F256L0[11:8]	F256L0[7:0]
	1	F256L3[11:4]	F256L3[3:0]F256L2[11:8]	F256L2[7:0]
	2	F256L5[11:4]	F256L5[3:0]F256L4[11:8]	F256L4[7:0]
	…			
	8	F256L17[11:4]	F256L17[3:0]F256L16[11:8]	F256L16[7:0]
Font 257	9	F257L1[11:4]	F257L1[3:0]F257L0[11:8]	F257L0[7:0]
↕	…			
Font 511	2303	F511L17[11:4]	F511L17[3:0]F511L16[11:8]	F511L16[7:0]

9.9.6. BG RAM Format

BGCOLOR Index	Address Offset	Bit [7:0]
BGCOLOR 0	0	BGCOLOR_0_V[7:0]
	1	BGCOLOR_0_U[7:0]
	2	BGCOLOR_0_Y[7:0]
	3	N/A
BGCOLOR 1	4	BGCOLOR_1_V[7:0]
	5	BGCOLOR_1_U[7:0]
	6	BGCOLOR_1_Y[7:0]
	7	N/A
BG COLOR 2 ↕ BGCOLOR 14	…	….
BGCOLOR 15	60	BGCOLOR_15_V[7:0]
	61	BGCOLOR_15_U[7:0]
	62	BGCOLOR_15_Y[7:0]
	63	N/A

9.9.7. FG RAM Format

FGCOLOR Index	Address Offset	Bit [7:0]
FGCOLOR 0	0	FGCOLOR_0_V[7:0]
	1	FGCOLOR_0_U[7:0]
	2	FGCOLOR_0_Y[7:0]
	3	N/A
FGCOLOR 1	4	FGCOLOR_1_V[7:0]
	5	FGCOLOR_1_U[7:0]
	6	FGCOLOR_1_Y[7:0]
	7	N/A
FG COLOR 2 ↕ FGCOLOR 14	…	….
FGCOLOR 15	60	FGCOLOR_15_V[7:0]
	61	FGCOLOR_15_U[7:0]
	62	FGCOLOR_15_Y[7:0]
	63	N/A

9.9.8. ICON RAM Format

ICONCOLOR Index	Address Offset	Bit [7:0]
ICONCOLOR 0	0	IconCOLOR_0_V[7:0]
	1	IconCOLOR_0_U[7:0]
	2	IconCOLOR_0_Y[7:0]
	3	N/A
ICONCOLOR 1	4	IconCOLOR_1_V[7:0]
	5	IconCOLOR_1_U[7:0]
	6	IconCOLOR_1_Y[7:0]
	7	N/A
ICONCOLOR 2 ↕ ICONCOLOR 14	…	….
ICONCOLOR 15	60	IconCOLOR_15_V[7:0]
	61	IconCOLOR_15_U[7:0]
	62	IconCOLOR_15_Y[7:0]
	63	N/A

9.9.9. Border and Shadow Registers

Substitute the **?** mark with 1, 2 or 3 for the OSD windows they belong to.

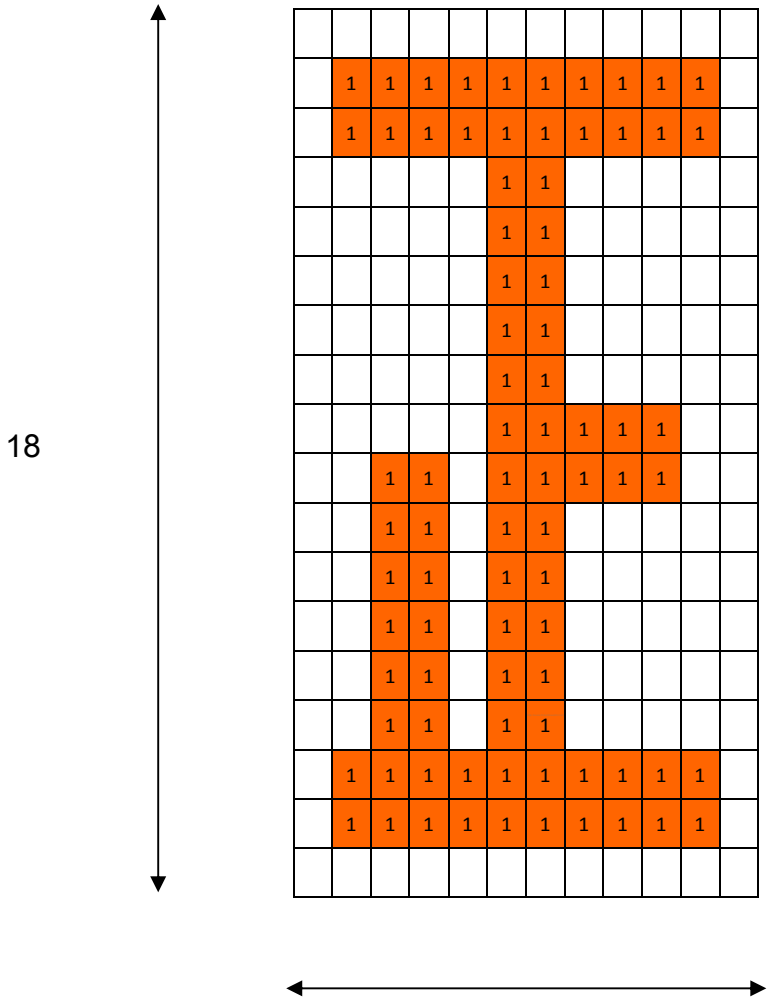
win?_boundary_sel[0] : boundary color in edge of **foreground** region.
win?_boundary_sel[1] : boundary color in edge of **background** region.

win?_shadow_sel[0] : boundary color in **lower right** edge of foreground region.
win?_shadow_sel[1] : boundary color in **lower left** edge of foreground region.
win?_shadow_sel[2] : boundary color in **lower edge** of foreground region.
win?_shadow_sel[3] : boundary color in **left edge** of foreground region.
win?_shadow_sel[4] : boundary color in **right edge** of foreground region.

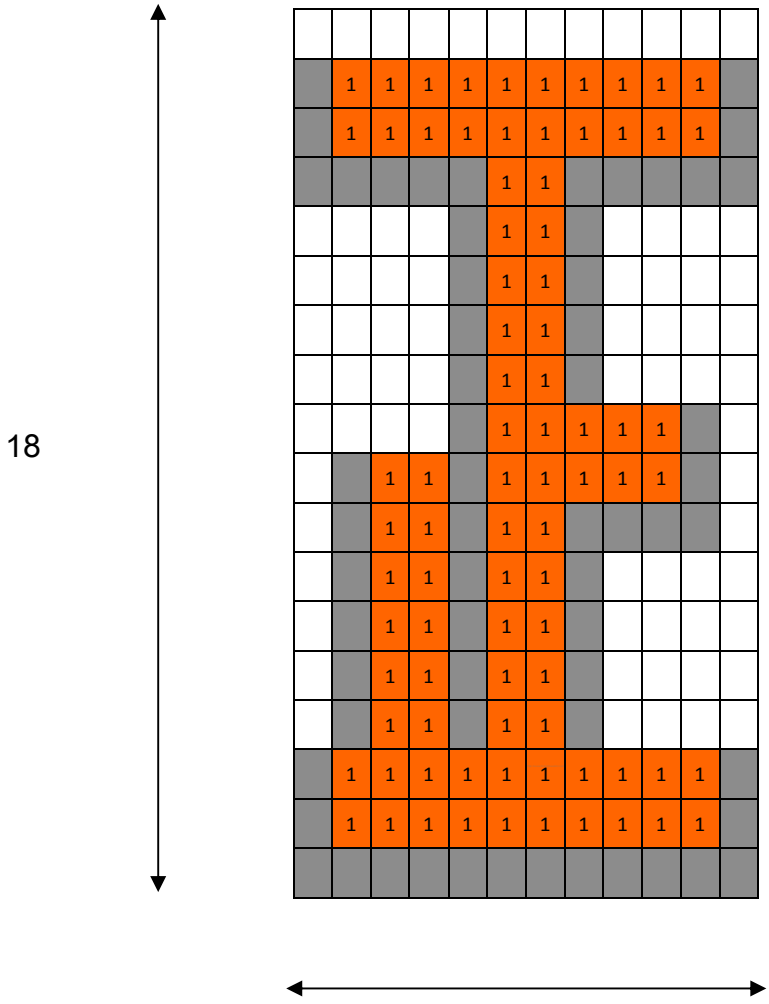
left edge win?_shadow_sel [3]	font foreground	**right edge** win?_shadow_sel [4]
lower left win?_shadow_sel [1]	**lower edge** win?_shadow_sel [2]	**lower right** win?_shadow_sel[0]

The following examples demonstrate boundary and shadow combinations:

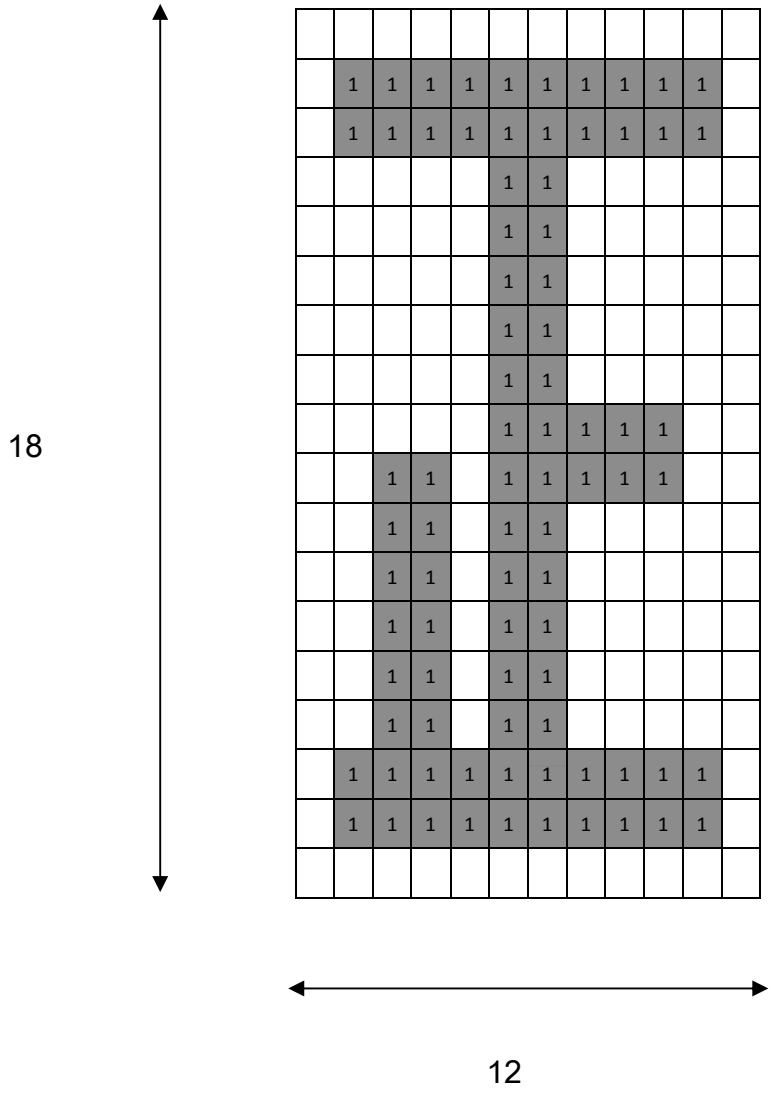
Example 1: Original font. win?_boundary_sel[1:0] = 00b.



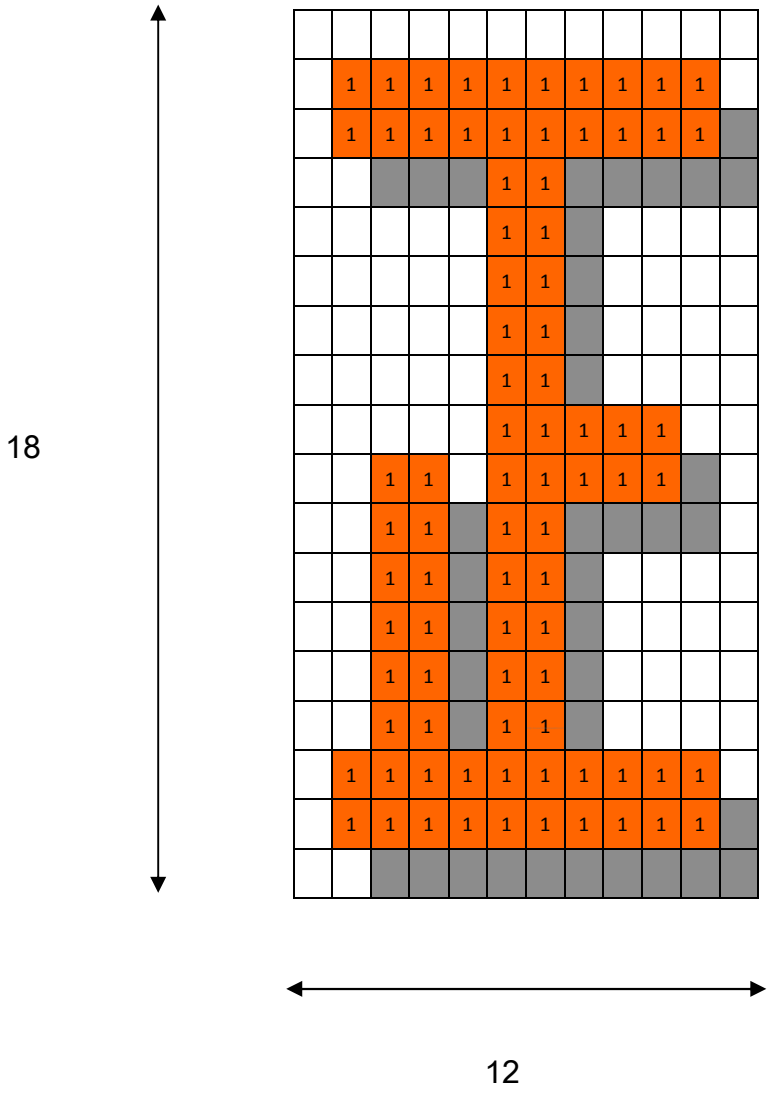
Example 2: Set boundary in edge of **background**; win?_ boundary_sel[1:0]=10b.



Example 3: Set boundary in edge of **foreground**; win?_ boundary_sel[1:0]=01b.



Example 4: Set shadow in **lower right** edge; bdr_sel[2:0] = 100b, sdw_sel[2:0]=101b.



Design Engineer's Seal

Content	Signature

Content	Signature

Final Approval: _____ Date: _____