

SOT-25



Pin Definition:

- 1. SW
- 2. Ground
- 3. FB
- 4. EN
- 5. Input

General Description

The TS1935 switching regulator is current –mode boost converters operating at fixed frequency of 1.6MHz. The use of SOT-25 made possible by the minimal power loss of the internal 1.6A switch, and use of small inductor and capacitors result in the industry’s highest power density. The 30V internal switch makes these solutions perfect for boosting to voltages up to 30V. These parts have a logic-level shutdown pin that can be used to reduce quiescent current and extend battery life. Protection is provided through cycle-by-cycle current limiting and thermal shutdown. Internal compensation simplifies and reduces component count.

Features

- 30V DMOS FET Switch
- 2.7V to 5.5V Input Range
- 1.6MHz Switching Frequency
- Low $R_{DS(ON)}$ DMOS FET
- Switch Current up to 1.6A
- Low Shutdown Current <1uA
- Use Tiny Capacitors and Inductor
- Cycle-by-Cycle Current Limiting

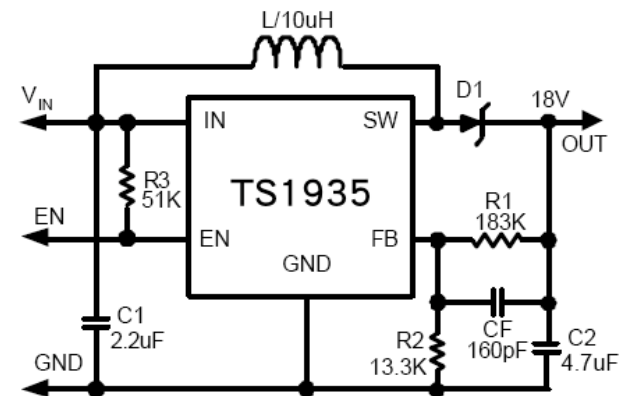
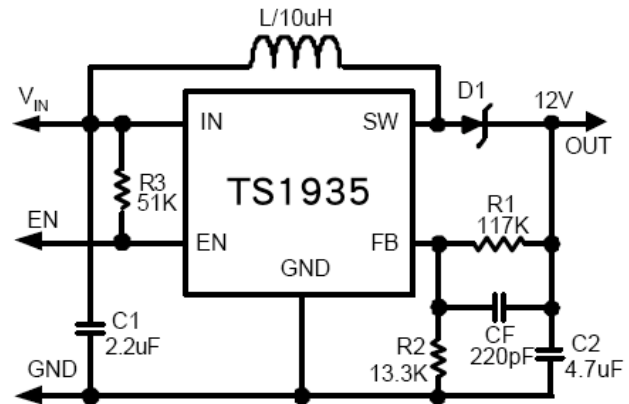
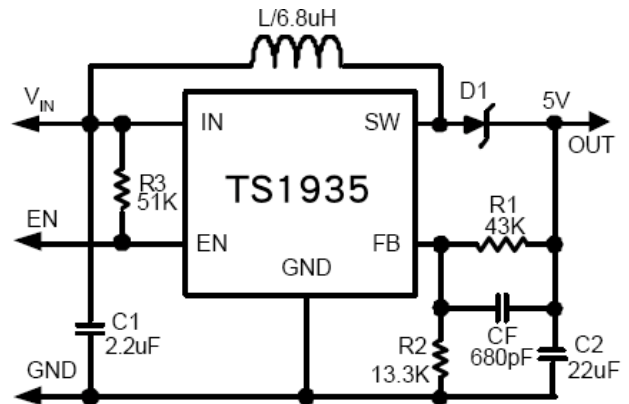
Application

- White LED Current Source
- Digital Still Cameras
- Portable Electronics
- PDA’s and Palm-Top Computers
- Local Boost Regulator

Ordering Information

Part No.	Package	Packing
TS1935CX5 RF	SOT-25	3Kpcs / 7” Reel

Typical Application Circuit



Absolute Maximum Rating

Parameter	Symbol	Limit	Unit
Input Voltage	V_{IN}	6	V
EN, V_{FB} Voltage	V_{EN}, V_{FB}	V_{IN}	V
SW Voltage	V_{SW}	30	V
Ambient Temperature Range	T_A	-40 to +85	°C
Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
ESD Classification		B*	

Note: Stress above the listed absolute maximum rating may cause permanent damage to the device

* HBM B: 2000~3999V

Thermal Information

Parameter	Symbol	Maximum	Unit
Thermal Resistance* (Junction to Case)	Θ_{JC}	81	°C/W
Thermal Resistance* (Junction to Ambient)	Θ_{JA}	260	°C/W
Internal Power Dissipation	P_D	400	mW
Maximum Junction Temperature		150	°C
Solder Iron (10 Sec)**		350	°C

* Measure Θ_{JC} on center of molding compound if IC has no tab.

** MIL-STD-202G210F

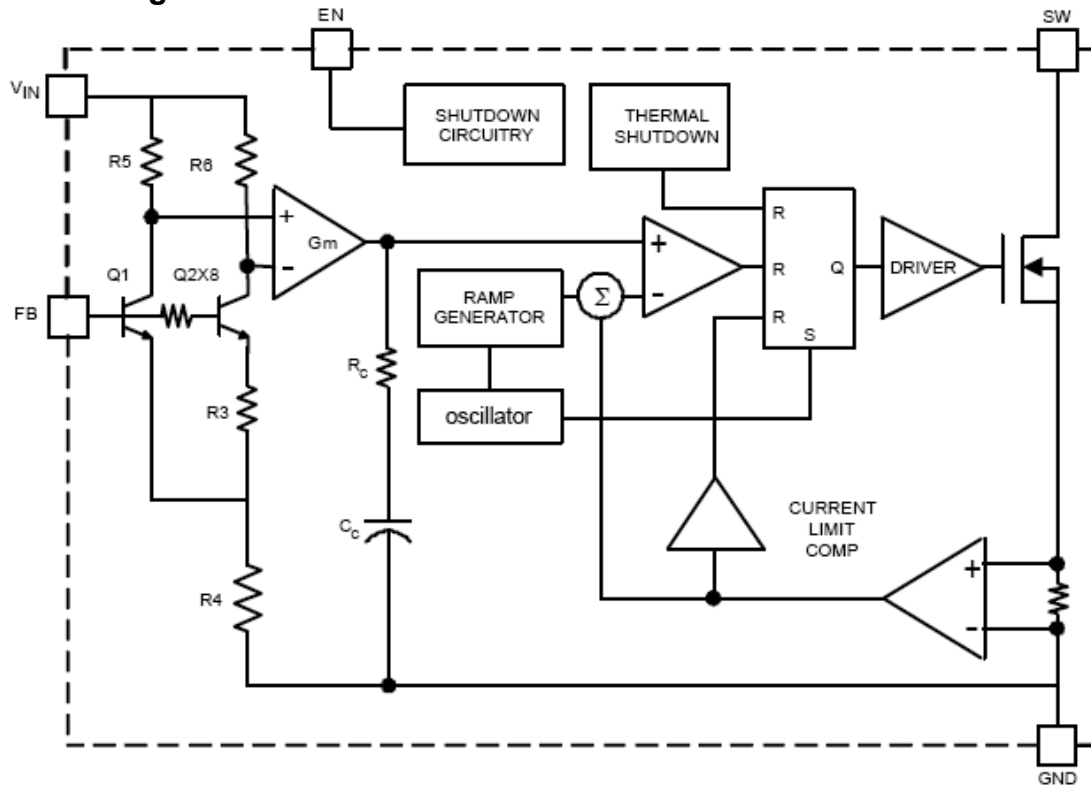
Pin Description

Pin Number	Pin Name	Description
1	SW	Power Switch Input. This is the drain of the internal NMOS power switch. Minimize the metal trace area connected to this pin to minimize EMI.
2	GND	Ground. Tie directly to ground plane.
3	FB	Output voltage feedback input. Set the output voltage by selecting values for R1 and R2 using: $R1 = R2 \left(\frac{V_{out}}{1.23V} - 1 \right)$ Connect the ground of the feedback network to a GND plane.
4	EN	Enable, active high. The enable pin is an active high control. Tie this pin above 2V to enable the device. Tie this pin below 0.4V to turn off the device.
5	IN	Analog and Power input. Input Supply Pin. Place bypass capacitor as close to V_{in} as possible.

**1.6MHz Boost Converter
with 30V Internal FET Switch**
Electrical Specifications ($T_a = 25^\circ\text{C}$, $V_{IN}=5\text{V}$, $EN=V_{IN}$, $I_L=0\text{A}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Input Voltage	V_{IN}		2.5	--	5.5	V	
Feedback Pin Bias Current	I_{FB}	$V_{FB} = 1.23\text{V}$	--	60	500	nA	
Regulated Feedback Voltage	V_{FB}	$V_{IN} = 3\text{V}$	1.205	1.23	1.255	V	
FB Voltage Line Regulation	$\Delta V_{FB} / \Delta V_{IN}$	$2.7\text{V} \leq V_{IN} \leq 5.5\text{V}$	--	0.02	--	%/V	
Minimum Output Voltage Under Load	$V_{OUT(MIN)}$	$R_L = 43\Omega$	$V_{IN} = 2.7\text{V}$	5.4	7	--	V
			$V_{IN} = 3.3\text{V}$	8	10	--	
			$V_{IN} = 5\text{V}$	13	17	--	
		$R_L = 43\Omega$	$V_{IN} = 2.7\text{V}$	3.75	5	--	
			$V_{IN} = 3.3\text{V}$	5	6.5	--	
			$V_{IN} = 5\text{V}$	8.75	11	--	
Switch Current Limit	I_{CL}	$T_a = 25^\circ\text{C}$	1.5	1.8	--	A	
		$T_a = -40 \sim +85^\circ\text{C}$	1.2	--	--		
Switch ON Resistance	R_{DSON}	$V_{IN} = 5\text{V}$, $T_a = -40 \sim +85^\circ\text{C}$	--	0.4	0.6	A	
		$V_{IN} = 3.3\text{V}$, $T_a = -40 \sim +85^\circ\text{C}$	--	--	0.7		
		$V_{IN} = 3.3\text{V}$, $T_a = -40 \sim +85^\circ\text{C}$	--	0.5	0.7		
Shutdown Current	I_{SD}	$V_{EN} = 0\text{V}$	--	0.1	1	μA	
Quiescent Current	I_Q	FB = 1.15V (Switching)	$T_a = 25^\circ\text{C}$	--	2	--	mA
			$V_{IN} = 5\text{V}$, $T_a = -40 \sim +85^\circ\text{C}$	--	--	3	
		FB = 1.3V (No Switching)	$T_a = 25^\circ\text{C}$	--	400	--	μA
			$V_{IN} = 5\text{V}$, $T_a = -40 \sim +85^\circ\text{C}$	--	--	500	
EN Pin Bias Current	I_{EN}	EN = 0	--	0	--	μA	
		EN = 5V	--	0	2		
Switching Frequency	f_{SW}	$T_a = -40 \sim +85^\circ\text{C}$	1	1.6	1.85	MHz	
Switching Leakage Current	I_{SW}	$V_{EN} = 0\text{V}$	--	0.1	2	μA	
Maximum Duty Cycle	D_{MAX}	$T_a = -40 \sim +85^\circ\text{C}$	86	93	--	%	
EN Input Threshold (High) (Shutdown)	V_{EH}	$T_a = -40 \sim +85^\circ\text{C}$	--	--	1.4	V	
EN Input Threshold (Low) (Enable the device)	V_{EL}	$T_a = -40 \sim +85^\circ\text{C}$	2	--	--		

Function Block Diagram



Pin Description

The TS1935 is a switching converter IC that operates at a fixed frequency (1.6MHz) for fast transient response over a wide input voltage range and incorporates pulse-by-pulse current limiting protection. Because this is current mode control, a 33mΩ sense resistor in series with the switch FET is used to provide a voltage (which is proportional to the FET current) to both the input of the pulse width modulation (PWM) comparator and the current limit amplifier.

At the beginning of each cycle, the S-R latch turns on the FET. As the current through the FET increases, a voltage (proportional to this current) is summed with the ramp coming from the ramp generator and then fed into the input of the PWM comparator. When this voltage exceeds the voltage on the other input (coming from the Gm amplifier), the latch resets and turns the FET off. Since the signal coming from the Gm amplifier is derived from the feedback (which samples the voltage at the output), the action of the PWM comparator constantly sets the correct peak current through the FET to keep the output voltage in regulation.

Q1 & Q2 along with R3 – R6 form a bandgap voltage reference used by the IC to hold the output in regulation. The currents flowing through Q1 & Q2 will be equal, and the feedback loop will adjust the regulated output to maintain this. Because of this, the regulated output is always maintained at a voltage level equal to the voltage at the FB node “multiplied up” by the ratio of the output resistive divider.

The current limit comparator feeds directly into the flip-flop that drives the switch FET. If the FET current reaches the limit threshold, the FET is turned off and the cycle terminates the pulse regardless of the status of the output of the PWM comparator.

Electrical Characteristics Curve

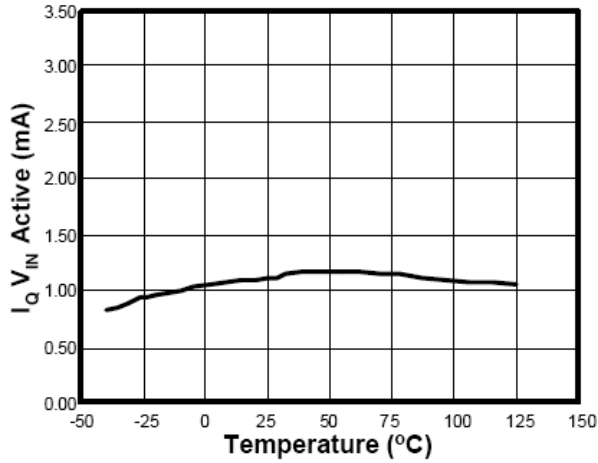


Figure 1. I_Q Vin (Active) vs. Temperature

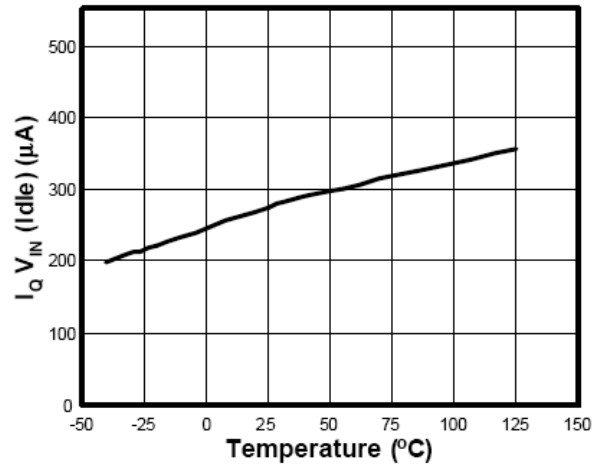


Figure 2. I_Q Vin (Idle) vs. Temperature

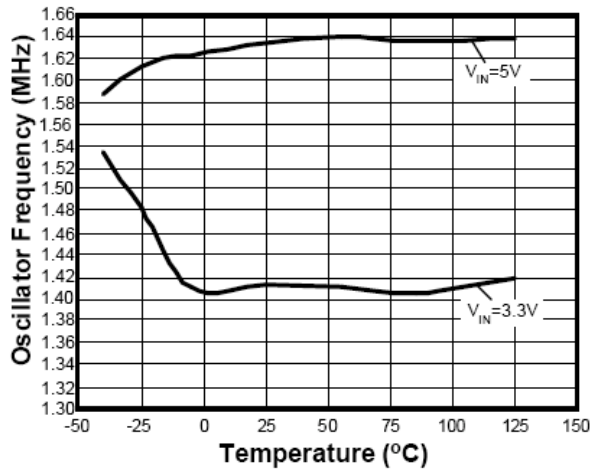


Figure 3. Oscillator Frequency vs. Temperature

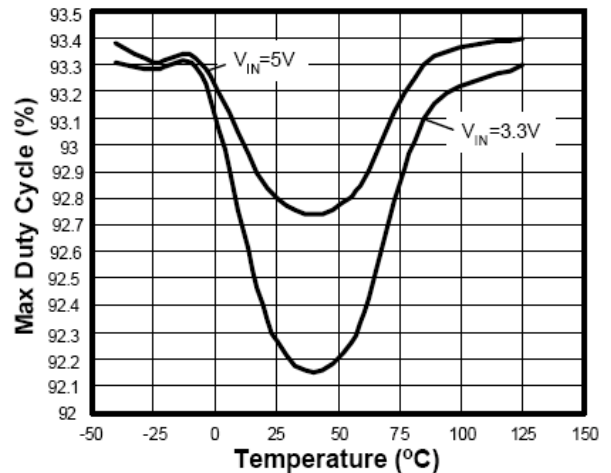


Figure 4. Max. Duty Cycle vs. Temperature

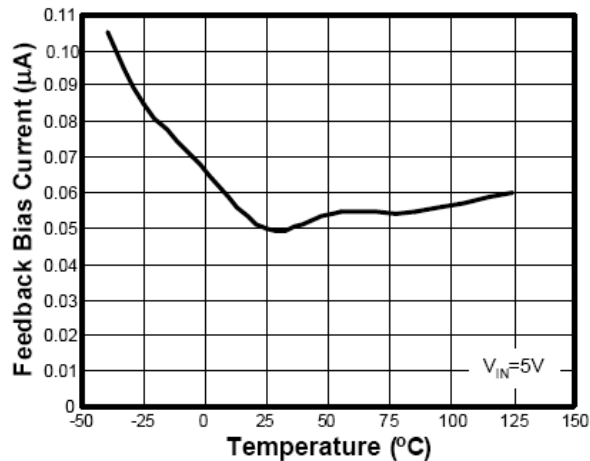


Figure 5. Feedback Bias Current vs. Temperature

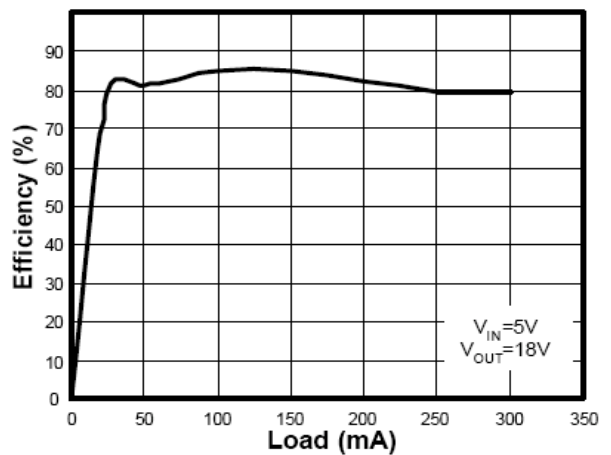


Figure 6. Efficiency vs. Load Current

Electrical Characteristics Curve

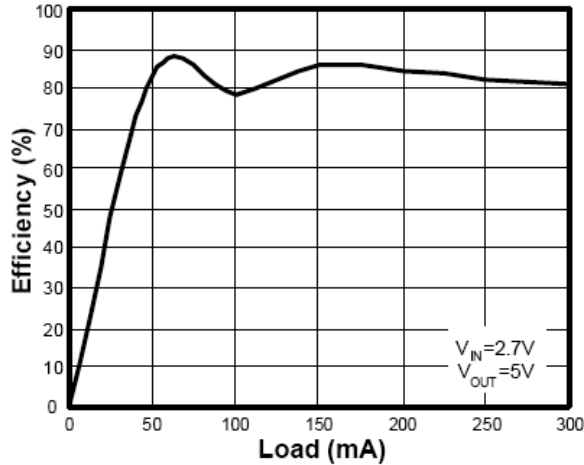


Figure 7. Efficiency vs. Load Current

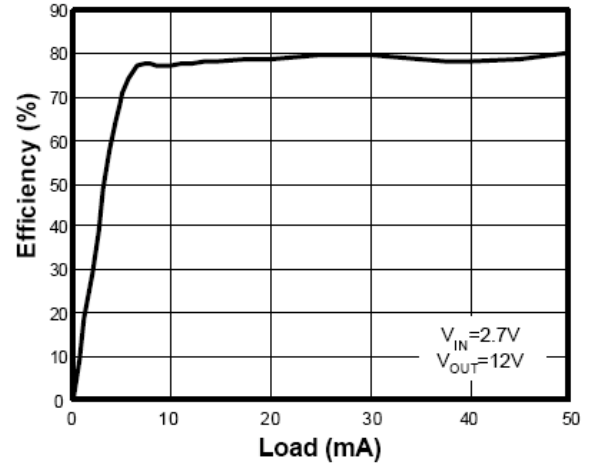


Figure 8. Efficiency vs. Load Current

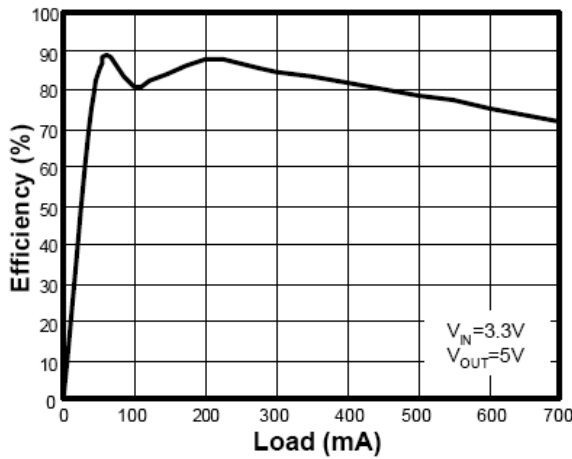


Figure 9. Efficiency vs. Load Current

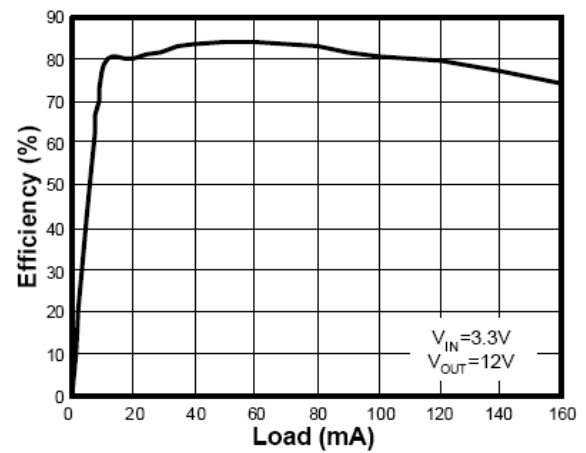


Figure 10. Efficiency vs. Load Current

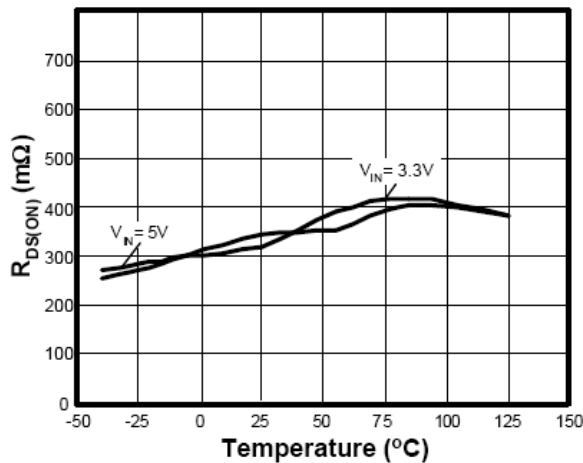


Figure 11. $R_{DS(ON)}$ vs. Temperature

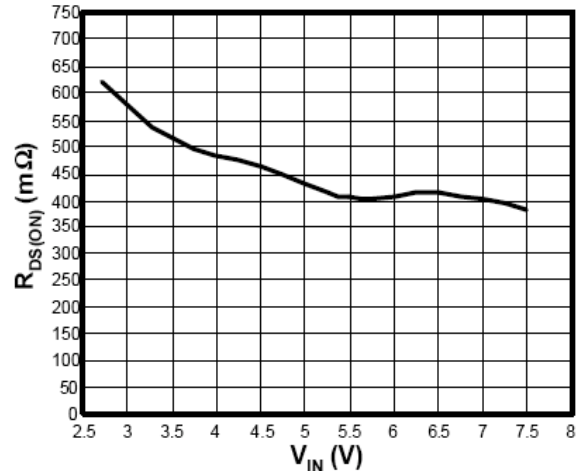
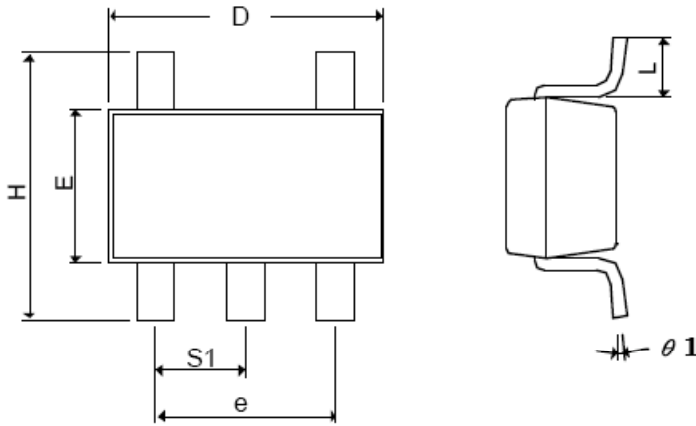
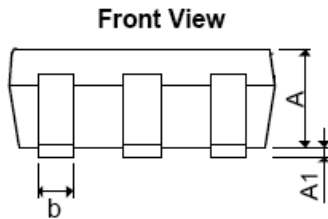


Figure 12. $R_{DS(ON)}$ vs. V_{IN}

SOT-25 Mechanical Drawing



SOT-25 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A+A1	0.09	1.25	0.0354	0.0492
B	0.30	0.50	0.0118	0.0197
C	0.09	0.25	0.0035	0.0098
D	2.70	3.10	0.1063	0.1220
E	1.40	1.80	0.0551	0.0709
E	1.90 BSC		0.0748 BSC	
H	2.40	3.00	0.09449	0.1181
L	0.35 BSC		0.0138 BSC	
Θ1	0°	10°	0°	10°
S1	0.95 BSC		0.0374 BSC	



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