TS25L16APP

16 Mbit Serial Flash memory with 75 MHz Dual and Quad SPI bus Interface

Features

Architectural Advantages

■ Single power supply operation

- Full voltage range: 2.7 to 3.6 V read and program operations

■ Memory Architecture

- 32ea sectors with 512 Kb each

■ Program

- Page Program (up to 256 bytes) in 0.3 ms (typical)
- Page Write (up to 256 bytes) in 2.8 ms (typical)
- Program cycles are on a page by page basis

■ Erase

- 2ms typical Page Erase Time
- 2ms typical SubSector Erase Time
- 32ms typical Sector Erase time
- 1 sec typical Bulk Erase time

■ Cycling Endurance

- 100,000 P/E cycles per sector typical

■ Data Retention

- 20 years typical

■ Device ID

- JEDEC standard two-byte electronic signature

■ Package Option

- Industry Standard Pin-outs
- 8-pin SOP 208 mil
- 8-pin SOP 150 mil
- 8-pin PDIP 300 mil

Performance Characteristics

■ Speed

- 75 MHz clock rate (maximum)

■ Dual/Quad Output Speed

- 150 MHz/300 MHz an equivalent clock rate (maximum)

■ Power Saving Standby Mode

- Standby Mode 1 μA (typical)
- Deep Power-down Mode 1 μA (typical)

Memory Protection Features

■ Memory Protection

- W# (SO2) pin works in conjunction with Status Register Bits to protect specified memory areas
- Status Register Block Protection bits (BP3, BP2, BP1, BP0) in status register configure parts of memory as read-only

Software Features

■ SPI Bus Compatible Serial Interface

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1. Description

The TS25L16AP device is a 3.0 Volt(2.7 V to 3.6 V) single power supply Flash memory device. TS25L16AP consists of thirty-two sectors, each with 512 Kb memory.

Data appears on Serial Data input SI(SO0) pin when inputting data into the memory and on Serial Data output SO(SO1) pin when outputting data from the memory. In case of Fast Read Dual Output mode, the SI(SO0) pin becomes another output Pin and Fast Read Quad Output mode, SI(SO0), W#(SO2) and Hold#(SO3) are used by additional outputs. The devices are designed to be programmed in-system with the standard system 3.0 Volt VCC supply.

The memory can be programmed 1 to 256 bytes at a time, using the Page Program, Page Write instruction.

The memory supports Page Erase, Sub-Sector Erase, Sector Erase and Bulk Erase instructions.

Each device requires only a 3.0 Volt power supply (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program operations.

Figure 1. Logic Diagram

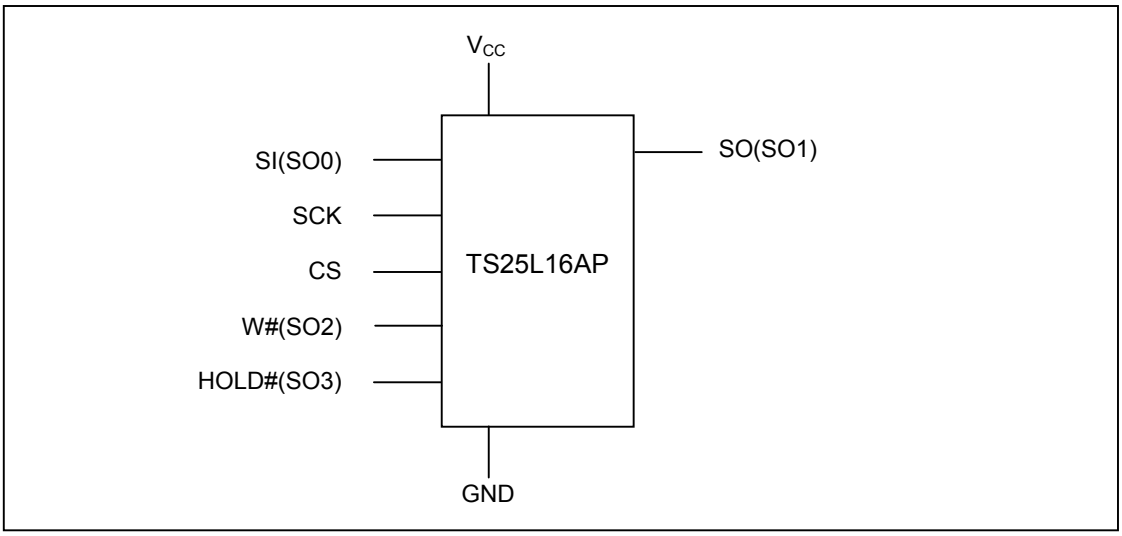
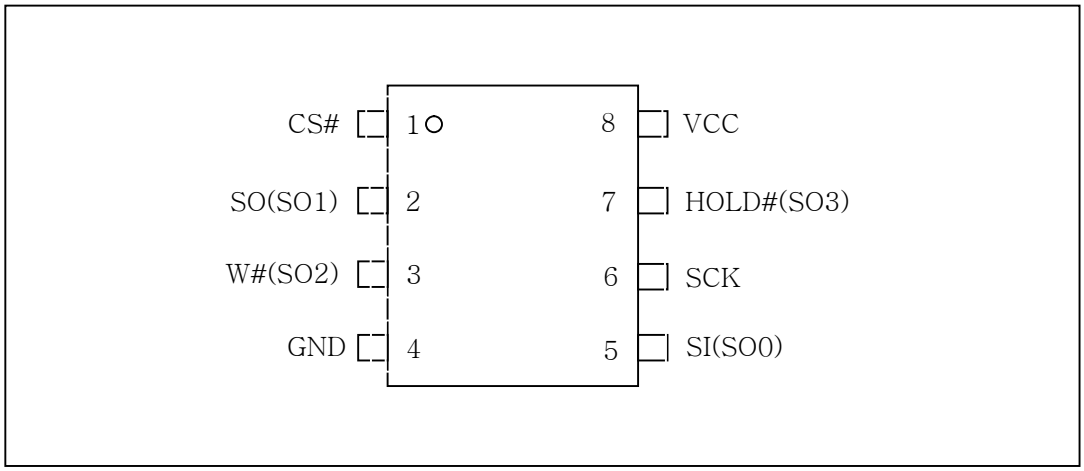


Table 1. Signal names

Signal name	Function	Direction
C = SCK	Serial Clock	Input
D = SI(SO0)	Serial Data input	Input / Output
Q = SO(SO1)	Serial Data output	Output
S = CS#	Chip Select	Input
W = W#(SO2)	Write Protect	Input / Output
HOLD = HOLD#(SO3)	Hold	Input / Output
V_{CC}	Supply voltage	
V_{SS} = GND	Ground	

Figure 2. SOP 8Pin connections



2 Signal descriptions

2.1 Serial Data output (SO) – SO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK) at all read mode. Also, When the device is FRDO(Fast Read Dual Output) or FRQO(Fast Read Quad Output) mode, this pin(SO) is used for SO1

2.2 Serial Data input (SI) – SO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (SCK). Also, When the device is FRDO(Fast Read Dual Output) or FRQO(Fast Read Quad Output) mode, this pin(SI) is used for SO0

2.3 Serial Clock (SCK)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (SI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SO) changes after the falling edge of Serial Clock (SCK).

2.4 Chip Select (CS#)

When this input signal is High, the device is deselected and Serial Data Output (SO) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select (CS#) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select (CS#) is required prior to the start of any instruction.

2.5 Hold (HOLD#) – SO3

The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select (CS#) driven Low. Also, When the QE bit of Status Register is set for "High", the Hold# function is not available and this pin used for SO3 in FRQO(Fast Read Quad Output) mode.

2.6 Write Protect (W#) – SO2

The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP3, BP2, BP1 and BP0 bits of the Status Register).
Like the Hold# pin, When the QE bit of Status Register is set for "High", the W# function is not available too, and this pin used for SO2 in FRQO(Fast Read Quad Output) mode.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

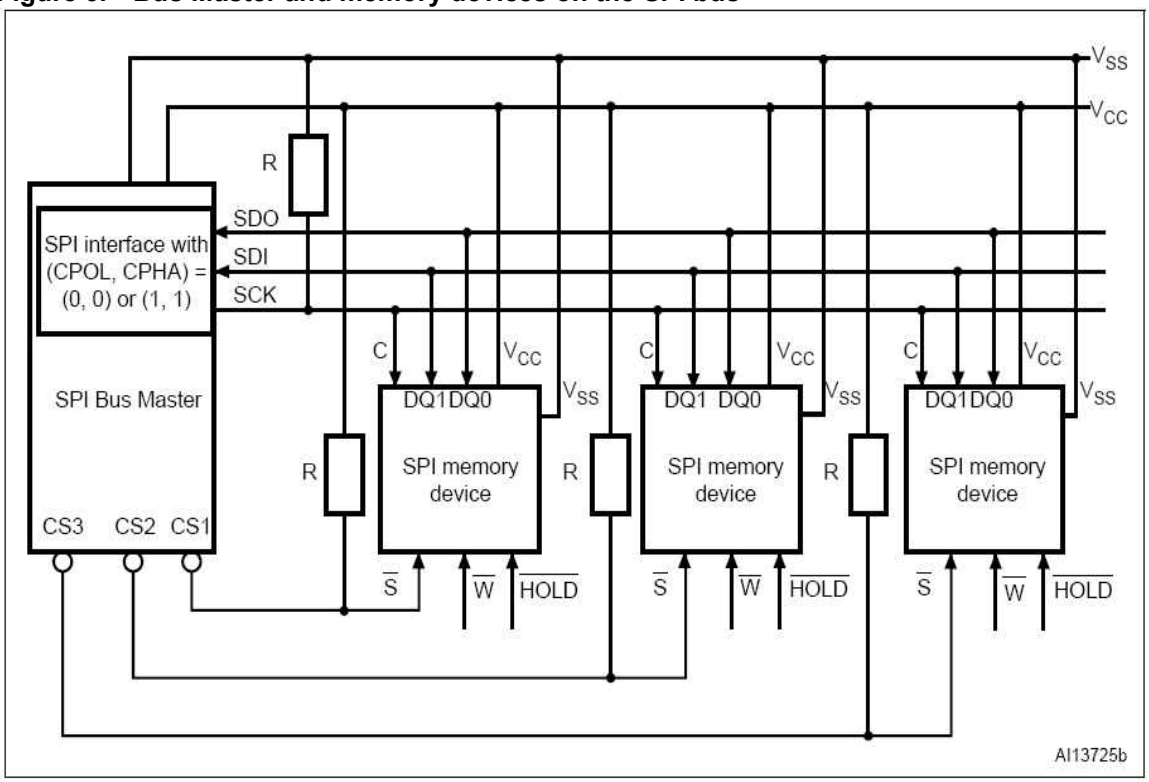
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (SCK), and output data is available from the falling edge of Serial Clock (SCK).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in Standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 3. Bus Master and memory devices on the SPI bus

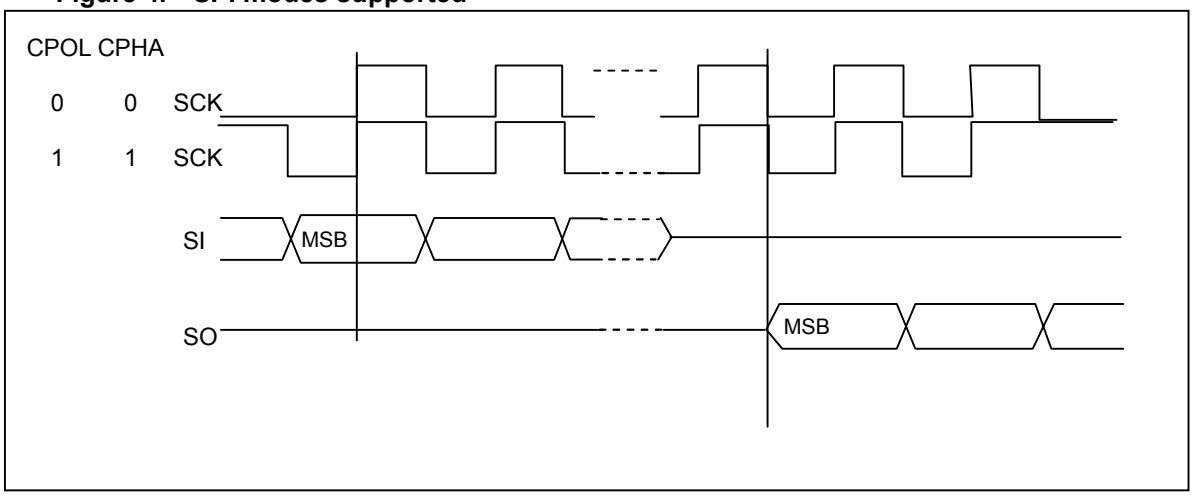


1. The Write Protect (W) and Hold (HOLD) signals should be driven, High or Low as appropriate.

Figure 3 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (SO) line at a time, the other devices are in the high impedance state. Resistors R (represented in *Figure 3*) ensure that the TS25L16AP is not selected if the Bus Master leaves the CS# line in the high impedance state. As the Bus Master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the Bus Master is reset), the clock line (SCK) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the S line is pulled High while the SCK line is pulled Low (thus ensuring that CS# and SCK do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant R*C_p (C_p = parasitic capacitance of the bus line) is shorter than the time during which the Bus Master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is R*C_p = 5 µs <=> the application must ensure that the Bus Master never leaves the SPI bus in the high impedance state for a time period shorter than 5µs.

Figure 4. SPI modes supported



4 Operating features

4.1 Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few bytes (see *Page Program (PP)*, and *Table 15: AC characteristics*.)

4.2 Page Erase, SubSector Erase, Sector Erase and Bulk Erase

The Page Program (PP) allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a page, subsector, and sector at a time, using the Page Erase (PE) , the SubSector Erase (SSE), and the Sector Erase (SE) instruction, or throughout the entire memory, using the Bulk Erase (BE) instruction. This starts an internal Erase cycle (of duration t_{SE} or t_{BE}).

The Erase instruction must be preceded by a Write Enable (WREN) instruction.

4.3 Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP or PW) or Erase (PE, SSE, SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{pw}, t_{PE}, t_{SSE}, t_{SE}, or t_{BE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

4.4 Active Power, Standby Power and Deep Power-down modes

When Chip Select (S) is Low, the device is enabled, and in the Active Power mode.

When Chip Select (S) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes in to the Standby Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down mode and Read Electronic Signature (RES) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

4.5 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. For a detailed description of the Status Register bits, see *Section 6.4: Read Status Register (RDSR)*.

4.6 Protection modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the TS25L16AP boasts the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Page Write (PW) instruction completion
  - Page Erase (PE) instruction completion
  - SebSector Erase (SSE) instruction completion
  - Sector Erase (SE) instruction completion
  - Bulk Erase (BE) instruction completion
- The Block Protect (BP3, BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (W) signal allows the Block Protect (BP3, BP2, BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 2. Protected area sizes

Status Register Bit				Memory Content
BP3	BP2	BP1	BP0	Protected Area
0	0	0	0	0(none)
0	0	0	1	1sector, sector 31^{th}
0	0	1	0	2sectors, sector 30^{th}~31^{th}
0	0	1	1	4sectors, sector 28^{th}~31^{th}
0	1	0	0	8sectors, sector 24^{th}~31^{th}
0	1	0	1	16sectors, sector 16^{th}~31^{th}
0	1	1	0	32sectors, ALL
0	1	1	1	32sectors, ALL
1	0	0	0	32sectors, ALL
1	0	0	1	32sectors, ALL
1	0	1	0	16sectors, sector 0^{th}~15^{th}
1	0	1	1	24sectors, sector 0^{th}~23^{th}
1	1	0	0	28sectors, sector 0^{th}~27^{th}
1	1	0	1	30sectors, sector 0^{th}~29^{th}
1	1	1	0	31sectors, sector 0^{th}~30^{th}
1	1	1	1	32sectors, ALL

4.7 Hold condition

The Hold (HOLD#) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (CS#) Low.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCK) being Low (as shown in *Figure 5*).

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCK) being Low.

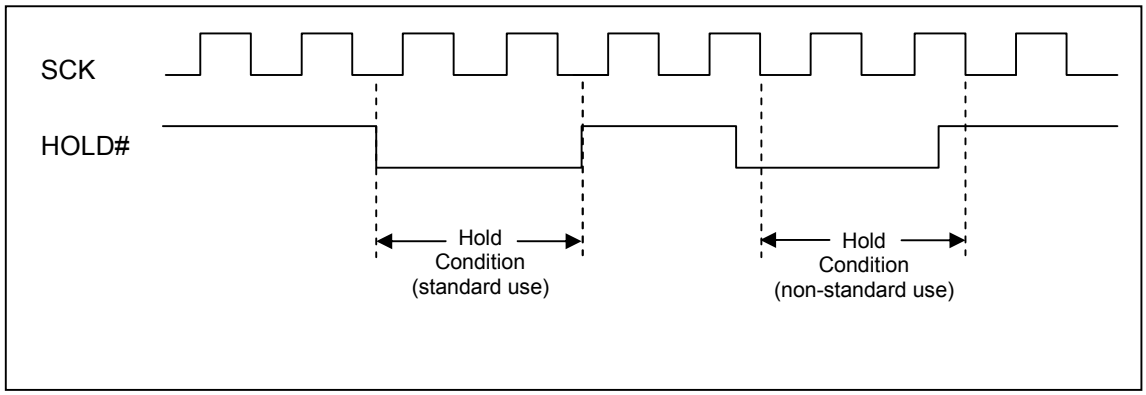
If the falling edge does not coincide with Serial Clock (SCK) being Low, the Hold condition starts after Serial Clock (SCK) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (SCK) being Low, the Hold condition ends after Serial Clock (SCK) next goes Low. (This is shown in *Figure 5*).

During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care.

Normally, the device is kept selected, with Chip Select (CS#) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (CS#) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD#) High, and then to drive Chip Select (CS#) Low. This prevents the device from going back to the Hold condition.

Figure 5. Hold condition activation



5 Memory organization

The memory is organized as:

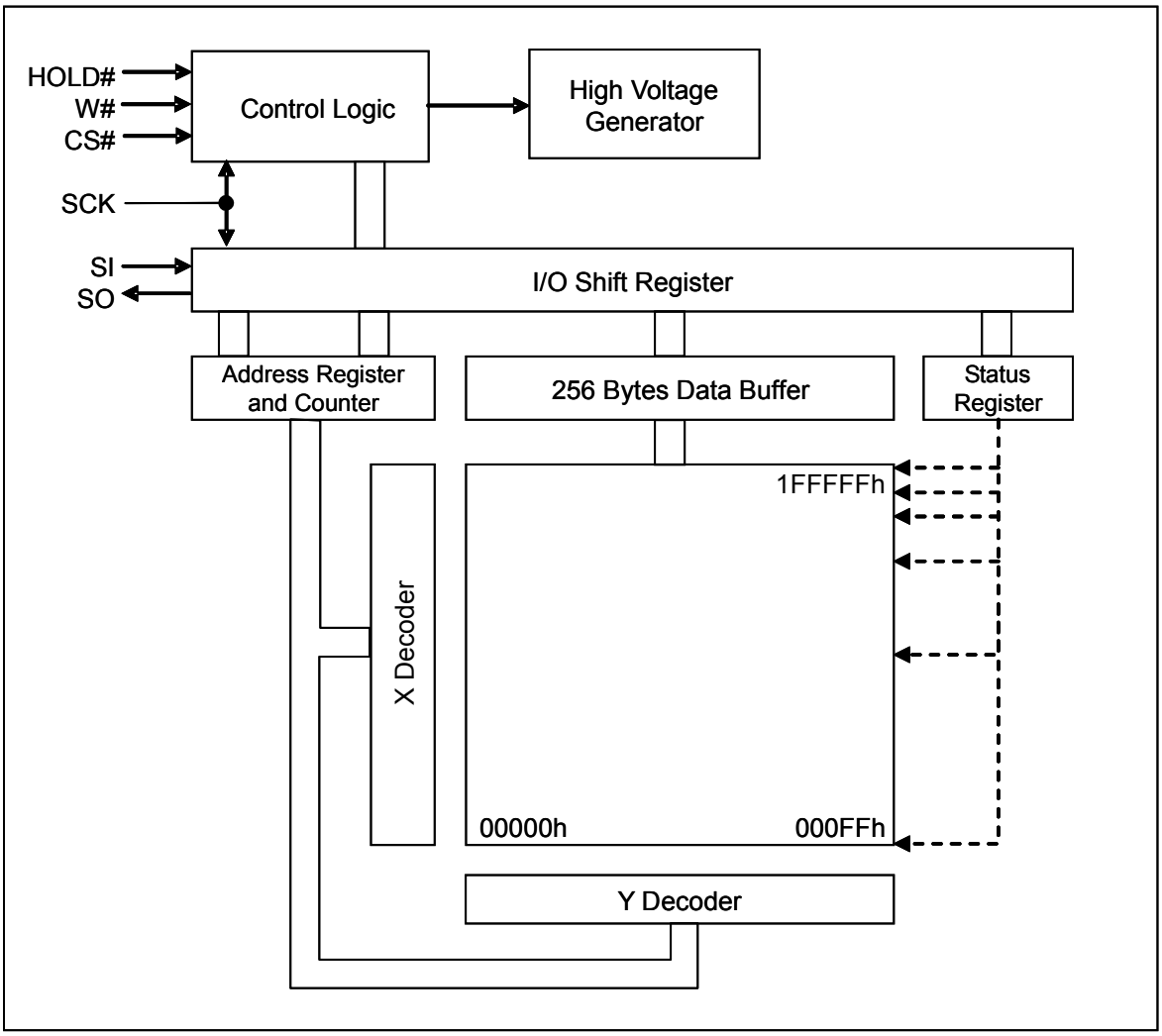
- 2,097,152 bytes (8 bits each)
- 32 sectors (65536 bytes , 512 Kbits each)
- 8192 pages (256 bytes each).

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector or Bulk Erasable (bits are erased from 0 to 1).

Table 3. Memory organization

Sector	SubSector	Address Range		Sector	SubSector	Address Range	
31	511	1FF000h	1FFFFFh	15	255	FF000h	FFFFFh
	...	...	...		...	...	...
	496	1F0000h	1F0FFFh		240	F0000h	F0FFFh
30	495	1EF000h	1EFFFFh	14	239	EF000h	EFFFFh
	...	...	...		...	...	...
	480	1E0000h	1E0FFFh		224	E0000h	E0FFFh
29	479	1DF000h	1DFFFFh	13	223	DF000h	DFFFFh
	...	...	...		...	...	...
	464	1D0000h	1D0FFFh		208	D0000h	D0FFFh
28	463	1CF000h	1CFFFFh	12	207	CF000h	CFFFFh
	...	...	...		...	...	...
	448	1C0000h	1C0FFFh		192	C0000h	C0FFFh
27	447	1BF000h	1BFFFFh	11	191	BF000h	BFFFFh
	...	...	...		...	...	...
	432	1B0000h	1B0FFFh		176	B0000h	B0FFFh
26	431	1AF000h	1AFFFFh	10	175	AF000h	AFFFFh
	...	...	...		...	...	...
	416	1A0000h	1A0FFFh		160	A0000h	A0FFFh
25	415	19F000h	19FFFFh	9	159	9F000h	9FFFFh
	...	...	...		...	...	...
	400	190000h	190FFFh		144	90000h	90FFFh
24	399	18F000h	18FFFFh	8	143	8F000h	8FFFFh
	...	...	...		...	...	...
	384	180000h	180FFFh		128	80000h	80FFFh
23	383	17F000h	17FFFFh	7	127	7F000h	7FFFFh
	...	...	...		...	...	...
	368	170000h	170FFFh		112	70000h	70FFFh
22	367	16F000h	16FFFFh	6	111	6F000h	6FFFFh
	...	...	...		...	...	...
	352	160000h	160FFFh		96	60000h	60FFFh
21	351	15F000h	15FFFFh	5	95	5F000h	5FFFFh
	...	...	...		...	...	...
	336	150000h	150FFFh		80	50000h	50FFFh
20	325	14F000h	14FFFFh	4	79	4F000h	4FFFFh
	...	...	...		...	...	...
	320	140000h	140FFFh		64	40000h	40FFFh
19	319	13F000h	13FFFFh	3	63	3F000h	3FFFFh
	...	...	...		...	...	...
	304	130000h	130FFFh		48	30000h	30FFFh
18	303	12F000h	12FFFFh	2	47	2F000h	2FFFFh
	...	...	...		...	...	...
	288	120000h	120FFFh		32	20000h	20FFFh
17	287	11F000h	11FFFFh	1	31	1F000h	1FFFFh
	...	...	...		...	...	...
	272	110000h	110FFFh		16	10000h	10FFFh
16	271	10F000h	10FFFFh	0	15	0F000h	0FFFFh
	...	...	...		...	...	...
	256	104000h	104FFFh		4	04000h	04FFFh
					3	03000h	03FFFh
					2	02000h	02FFFh
					1	01000h	01FFFh
					0	00000h	00FFFh

Figure 6. Block diagram



6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (SI) is sampled on the first rising edge of Serial Clock (SCK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data input (SI), each bit being latched on the rising edges of Serial Clock (SCK).
The instruction set is listed in *Table 4*.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast Read), Fast Read Dual Output(FRDO), Fast Read Quad Output(FRQO), Read Status Register (RDSR), Read Identification (RDID) or Release from Deep Power-down, and Read Electronic Signature (RES) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Page Write (PW), Page Erase (PE), SubSector Erase (SSE), Sector Erase (SE), Bulk Erase (BE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4. Instruction set

Instruction	Description	One-byte instruction code		Address bytes	Dummy bytes	Data bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDID	Read Identification	1001 1111	9Fh	0	0	1 to 3
		1001 0000	90h	0	0	1 to 8
RDSR	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	01h	0	0	1
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞
FRDO	Read Data Bytes at Fast Read Dual Output	0011 1011	3Bh	3	1	1 to ∞
FRQO	Read Data Bytes at Fast Quad Dual Output	0110 1011	6Bh	3	1	1 to ∞
PP	Page Program	0000 0010	02h	3	0	1 to 256
PW	Page Write	0000 0000	0Ah	3	0	1 to 256
PE	Page Erase	1101 1011	DBh	3	0	0
SSE	SubSector Erase	0010 0000	20h	3	0	0
SE	Sector Erase	1101 1000	D8h	3	0	0
BE	Bulk Erase	1100 0111	C7h	0	0	0
DP	Deep Power-down	1011 1001	B9h	0	0	0
RES	Release from Deep Power-down, and Read Electronic Signature	1010 1011	ABh	0	3	1 to ∞
	Release from Deep Power-down			0	0	0

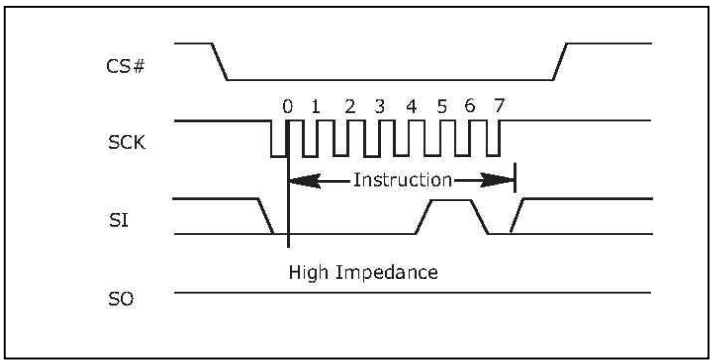
6.1 Write Enable (WREN)

The Write Enable (WREN) instruction (*Figure 7*) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Page Write (PW), Page Erase (PE), SubSector Erase (SSE), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

Figure 7. Write Enable (WREN) instruction sequence



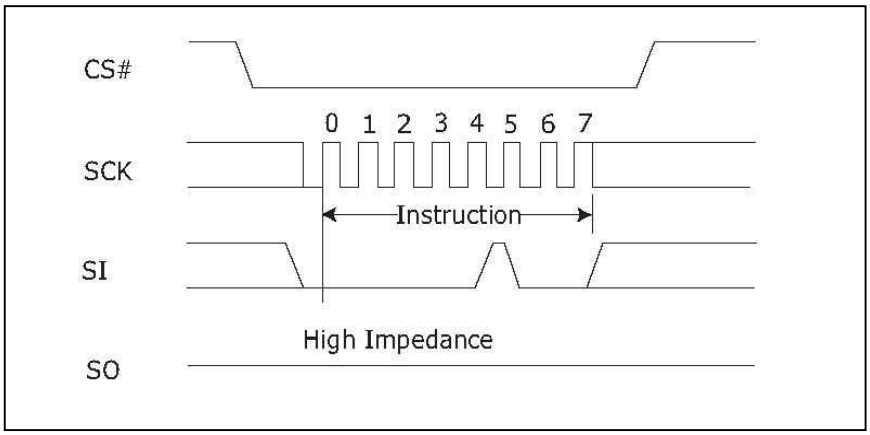
6.2 Write Disable (WRDI)

The Write Disable (WRDI) instruction (*Figure 8*) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High. The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Page Write (PW) instruction completion
- Page Erase (PE) instruction completion
- SebSector Erase (SSE) instruction completion
- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion

Figure 8. Write Disable (WRDI) instruction sequence



6.3 Read Identification (RDID)

The Read Identification (RDID) instruction allows to read the device identification data:

- Manufacturer identification (one byte or five byte)
- Device identification (two bytes)

There are two Read Identification instructions which are available for users to read the device identification data in the TSI's Flash product. One instruction(9Fh) allows the product to release one byte Manufacturer ID(20h) and another instruction(90h) does the product to release another six byte Manufacturer ID(7F7F7F7F7F20h). The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (20h), and the memory capacity of the device in the second byte (15h). Device has the same value in device identification regardless of two Read Identifications.

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select (CS#) Low. Then, the 8-bit instruction code for the instruction is shifted in. After this, the 24-bit device identification, stored in the memory will be shifted out on Serial Data Output (SO). Each bit is shifted out during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in *Figure 9*.

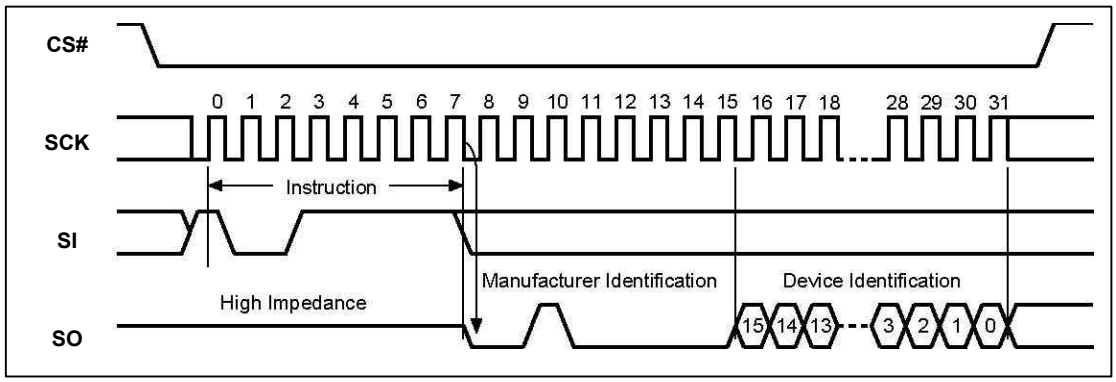
The Read Identification (RDID) instruction is terminated by driving Chip Select (CS#) High at any time during data output.

When Chip Select (CS#) is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 5. Read Identification (RDID) data-out sequence

Instruction	Manufacturer Identification	Device Identification	
		Memory Type	Memory Capacity
9Fh	20h	20h	15h

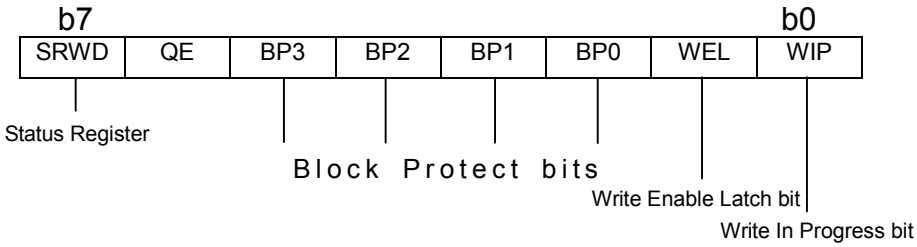
Figure 9. Read Identification (RDID) instruction sequence and data-out sequence



6.4 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 10*.

Table 6. Status Register format



The status and control bits of the Status Register are as follows:

6.4.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.4.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

6.4.3 BP3, BP2, BP1, BP0 bits

The Block Protect (BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP3, BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 2*) becomes protected against Page Program (PP), Page Write (PW), Page Erase (PE), SubSector Erase (SSE) and Sector Erase (SE) instructions. The Block Protect (BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Bulk Erase (BE) instruction is executed if, and only if, both Block Protect (BP3, BP2, BP1, BP0) bits are 0.

6.4.4 QE bit

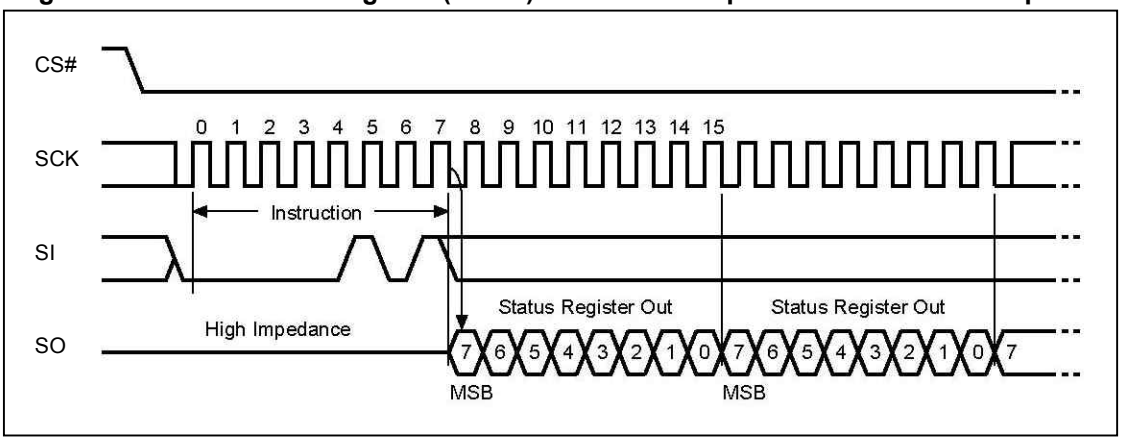
The Quad Enable(QE) is non-volatile read/write bit in the status register that allows Quad operation. When the QE bit is set to a 0 state(factory default), W# pin and HOLD# are enabled. When the QE bit is set to a 1 the Quad SO2 and SO3 pins are enabled.

WARNING : The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the W# or HOLD# pins are tied directly to the power supply or ground.

6.4.5 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect (W#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP3, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Figure 10. Read Status Register (RDSR) instruction sequence and data-out sequence



6.5 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data input (SI).

The instruction sequence is shown in *Figure 11*.

The Write Status Register (WRSR) instruction has no effect on b6, b5, b1 and b0 of the Status Register. b6 and b5 are always read as 0.

Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.
The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in *Table 2*. The Write Status Register (WRSR) instruction can set or reset the Quad enable(QE) bit and also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

Figure 11. Write Status Register (WRSR) instruction sequence

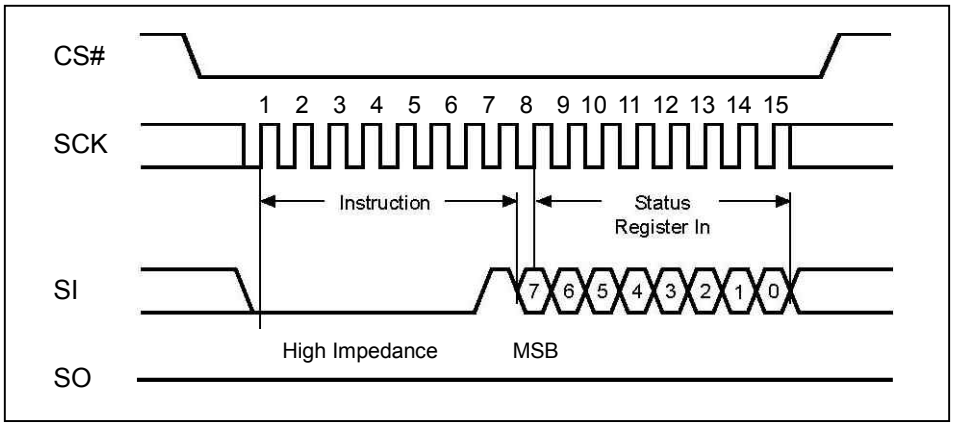


Table 7. Protection modes

W# Signal	SRWD bit	Mode	Write Protection of the Status Register	Protected Area	Unprotected Area
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the SRWD, BP3, BP2, BP1 and BP0 bits can be changed	Protected against Page Program, Page Write, Page Erase, SubSector Erase, Sector Erase and Bulk Erase	Ready to accept Page Program, Page Write, Page Erase, SubSector Erase, Sector Erase and Bulk Erase
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the SRWD, BP3, BP2, BP1 and BP0 bits cannot be changed	Protected against Page Program, Page Write, Page Erase, SubSector Erase, Sector Erase and Bulk Erase	Ready to accept Page Program, Page Write, Page Erase, SubSector Erase, Sector Erase and Bulk Erase

1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *Table 2*.

The protection features of the device are summarized in *Table 7*.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect (W#) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect (W#):

- If Write Protect (W#) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect (W#) is driven Low, it is not possible to write to the Status Register even if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect (W#) Low
- or by driving Write Protect (W#) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect (W#) High.

If Write Protect (W#) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, can be used.

6.6 Read Data Bytes (READ)

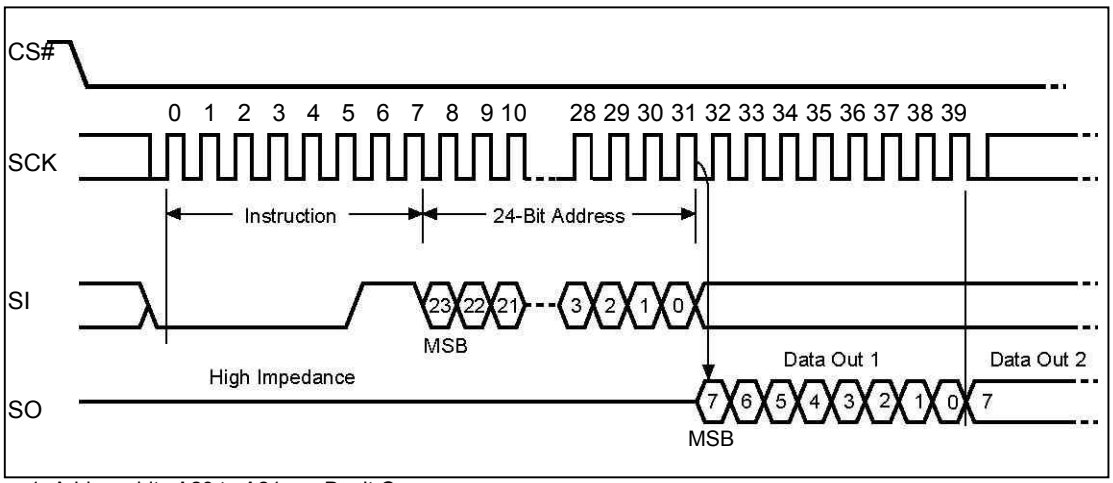
The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, is shifted out on Serial Data Output (SO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in *Figure 12*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allows the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12. Read Data Bytes (READ) instruction sequence and data-out sequence



1. Address bits A23 to A21 are Don't Care.

6.7 Read Data Bytes at Higher Speed (FAST_READ)

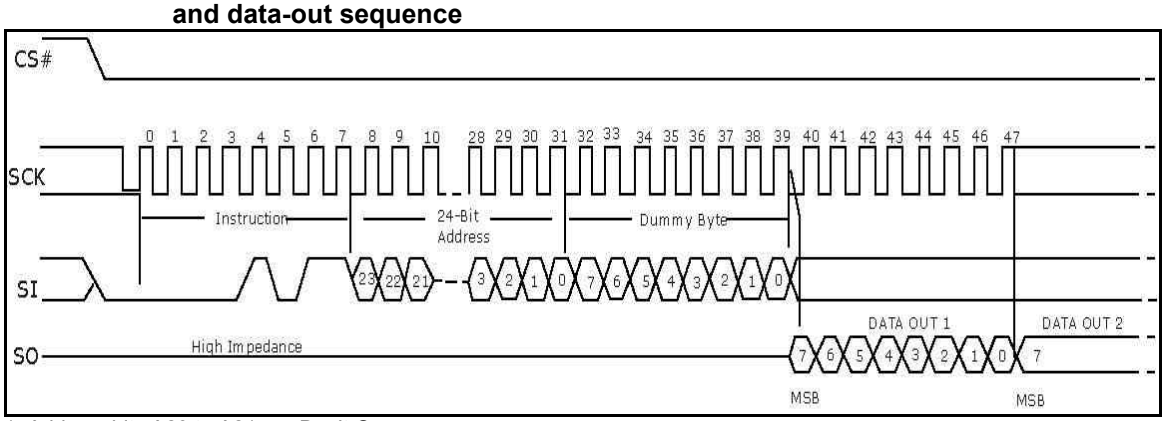
The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, is shifted out on Serial Data Output (SO), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in *Figure 13*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allows the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 13. Read Data Bytes at Higher Speed (FAST_READ) instruction sequence and data-out sequence



1. Address bits A23 to A21 are Don't Care.

6.8 Fast Read Dual Output(FRDO)

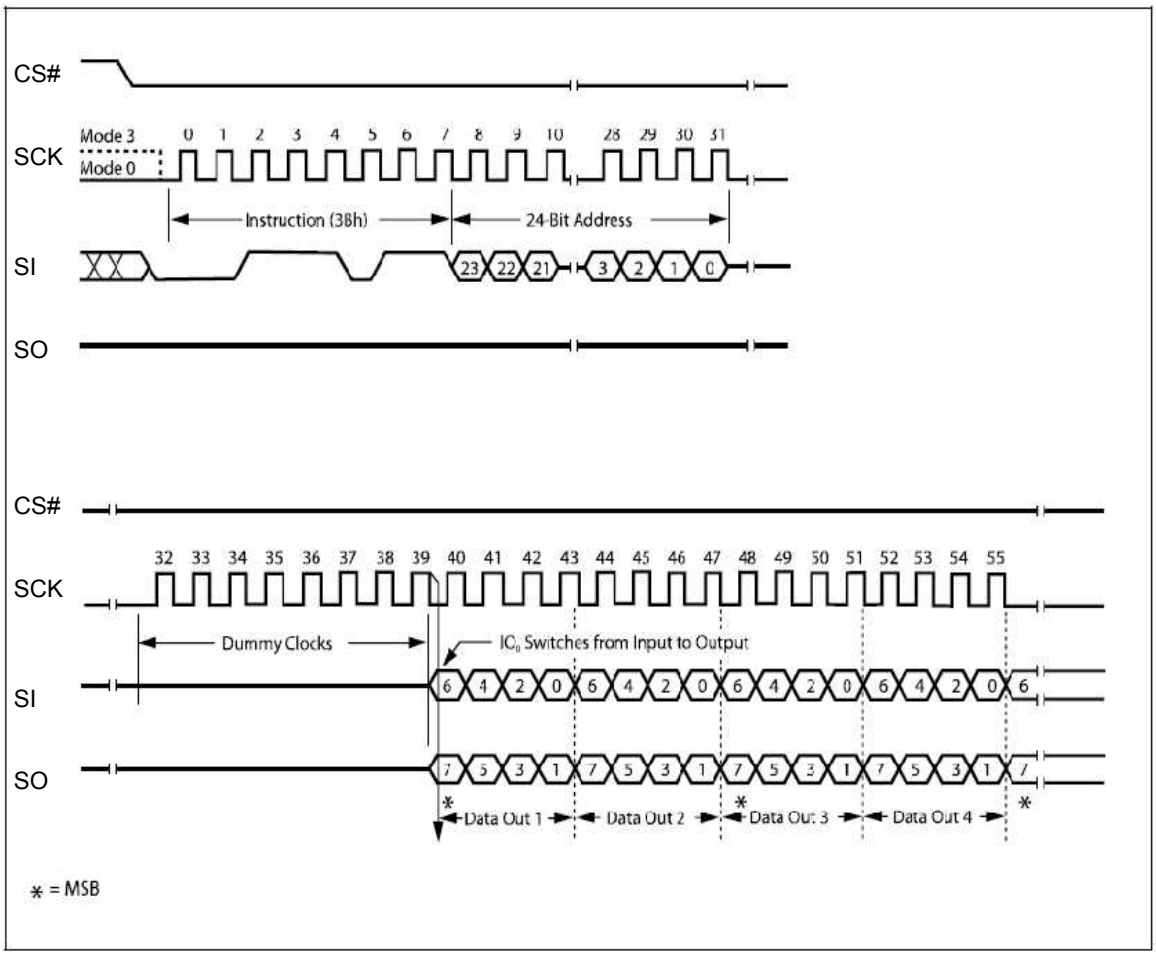
The Fast Read Dual Output (FRDO) instruction is very similar to the Read Data Bytes at higher speed (FAST_READ) instruction except that the data are shifted out on two pins (pin SO0, SO1). This allows data to be transferred from the TS25L26AP at twice the rate of standard SPI devices. The Fast Read Dual Output (FRDO) instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to RAM for execution.

The device is first selected by driving Chip Select (S) Low. The instruction code for the Dual Output Fast Read instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, are shifted out on SO0 and SO1 at a maximum frequency fC, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 14*.

The input data during the dummy clocks is “don’t care.” However, the SO0 pin should be high impedance prior to the falling edge of the first data out clock.

Figure 14. Fast Read Dual Output instruction sequence



1. Address bits A23 to A21 are Don’t Care.

6.9 Fast Read Quad Output(FRQO)

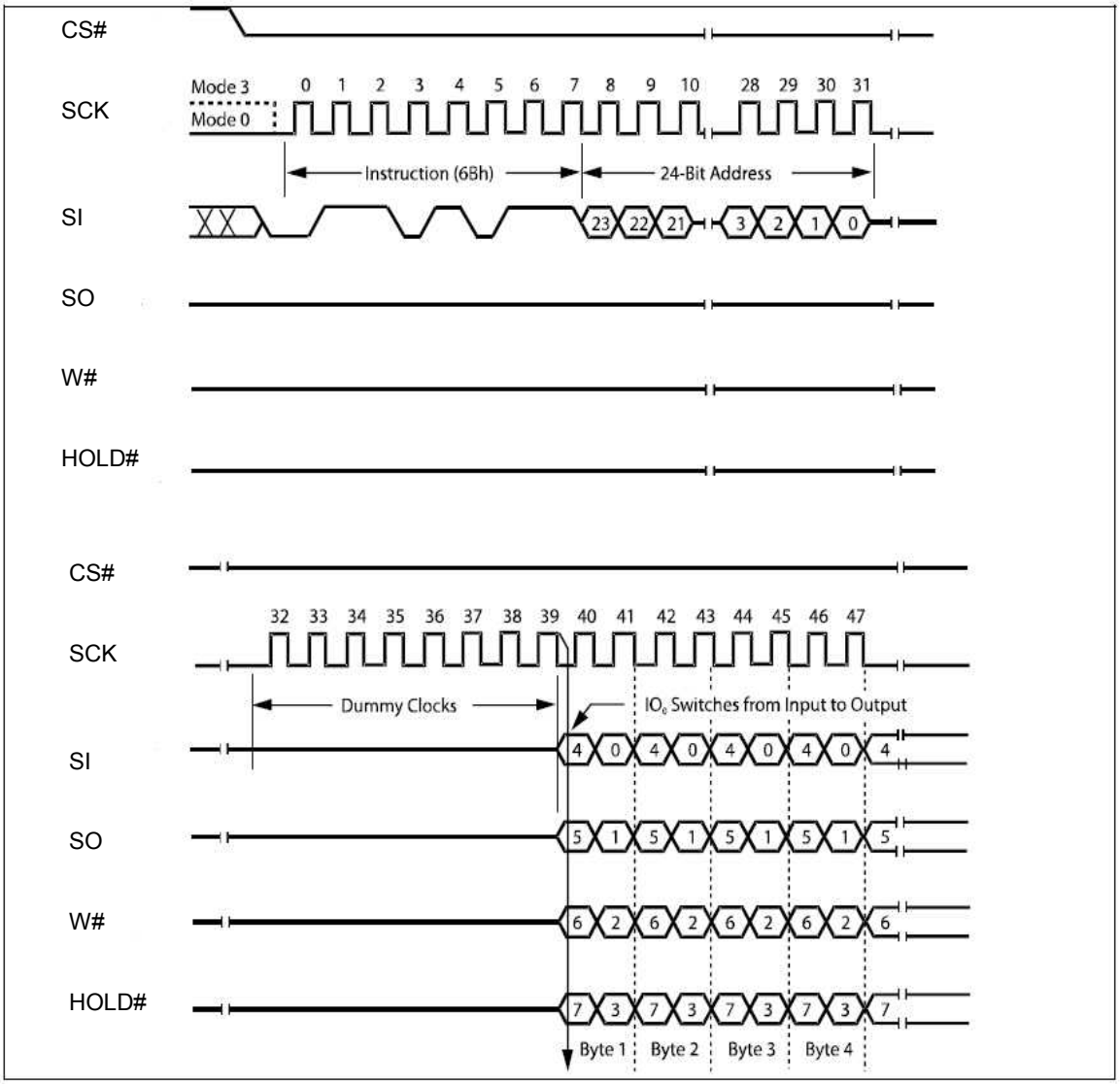
The Fast Read Quad Output (FRQO) instruction is very similar to the Fast Read Dual Output (FRDO) instruction except that the data are shifted out on four pins (pin SO0, SO1, SO2, SO3). This allows data to be transferred from the TS25L26AP at four times the rate of standard SPI devices. The Fast Read Dual Output (FRQO) instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to RAM for execution. A Quad enable of status register bit must be executed before the device will accept the Fast Read Quad Output instruction (Status Register bit, QE must equal 1).

The device is first selected by driving Chip Select (S) Low. The instruction code for the Dual Output Fast Read instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, are shifted out on SO0, SO1, SO2 and SO3 at a maximum frequency fC, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 15*.

The input data during the dummy clocks is “don’t care.” However, the SO pins should be high impedance prior to the falling edge of the first data out clock.

Figure 15. Fast Read Quad Output instruction sequence



6.10 Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data input (SI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 16*.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few bytes (see *Table 15: AC characteristics (75 MHz operation)*).

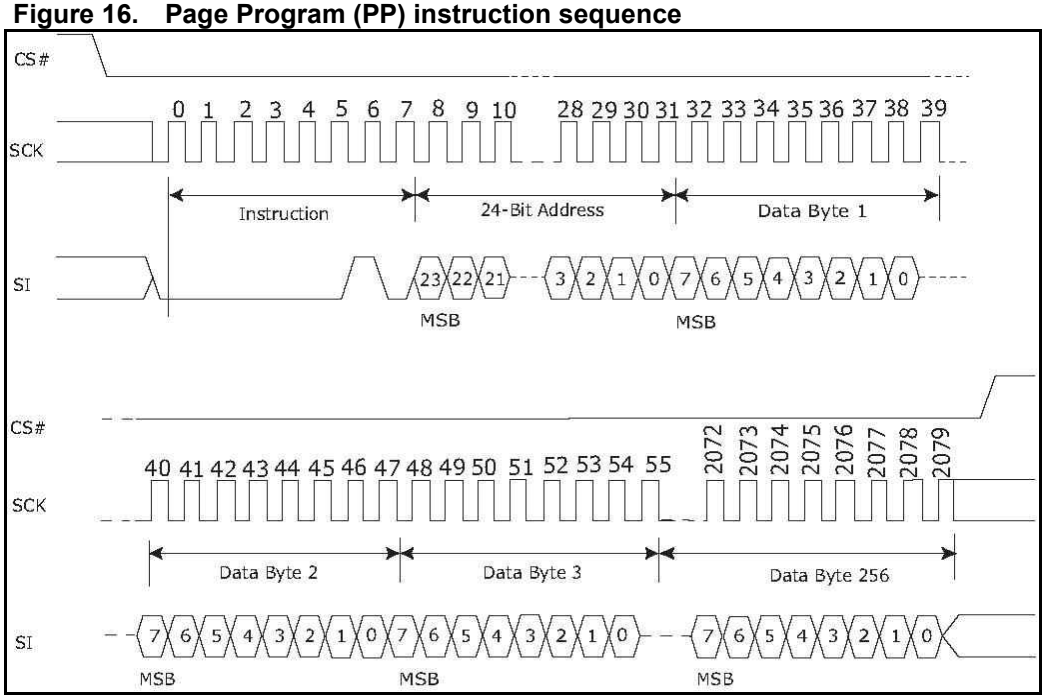
Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP3, BP2, BP1, BP0) bits (see *Table 3* and *Table 2*) is not executed

If Reset (Reset) is driven Low while a Page Program (PP) cycle is in progress, the Page Program cycle is interrupted and the programmed data may be corrupted (see *Table 15: Device status after a Reset Low pulse*). On Reset going Low, the device enters the Reset mode and a time of t_{RHSL} is then required before the device can be re-selected by driving Chip Select (S) Low. For the value of t_{RHSL} see *Table 24: Timings after a Reset Low pulse* in *Section 11: DC and AC parameters*.

Figure 16. Page Program (PP) instruction sequence



1. Address bits A23 to A21 are Don't Care.

6.11 Page Write (PW)

The Page Write (PW) instruction allows Bytes to be written in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Write (PW) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address Bytes and at least one data Byte on Serial Data Input (SI). The rest of the page remains unchanged if no power failure occurs during this write cycle.

The Page Write (PW) instruction performs a page erase cycle even if only one Byte is updated.

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary roll over, and are written from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 17*.

If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be written correctly within the same page. If less than 256 Data Bytes are sent to device, they are correctly written at the requested addresses without having any effects on the other Bytes of the same page.

For optimized timings, it is recommended to use the Page Write (PW) instruction to write all consecutive targeted Bytes in a single sequence versus using several Page Write (PW) sequences with each containing only a few Bytes.

Chip Select (CS#) must be driven High after the eighth bit of the last data Byte has been latched in, otherwise the Page Write (PW) instruction is not executed.

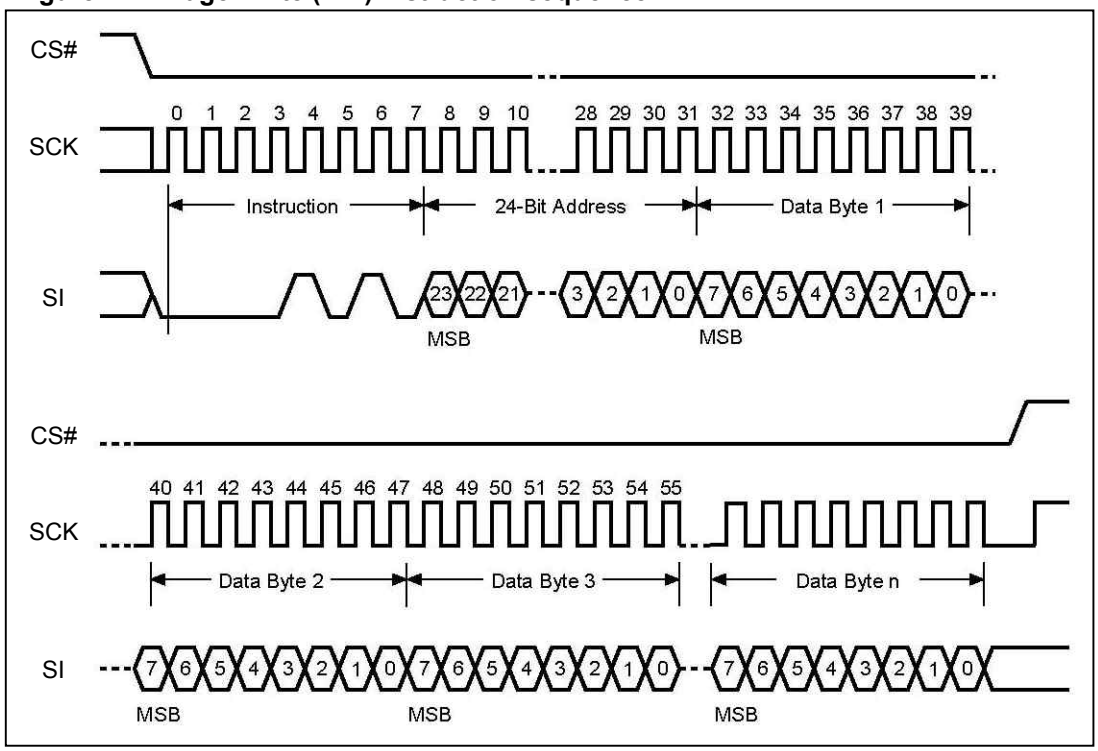
As soon as Chip Select (CS#) is driven High, the self-timed Page Write cycle (whose duration is t_{PW}) is initiated. While the Page Write cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Write cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Write (PW) instruction applied to a page that is Hardware or Software Protected is not executed.

Any Page Write (PW) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

If Reset (Reset) is driven Low while a Page Write (PW) cycle is in progress, the Page Write cycle is interrupted and the programmed data may be corrupted (see *Table 15: Device status after a Reset Low pulse*). On Reset going Low, the device enters the Reset mode and a time of t_{RHSL} is then required before the device can be re-selected by driving Chip Select (CS#) Low. For the value of t_{RHSL} see *Table 24: Timings after a Reset Low pulse* in *Section 11: DC and AC parameters*.

Figure 17. Page Write (PW) instruction sequence



1. Address bits A23 to A21 are Don't Care
2. 1 ≤n ≤256

6.12 Page Erase (PE)

The Page Erase (PE) instruction sets to 1 (FFh) all bits inside the chosen page. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Erase (PE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address Bytes on Serial Data Input (SI). Any address inside the Page is a valid address for the Page Erase (PE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

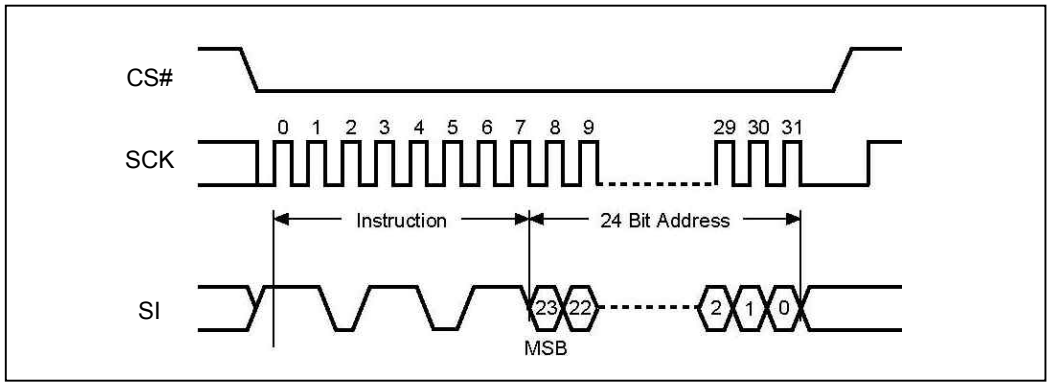
The instruction sequence is shown in *Figure 18*.

Chip Select (CS#) must be driven High after the eighth bit of the last address Byte has been latched in, otherwise the Page Erase (PE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Page Erase cycle (whose duration is t_{PE}) is initiated. While the Page Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Erase (PE) instruction applied to a page that is Hardware or software Protected is not executed.

Any Page Erase (PE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 18. Page Erase (PE) instruction sequence



1. Address bits A23 to A21 are Don't Care.

6.13 SubSector Erase (SSE)

The SubSector Erase (SSE) instruction sets to 1 (FFh) all bits inside the chosen subsector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The SubSector Erase (SSE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address Bytes on Serial Data Input (SI). Any address inside the SubSector (see *Table 5*) is a valid address for the SubSector Erase (SSE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

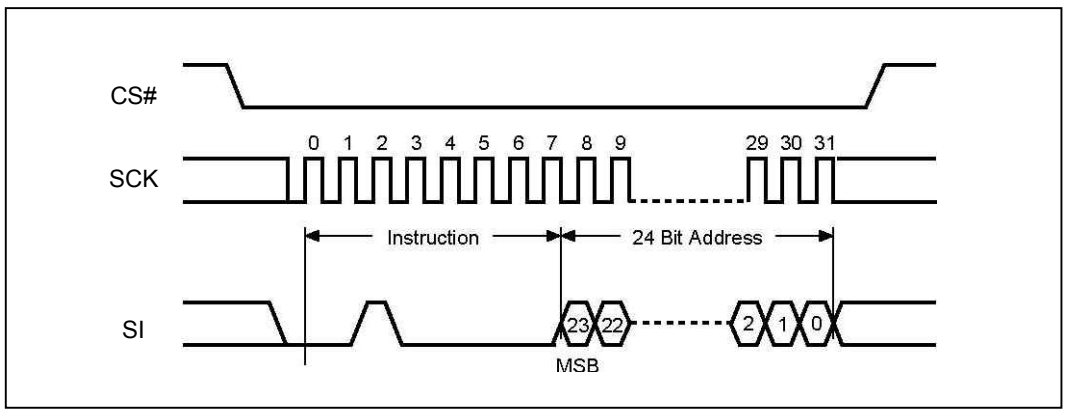
The instruction sequence is shown in *Figure 19*.

Chip Select (CS#) must be driven High after the eighth bit of the last address Byte has been latched in, otherwise the SubSector Erase (SSE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed SubSector Erase cycle (whose duration is t_{SSE}) is initiated. While the SubSector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed SubSector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A SubSector Erase (SSE) instruction applied to a subsector that contains a page that is Hardware or software Protected is not executed.

Any SubSector Erase (SSE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 19. SubSector Erase (SSE) instruction sequence



1. Address bits A23 to A21 are Don't Care.

6.14 Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

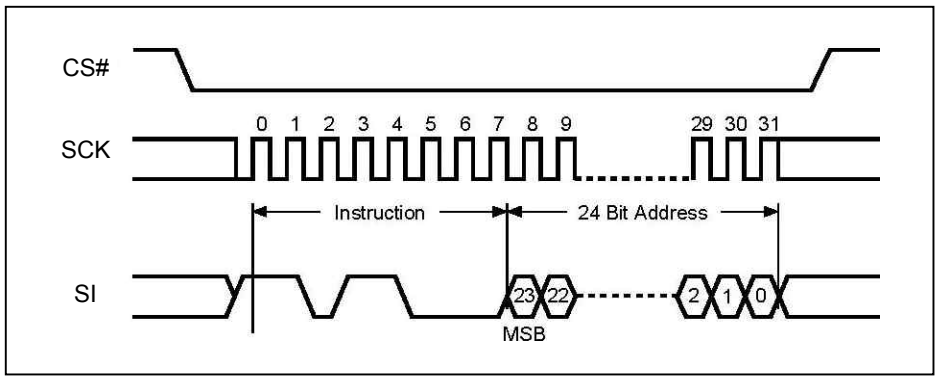
The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (SI). Any address inside the Sector (see *Table 3*) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 20*.

Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a page which is protected by the Block Protect (BP3, BP2, BP1, BP0) bits (see *Table 3* and *Table 2*) is not executed.

Figure 20. Sector Erase (SE) instruction sequence



1. Address bits A23 to A21 are Don't Care.

6.15 Bulk Erase (BE)

The Bulk Erase (BE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

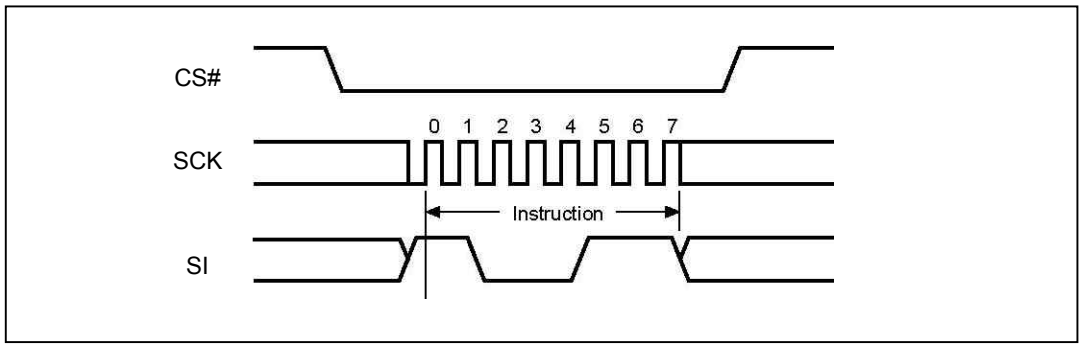
The Bulk Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 21*.

Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Bulk Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Bulk Erase (BE) instruction is entered when some Block Protect (BP3, BP2, BP1, BP0) bits are issued, all sector except protected sectors are erased.

Figure 21. Bulk Erase (BE) instruction sequence



6.16 Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in *Table 14*).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (SO).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode.

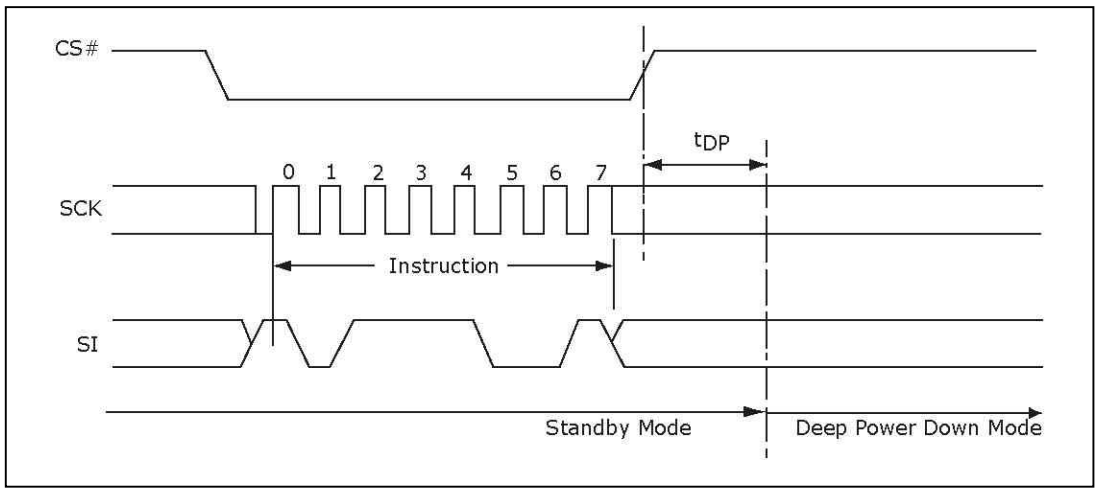
The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 22*.

Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 22. Deep Power-down (DP) instruction sequence



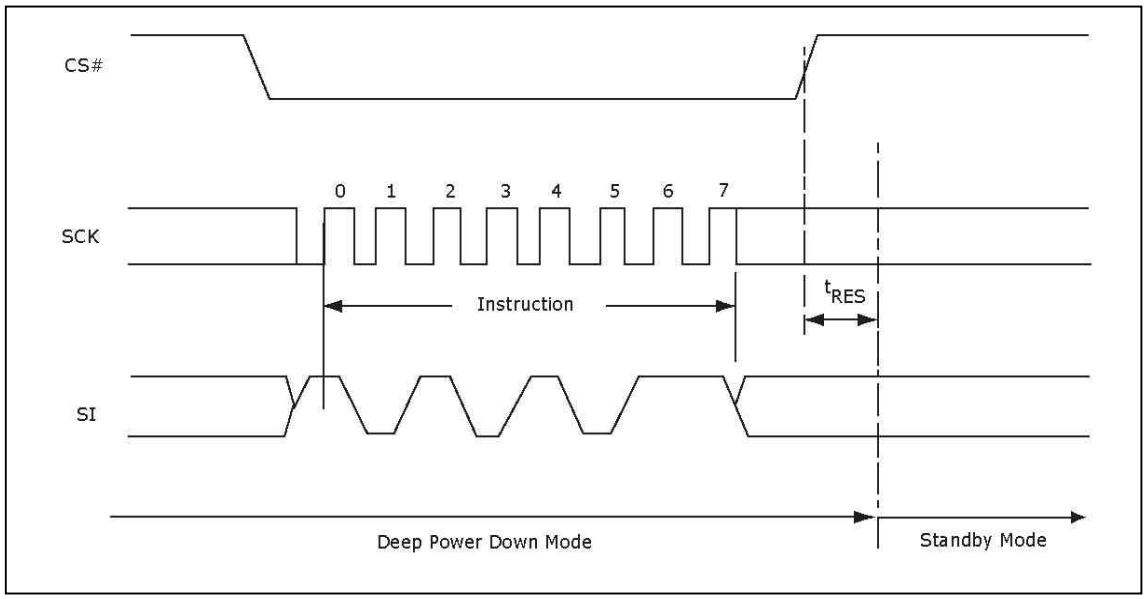
6.17 Release from Deep Power-down (RES)

The Release from Deep Power-down (RES) instruction provides the only way to exit the Deep Power Down mode. Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down (RES) instruction. Executing this instruction takes the device out of Deep Power Down mode.

The Release from Deep Power-down (RES) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

Driving Chip Select (CS#) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit Electronic Signature has been transmitted for the first time (as shown in *Figure 23*), still insures that the device is put into Standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES1}, and Chip Select (CS#) must remain High for at least t_{RES1}(max), as specified in *Table 15*. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 23. Release from Deep Power-down



6.18 Release from Deep Power-down and Read Electronic Signature (RES)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

The instruction can also be used to read, on Serial Data Output (SO), the 8-bit Electronic Signature, whose value for the *TS25L16APP* is *14h*.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Electronic Signature (RES) instruction always provides access to the 8-bit Electronic Signature of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Electronic Signature (RES) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

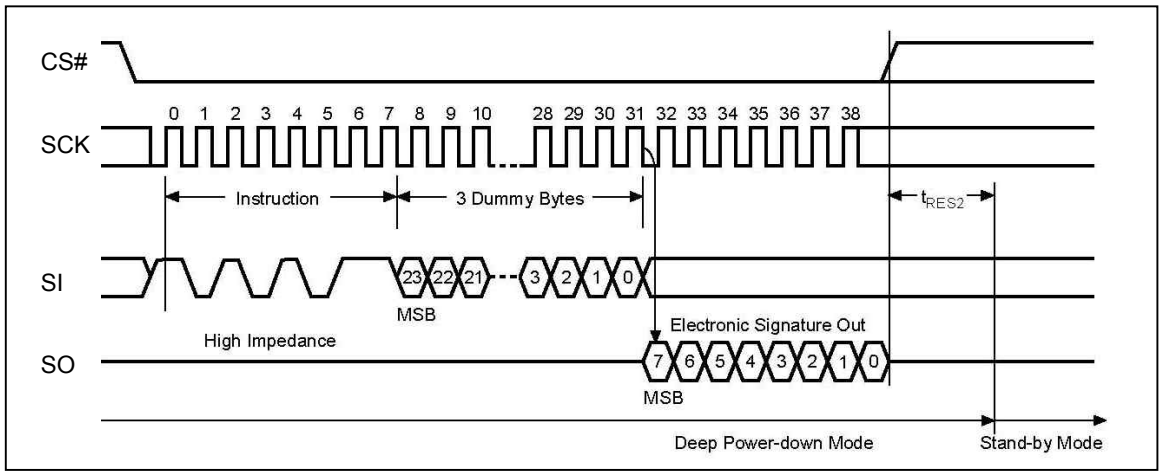
The device is first selected by driving Chip Select (CS#) Low. The instruction code is followed by 3 dummy bytes, each bit being latched-in on Serial Data Input (SI) during the rising edge of Serial Clock (SCK). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (SO), each bit being shifted out during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in *Figure 24*.

The Release from Deep Power-down and Read Electronic Signature (RES) instruction is terminated by driving Chip Select (CS#) High after the Electronic Signature has been read at least once. Sending additional clock cycles on Serial Clock (SCK), while Chip Select (CS#) is driven Low, cause the Electronic Signature to be output repeatedly.

When Chip Select (CS#) is driven High, the device is put in the Standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain High for at least t_{RES2}(max), as specified in *Table 15*. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 24. Release from Deep Power-down and Read Electronic Signature (RES) instruction sequence



1. The value of the 8-bit Electronic Signature, for the TS25L16AP, is 14h.

7 Power-up and Power-down

At Power-up and Power-down, the device must not be selected (that is Chip Select (S) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at Power-up, and then for a further delay of t_{VSL}
- V_{SS} at Power-down

To avoid data corruption and inadvertent write operations during Power-up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold value, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Program (PP), Page Write (PW), Page Erase (PE), SubSector Erase (SSE), Sector Erase (SE), Bulk Erase (BE) and Write Status Register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write Status Register, Program or Erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the V_{WI} threshold
- t_{VSL} after V_{CC} passed the V_{CC}(min) level

These values are specified in *Table 8*.

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for READ instructions even if the t_{PUW} delay is not yet fully elapsed. At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-down mode).
- The Write Enable Latch (WEL) bit is reset.
- The Write In Progress (WIP) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 100 nF).

At Power-down, when V_{CC} drops from the operating voltage, to below the Power On Reset (POR) threshold value, V_{WI}, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

Figure 25. Power-up timing

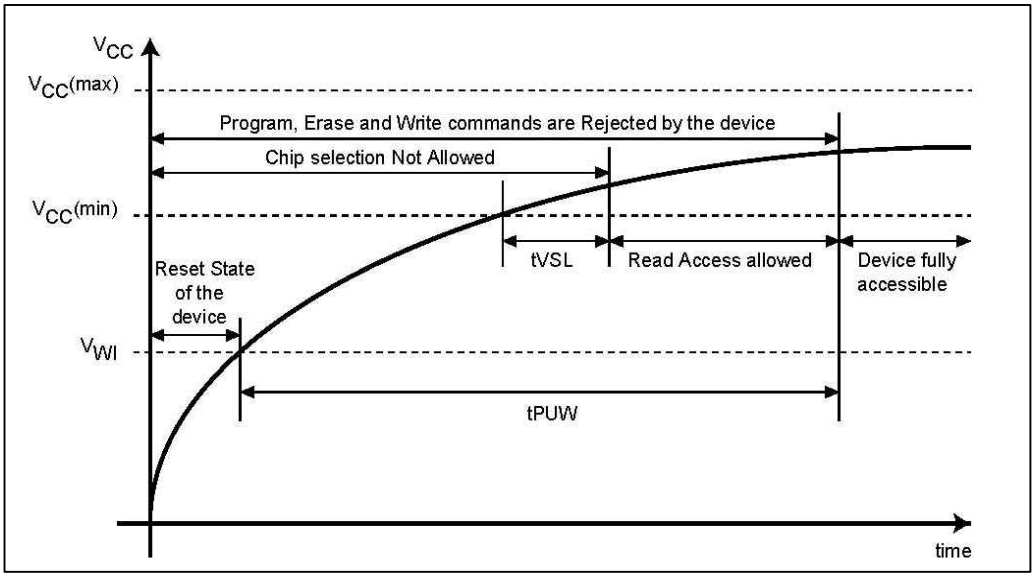


Table 8. Power-up timing and V_{WI} threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}(1)	Vcc(min) to S low	10		µs
t_{PUW}(1)	Time delay to Write instruction	1	10	ms
V_{WI}(1)	Write Inhibit voltage	1	2	V

1. These parameters are characterized only.

8 Initial delivery state

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

9 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to relevant quality documents.

Table9. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering		see (0)	°C
V_{IO}	Input and output voltage (with respect to ground)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4.0	V
V_{ESD}	Electrostatic discharge voltage (Human Body model) (1)	–2000	2000	V

0. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly)
1. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω , R2=500 Ω)

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 10. Operating conditions

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply voltage		2.7	3.6	V
T_A	Ambient operating temperature	I(Industrial)	–40	85	°C
		C(Commercial)	0	70	°C

Table 11. Data retention and endurance

Parameter	Condition	Min.	Max.	Unit
Erase/Program cycles			100,000	cycles per sector
Data Retention			20	years

Table 12. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		5	ns
	Input pulse voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input timing reference voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output timing reference voltages	V_{CC} / 2		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 26. AC measurement I/O waveform

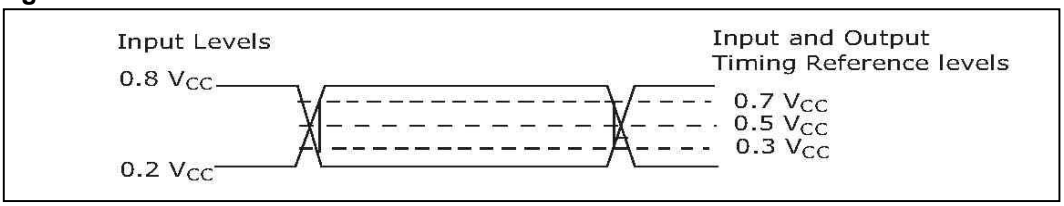


Table 13. Capacitance[1]

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 20 MHz.

Table 14. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table10*)	Min.	Max.	Unit
I_{LI}	Input leakage current			± 2	µA
I_{LO}	Output leakage current			± 2	µA
I_{CC1}	Standby current	S = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	µA
I_{CC2}	Deep Power-down current	S = V_{CC}, V_{IN} = V_{SS} or V_{CC}		1	µA
I_{CC3}	Operating current (READ)	C = 0.1V_{CC} / 0.9.V_{CC} at 75 MHz, Q = open		12	mA
		C = 0.1V_{CC} / 0.9.V_{CC} at 33 MHz, Q = open		4	mA
I_{CC4}	Operating current (PP)	S = V_{CC}		15	mA
I_{CC5}	Operating current (WRSR)	S = V_{CC}		15	mA
I_{CC6}	Operating current (SE)	S = V_{CC}		15	mA
I_{CC7}	Operating current (BE)	S = V_{CC}		15	mA
V_{IL}	Input low voltage		–0.5	0.3V_{CC}	V
V_{IH}	Input high voltage		0.7V_{CC}	V_{CC} + 0.4	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –100 µA	V_{CC} – 0.2		V

Table 15. AC characteristics (75 MHz operation)

Test conditions specified in *Table10* and *Table12*						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.(1)**	**Max.**	**Unit**
f_C	fC	Clock frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDID, RDSR, WRSR	D.C.		75	MHz
f_R		Clock frequency for READ instructions	D.C.		33	MHz
t_{CH}(2)	tCLH	Clock High time	11			ns
t_{CL}(2)	tCLL	Clock Low time	11			ns
t_{CLCH}(3)		Clock Rise time(4) (peak to peak)	0.1			V/ns
t_{CHCL}(3)		Clock Fall time(3) (peak to peak)	0.1			V/ns
t_{SLCH}	tCSS	S active setup time (relative to C)	5			ns
t_{CHSL}		S not active hold time (relative to C)	5			ns
t_{DVCH}	tDSU	Data In setup time	2			ns
t_{CHDX}	tDH	Data In hold time	5			ns
t_{CHSH}		S active hold time (relative to C)	5			ns
t_{SHCH}		S not active setup time (relative to C)	5			ns
t_{SHSL}	tCSH	S deselect time	100			ns
t_{SHQZ}(3)	tDIS	Output disable time			8	ns
t_{CLQV}	tV	Clock Low to Output Valid			8	ns
t_{CLQX}	tHO	Output hold time	0			ns
t_{HLCH}		HOLD setup time (relative to C)	5			ns
t_{CHHH}		HOLD hold time (relative to C)	5			ns
t_{HHCH}		HOLD setup time (relative to C)	5			ns
t_{CHHL}		HOLD hold time (relative to C)	5			ns
t_{HHQX}(3)	tLZ	HOLD to Output Low-Z			9	ns
t_{HLQZ}(3)	tHZ	HOLD to Output High-Z			9	ns
t_{WHSL}(5)		Write Protect setup time	20			ns
t_{SHWL}(5)		Write Protect hold time	100			ns
t_{DP}(3)		S High to Deep Power-down mode			3	µs
t_{RES1}(3)		S High to Standby mode without Electronic Signature Read			3	µs
t_{RES2}(3)		S High to Standby mode with Electronic Signature Read			1.8	µs
t_W		Write Status Register cycle time		2.5	3	ms
t_{PP}		Page Program time		0.3	0.7	ms
t_{PW}		Page Write time		2.8	3.6	ms
t_{PE}		Page Erase time		2.2	3	ms
t_{SSE}		SubSector Erase time		2.2	3	ms
t_{SE}		Sector Erase time		32	48	ms
t_{BE}		Bulk Erase time		1	1.5	s

1 Typical values given for T_A = 25°C.
2 t_{CH} + t_{CL} must be greater than or equal to 1/ fc
3 Value guaranteed by characterization, not 100% tested in production.
4 Expressed as a slew-rate.
5 Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.

Figure 27. Serial input timing

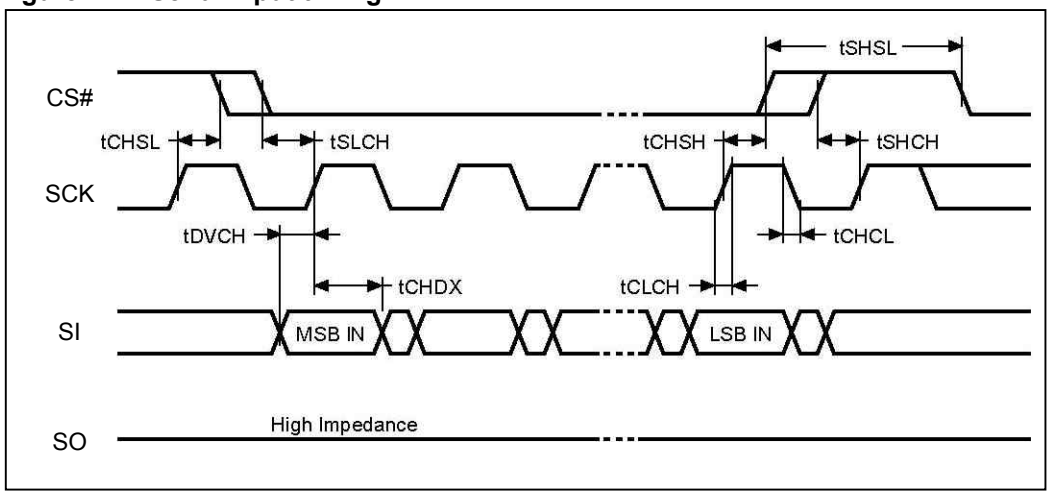


Figure 28. Write protect setup and hold timing during WRSR and SRWD = 1

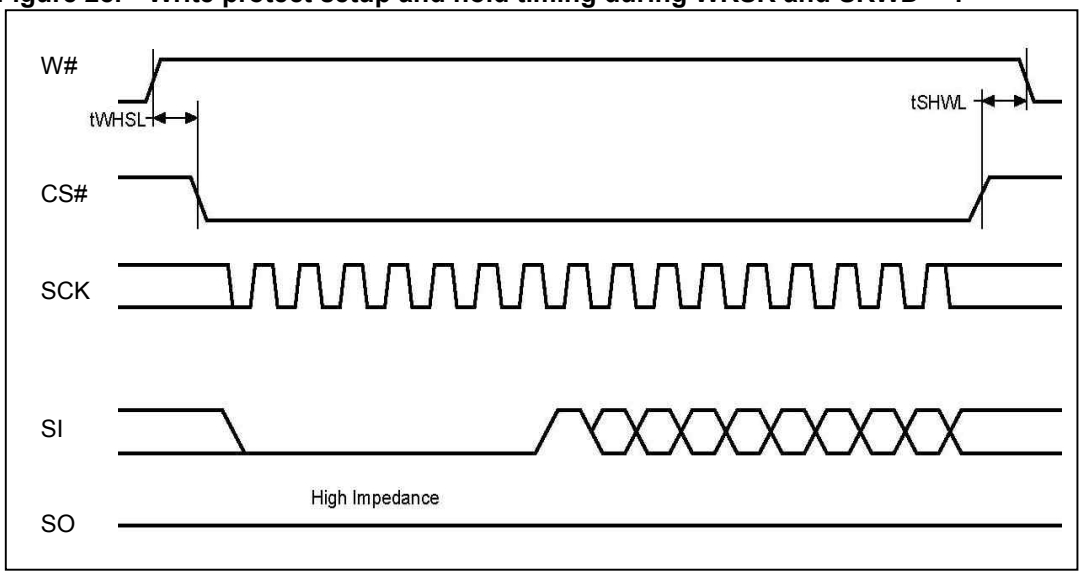


Figure 29. Hold timing

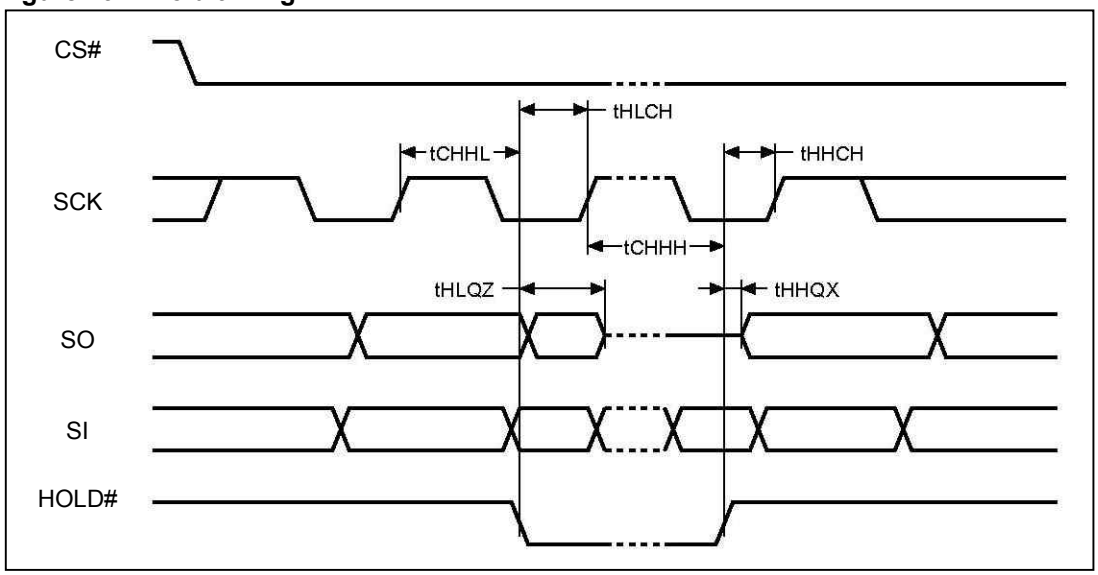
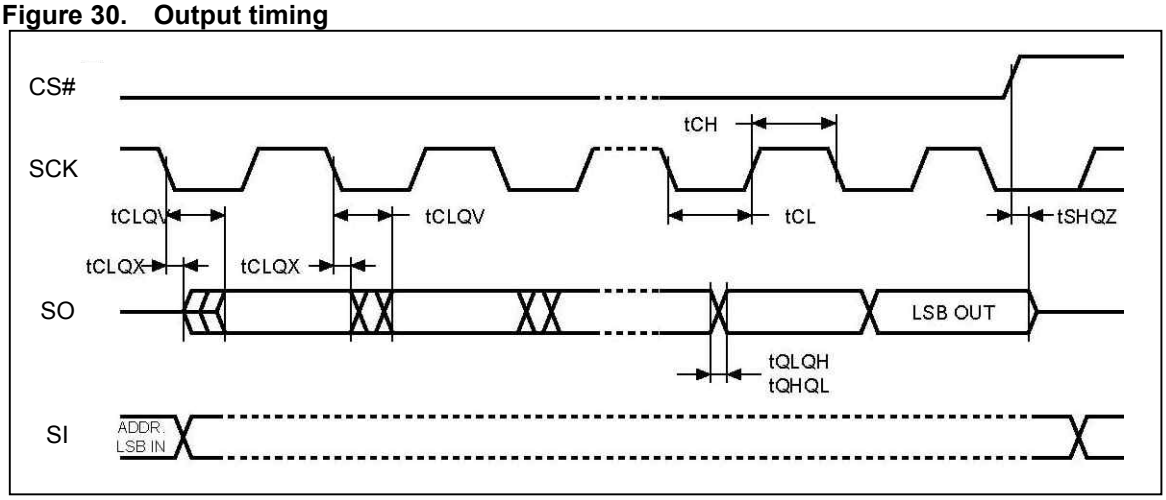
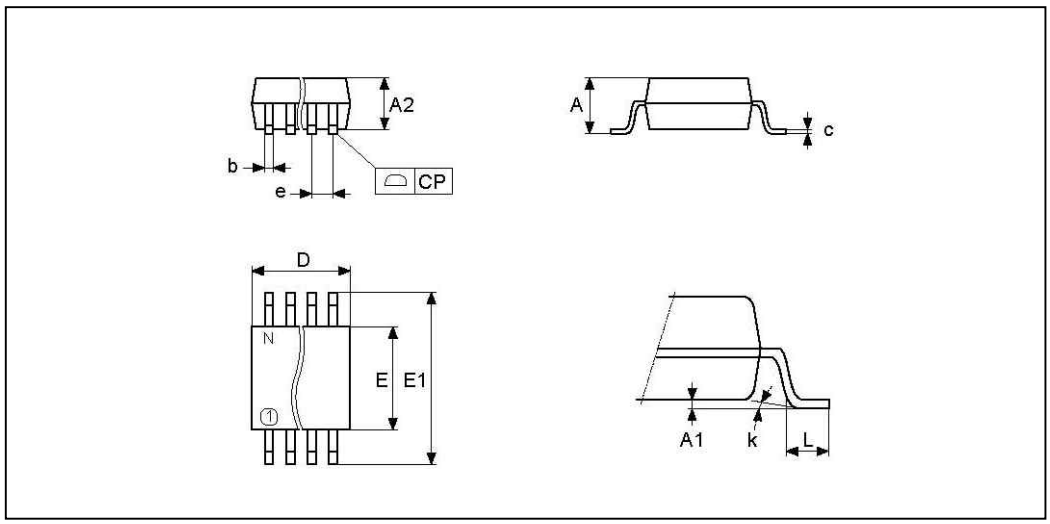


Figure 30. Output timing



11 Package mechanical

Figure 31. SOP – 8 lead Plastic Small Outline, 208 mils body width, package outline

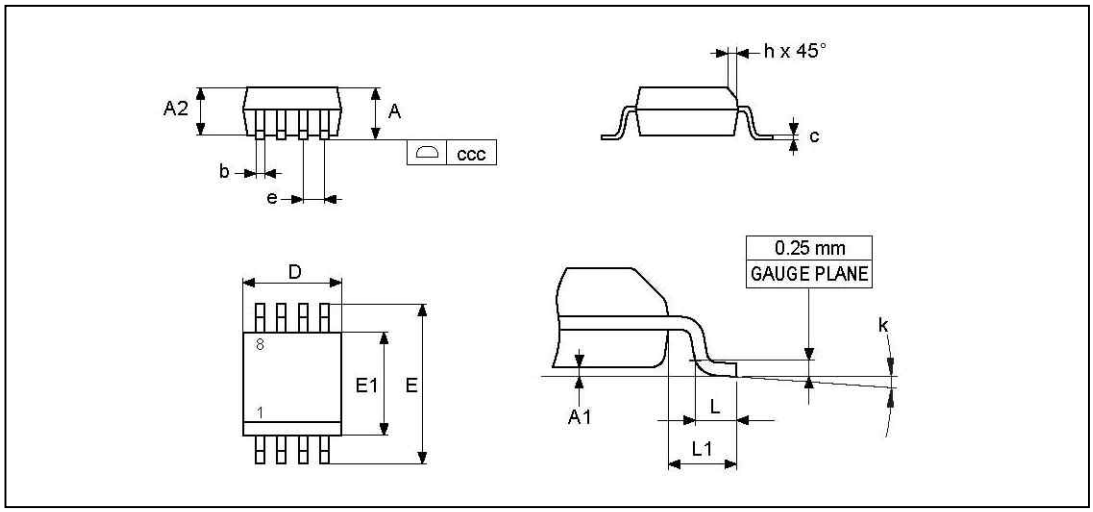


1 Drawing is not to scale.
2 The '1' that appears in the top view of the package shows the position of pin 1.

Table 16. SOP – 8 lead Plastic Small Outline, 208 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.50			0.098
A1		0.00	0.25		0.000	0.010
A2		1.51	2.00		0.059	0.079
b	0.40	0.35	0.51	0.016	0.014	0.020
c	0.20	0.10	0.35	0.008	0.004	0.014
CP			0.10			0.004
D			6.05			0.238
E		5.02	6.22		0.198	0.245
E1		7.62	8.89		0.300	0.350
e	1.27	–	–	0.050	–	–
k		0°	10°		0°	10°
L		0.50	0.80		0.020	0.031
N	8			8		

Figure 32. SOP – 8 lead Plastic Small Outline, 150 mils body width, package outline

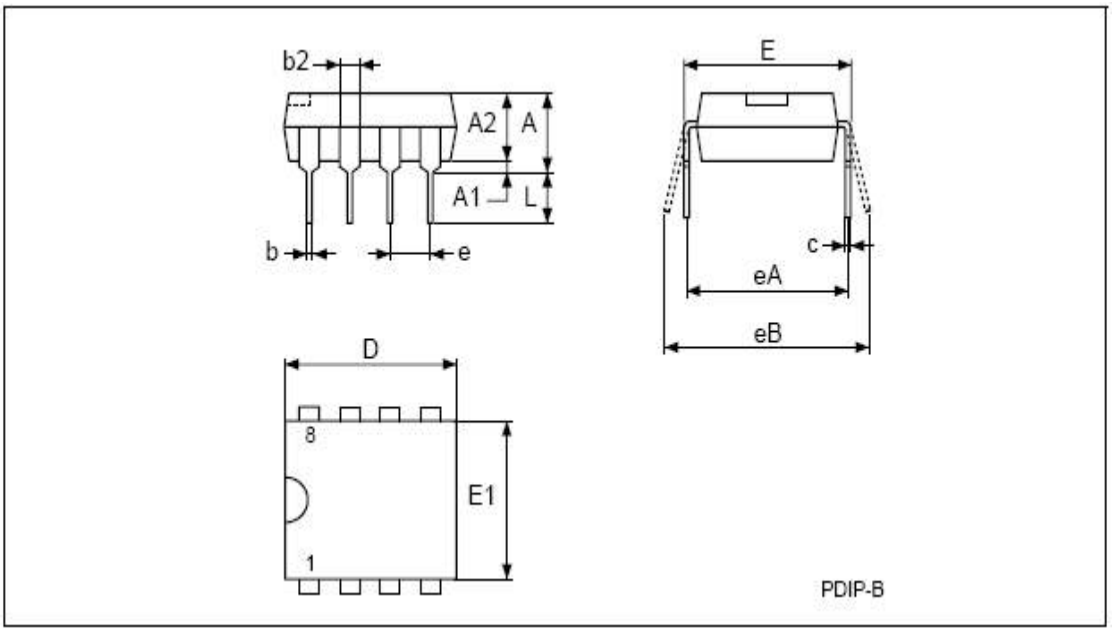


1. Package is not to scale.

Table 17. SOP – 8 lead Plastic Small Outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 33. PDIP – 8 lead Plastic Small Outline, 300 mils body width, package outline



1. Package is not to scale.

Table 18. PDIP – 8 lead Plastic Small Outline, 300 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.188
A1	0.50			0.019		
A2	3.10	3.30	3.50	0.122	0.129	0.137
b	0.38		0.55	0.014		0.021
b2	1.47	1.52	1.57	0.057	0.059	0.061
c	0.21		0.35	0.008		0.013
D	9.10	9.20	9.30	0.358	0.362	0.366
E	7.62	7.87	8.25	0.300	0.309	0.324
E1	6.25	6.35	6.45	0.246	0.250	0.253
e		2.54			0.100	
eA		7.62			0.300	
eB	7.62	8.80	10.90	0.300	0.346	0.429
L	2.92	3.30	3.81	0.114	0.122	0.150

11 Part Numbering

Table 19. Ordering information scheme