TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

Preliminary

TS4268

180mA Ultra Low Dropout Voltage Regulator with Reset & Watchdog Function

SOP-8

Pin Definition:

1. Input	8. Output
2. N/C	7. Watchdog
3. Reset Output	6. Radj
4. Ground	5. Reset Delay

General Description

TS4268 is a low dropout voltage regulator. The maximum input voltage is 45 V. It can deliver an output current of at least 180mA. TS4268 is short circuit proof and features temperature protection that disables the circuit in the event of impermissibly high temperatures. The watchdog function is disabled as a function of the load, so that a controller is not interrupted during sleep mode by a watchdog reset.

Application Description

TS4268 regulates an input voltage in the range 5.5V ~ 45V. In the event of an output voltage Vout < V_{RT}, *a* reset signal is generated. The wiring of the reset switching threshold input enables the value of V_{RT} to be reduced. The reset delay time can be adjusted using an external capacitor. The integrated watchdog monitors the connected active controller. If there is no positive going edge at the watchdog input, the reset output is set to low. The reset delay capacitor provides a wide adjustment range for the pulse repetition time. The watchdog function is only activated if the load exceeds 8mA. This ensures that a microcontroller is not activated during power-down and the current drain is not increased.

Features

- Output voltage tolerance < ± 2 %
- Very low current consumption
- Low-drop voltage
- Watchdog
- Settable reset threshold
- Over temperature protection
- Reverse polarity protection
- Short-circuit proof
- Suitable for use in automotive electronics
- Wide temperature range

Ordering Information

Part No.	Package	Packing
TS4268CS50 RL	SOP-8	2.5Kpcs/ 13” Reel

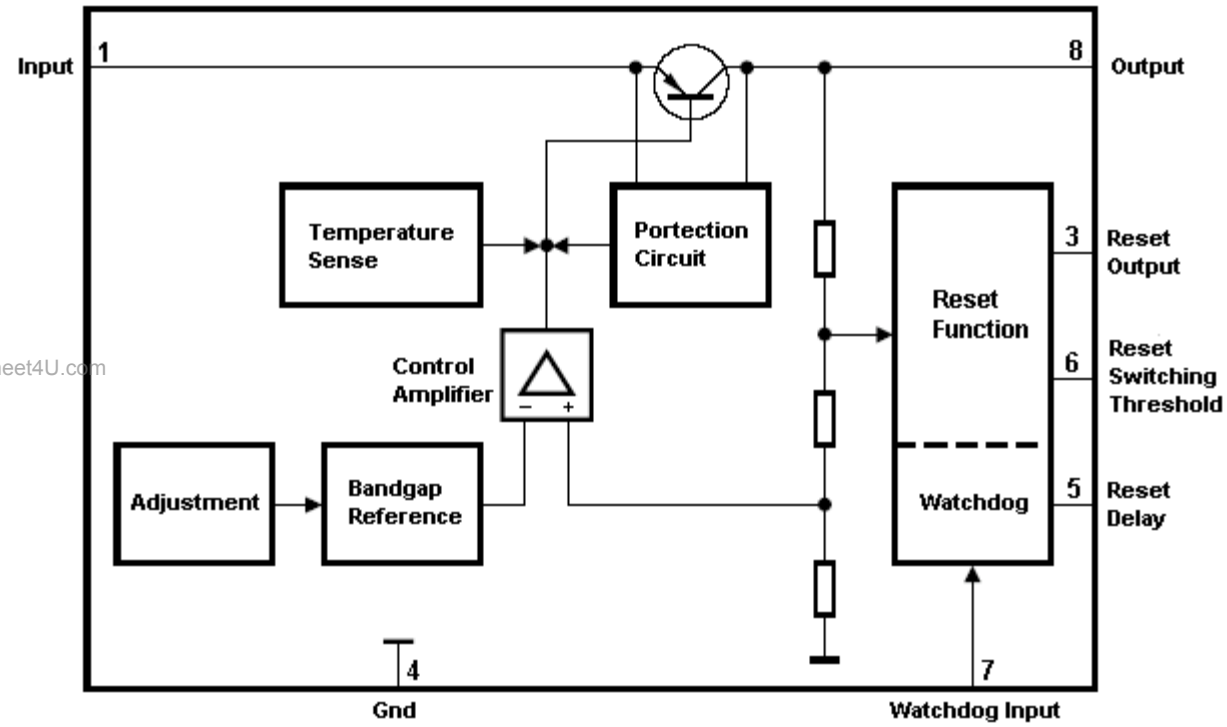
Pin Description

Pin No.	Symbol	Pin Description
1	IN	**Input Voltage.** block to ground directly with ceramic capacitor
2	N/C	Not Connected
3	RO	**Reset Output.** the open collector output is connected to the 5V output via an integrated resistor of 30kΩ
4	GND	**Ground**
5	RD	**Reset Delay.** connect a capacitor to ground for delay time adjustment.
6	RADJ	**Reset Switching Threshold.** for setting the switching threshold, output to ground with voltage divider. If this input is connected to ground, the reset is triggered at an output voltage of 4.5V.
7	WI	**Watchdog Input.** positive-edge-triggered input for monitoring a microcontroller.
8	OUT	**Output Voltage.** block to ground with 22uF capacitor, ESR <3Ω

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold V_{ST}, a reset signal is generated on the reset output and not cancelled again until the upper threshold voltage is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5V. A connected microcontroller is monitored by the watchdog logic. If pulses are missing, the rest output is set to low. The pulse sequence time can be set within a wide range with the reset delay capacitor. TS4268 is also incorporates a member of internal circuits for protection against:

- **Over load**
- **Over temperature**
- **Reverse polarity**



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Notes
Input					
Input voltage	Vin	-30	45	V	
Input current	Iin	Internally limited			
Reset Output					
Voltage	Vres	-0.3	7	V	
Current	Ires	Internally limited			
Reset Delay					
Voltage	V_{RD}	-0.3	7	V	
Current	I_{RD}	Internally limited			
Watchdog					
Watchdog input	Vwi	-0.3	7	V	
Reset Input					
Reset threshold	V_{RT}	-0.3	7	V	
Output					
Output voltage	Vout	-0.3	7	V	
Output current	Iout	Internally limited			
Ground					
Current	Iq	-100	50	mA	
Temperatures					
Junction temperature	Tj	-40	150	°C	
Storage temperature	Tstg	-50	150		

Operation Range

Parameter	Symbol	min.	max.	Unit	Notes
Input voltage	Vin	--	45	°C	
Junction temperature	Tj	-40	150		

Thermal Resistance

Parameter	Symbol	min.	max.	Unit	Notes
Junction to ambient (soldered)	Rθja	--	185	°C/W	(note 1)
Junction pin	Rθjp	--	72		(note 2)

1. Package mounted on PCB 80 x 80 x 1.5mm3, footprint only, zero airflow.
2. Measure to pin 2

Operation at up to the maximum junction temperature of 150°C is possible in principle. Note, however, operation at the maximum permitted rating could be affected the reliability of the device.

Electrical Characteristics

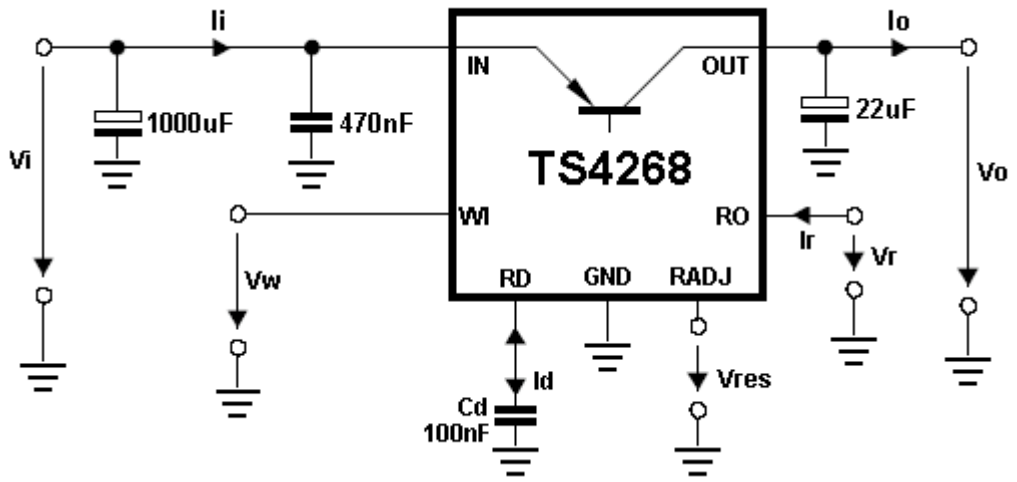
(Vin=13.5V, -40≤ Tj ≤125 °C, unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Output Voltage	5mA ≤ I_L ≤ 150mA, 6V ≤ Vin ≤ 28V	4.90	5.00	5.10	V
Current Limit	Vout= 0	180	250	--	mA
Quiescent Current	Iq= 0mA	--	300	400	uA
	Iq= 100mA	--	13	20	mA
Dropout Voltage (note 1)	I_L=150mA	--	250	500	mV
Line Regulation	6V≤ Vin ≤28V, I_L=150mA	--	10	30	mV
Load Regulation	5mA≤ I_L ≤150mA	--	10	30	mV
Reset Function					
Reset threshold		4.20	4.50	4.80	V
Reset adjust threshold		1.28	1.35	1.45	V
Reset low voltage	1mA external	--	0.20	0.50	V
Saturation voltage	Vout < V_{RT}	--	0.03	0.10	V
Charging current	V_{RD} < 1.0V	5	12	18	uA
Upper reset timing threshold		1.4	1.8	2.2	V
Reset delay time	C_{RD} = 100nF	10	15	25	mS
Reset reaction time	C_{RD} = 100nF	--	2	--	uS
Pull-up	With resp. to Vout	18	30	46	KΩ
Lower reset timing threshold		0.20	0.40	0.55	V
Watchdog Input					
Discharge current	V_{RD} < 1.0V	1.5	3.5	5.2	uA
Charging current	V_{RD} < 1.0V	5	12	18	uA
Upper timing threshold		1.4	1.8	2.2	V
Lower timing threshold		0.20	0.40	0.55	V
Watchdog periode	C_{RD} = 100nF	30	55	75	mS
Watchdog trigger time	C_{RD} = 100nF	25	40	60	mS
Activating current	Activates watchdog	2	8	15	mA
Slew rate	from 20% up to 80% Vout	5	--	--	V/us

Note 1: Drop voltage = Vin - Vout (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

Note 2: The reset output is low in range from Vout = 1V to Vout,rt.

Test Circuit



Reset Timing

The power-on reset delay time is defined by charging time of an external capacitor C_D which can be calculated as follow:

$$C_D = (\Delta t_{rd} \times I_{D,C}) / \Delta V$$

Definitions:

C_D = delay capacitor

Δt_{rd} = delay time

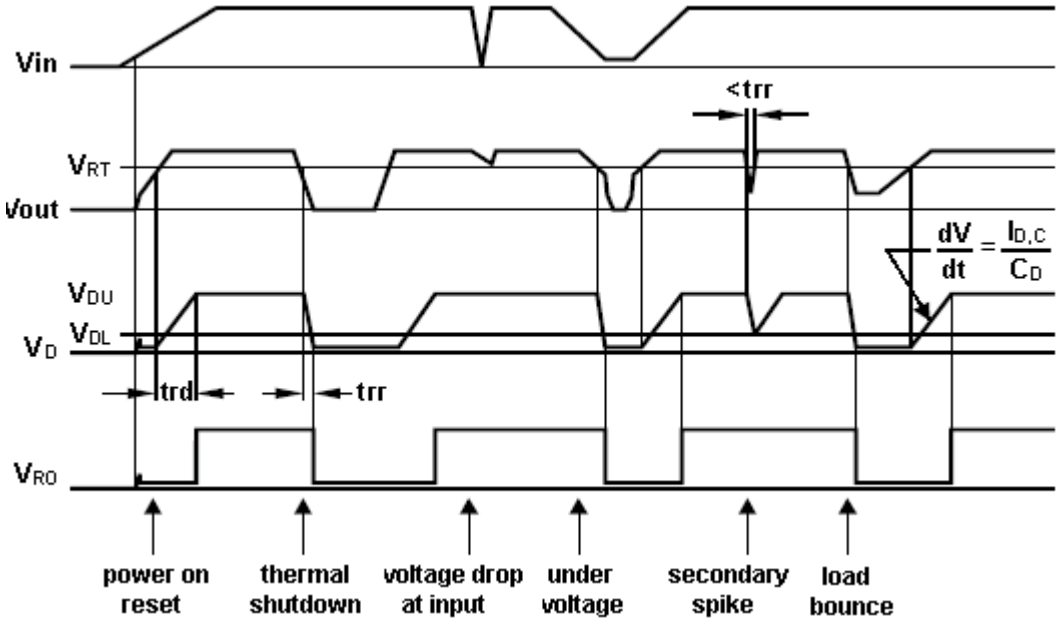
$I_{D,C}$ = charge current, typical 12uA

ΔV = V_{DU}, typical 1.8 V

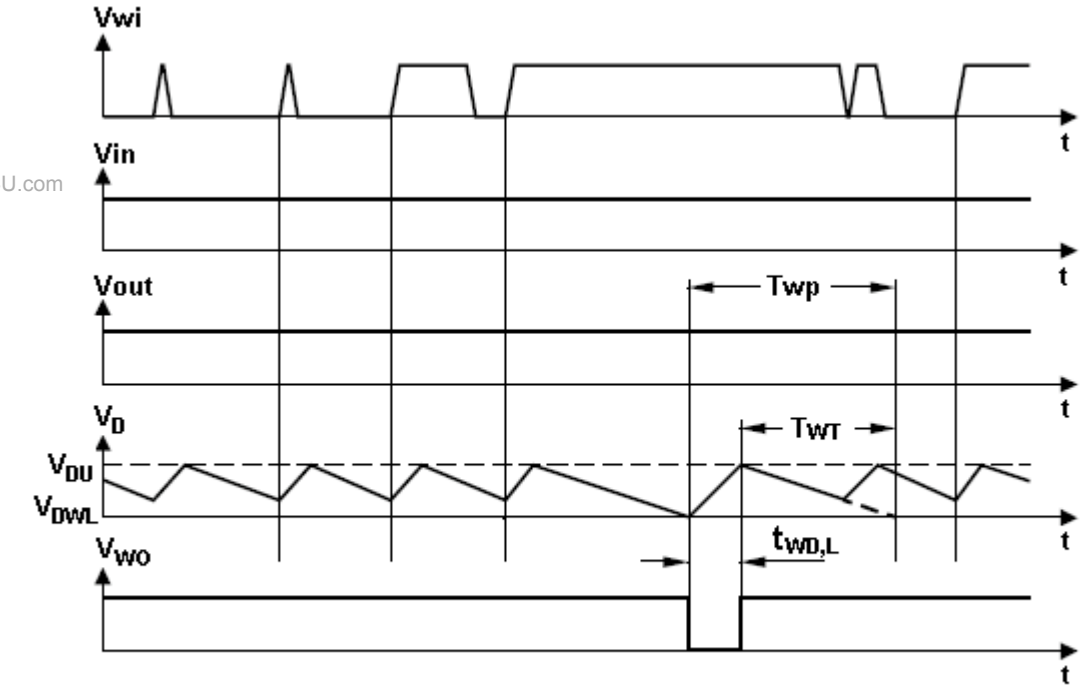
V_{DU} = upper delay switching threshold at C_D for reset delay time

The reset reaction time trr is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1uS for delay capacitor of 47nF. For other values for C_D the reaction time can be estimated using the following equation:

$$Trr \approx 20\ s/F \times C_D$$



Timing (Watchdog Disabled)



$$T_{WT} = \frac{(V_{DU} - V_{DWL})}{I_{D,d}} \; ; \; T_{wp} = \frac{(V_{DU} - V_{DWL})(I_{D,c} + I_{D,d})}{I_{D,c} * I_{D,d}} C_D \; ; \; t_{WD,L} = \frac{(V_{DU} - V_{DWL})}{I_{D,c}} C_D$$

Timing of the Watchdog Function

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