

100mW Stereo Headphone Amplifier

- Operating from **V_{cc}=2V to 5.5V**
- 100mW into 16Ω at 5V
- 38mW into 16Ω at 3.3V
- 11.5mW into 16Ω at 2V
- Switch ON/OFF click reduction circuitry
- High power supply rejection ratio: 85dB at 5V
- High signal-to-noise ratio: 110dB(A) at 5V
- High crosstalk immunity: 100dB (F=1kHz)
- Rail-to-rail input and output
- Unity-gain stable
- Available in **SO-8, MiniSO-8 & DFN8**

Description

The TS482 is a dual audio power amplifier able to drive a 16 or 32Ω stereo headset down to low voltages.

It is delivering up to 100mW per channel (into 16Ω loads) of continuous average power with 0.1% THD+N from a 5V power supply.

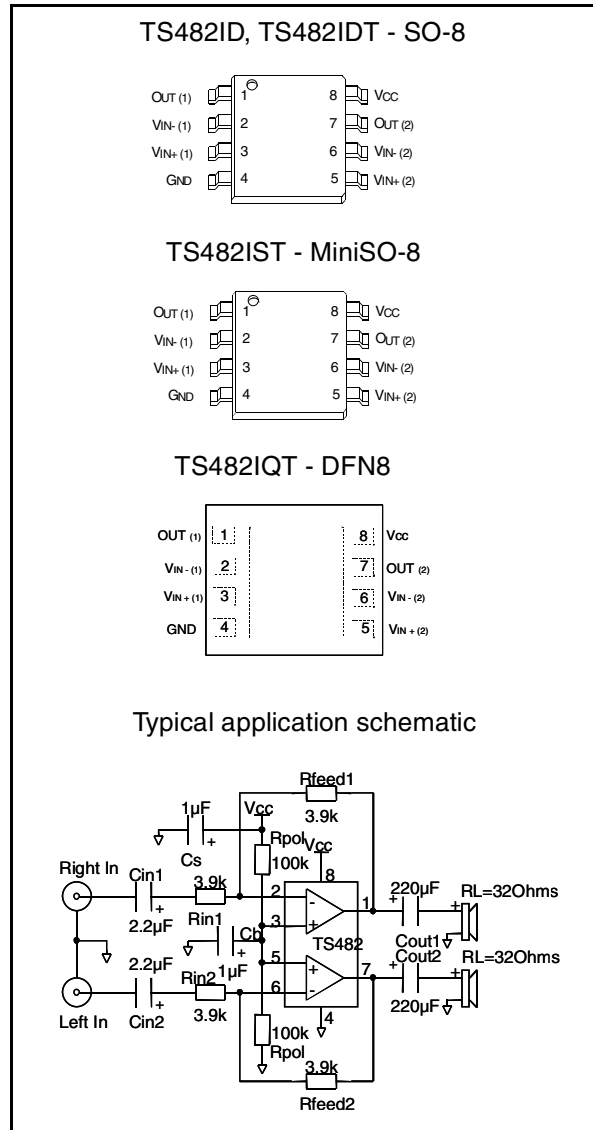
The unity gain stable TS482 can be configured by external gain-setting resistors.

Applications

- Stereo headphone amplifier
- Optical storage
- Computer motherboard
- PDA, organizers & notebook computers
- High-end TV, set-top box, DVD players
- Sound cards

Order Codes

| Part Number | Temperature Range | Package | Packing | Marking |
|-------------|-------------------|----------|---------------------|---------|
| TS482ID/IDT | -40, +85°C | SO-8 | Tube or Tape & Reel | 4821 |
| TS482IST | | miniSO-8 | Tape & Reel | |
| TS482IQT | | DFN8 | | |



1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-------------------|--|------------------------------|------|
| V _{CC} | Supply voltage ⁽¹⁾ | 6 | V |
| V _i | Input Voltage | -0.3 to V _{CC} +0.3 | V |
| T _{oper} | Operating Free Air Temperature Range | -40 to + 85 | °C |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _j | Maximum Junction Temperature | 150 | °C |
| R _{thja} | Thermal Resistance Junction to Ambient SO8 MiniSO8 DFN8 | 175 215 70 | °C/W |
| Pd | Power Dissipation ⁽²⁾ SO-8 MiniSO-8 DFN8 | 0.71 0.58 1.79 | W |
| ESD | Human Body Model (pin to pin) | 2 | kV |
| ESD | Machine Model - 220pF - 240pF (pin to pin) | 200 | V |
| Latch-up | Latch-up Immunity (all pins) | 200 | mA |
| | Lead Temperature (soldering, 10sec) | 250 | °C |
| | Lead Temperature (soldering, 10sec) for lead-free | 260 | °C |
| | Output Short-Circuit Duration | see note ⁽³⁾ | |

1. All voltages values are measured with respect to the ground pin.
2. Pd has been calculated with Tamb = 25°C, Tjunction = 150°C.
3. Attention must be paid to continuous power dissipation. Exposure of the IC to a short circuit on one or two amplifiers simultaneously can cause excessive heating and the destruction of the device.

Table 2. Operating conditions

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------------------|------|
| V _{CC} | Supply Voltage | 2 to 5.5 | V |
| R _L | Load Resistor | >= 16 | Ω |
| C _L | Load Capacitor R _L = 16 to 100Ω R _L > 100Ω | 400 100 | pF |
| V _{icm} | Common Mode Input Voltage Range | G _{ND} to V _{CC} | V |
| R _{thja} | Thermal Resistance Junction to Ambient SO-8 MiniSO-8 DFN8 ⁽¹⁾ | 150 190 41 | °C/W |

1. When mounted on a 4-layer PCB.

2 Electrical Characteristics

Table 3. Electrical characteristics when $V_{CC} = +5V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|--|-------------|---------------------------|--------------|------------|
| I_{CC} | Supply Current No input signal, no load | | 5.5 | 7.2 | mA |
| V_{IO} | Input Offset Voltage ($V_{ICM} = V_{CC}/2$) | | 1 | 5 | mV |
| I_{IB} | Input Bias Current ($V_{ICM} = V_{CC}/2$) | | 200 | 500 | nA |
| P_O | Output Power THD+N = 0.1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 0.1% Max, F = 1kHz, $R_L = 16\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 16\Omega$ | 60 95 | 65 67.5 100 107 | | mW |
| THD + N | Total Harmonic Distortion + Noise ($A_v=-1$) ⁽¹⁾ $R_L = 32\Omega$, $P_{out} = 60mW$, $20Hz \leq F \leq 20kHz$ $R_L = 16\Omega$, $P_{out} = 90mW$, $20Hz \leq F \leq 20kHz$ | | 0.03 0.03 | | % |
| PSRR | Power Supply Rejection Ratio ($A_v=1$), inputs floating F = 100Hz, Vripple = 100mVpp | | 85 | | dB |
| I_O | Max Output Current THD +N < 1%, $R_L = 16\Omega$ connected between out and $V_{CC}/2$ | 106 | 120 | | mA |
| V_O | Output Swing V_{OL} : $R_L = 32\Omega$ V_{OH} : $R_L = 32\Omega$ V_{OL} : $R_L = 16\Omega$ V_{OH} : $R_L = 16\Omega$ | 4.45 4.2 | 0.4 4.6 0.55 4.4 | 0.48 0.65 | V |
| SNR | Signal-to-Noise Ratio (Filter Type A, $A_v=-1$) $R_L = 32\Omega$, THD +N < 0.2%, $20Hz \leq F \leq 20kHz$ | 95 | 110 | | dB |
| Crosstalk | Channel Separation, $R_L = 32\Omega$ F = 1kHz F = 20Hz to 20kHz Channel Separation, $R_L = 16\Omega$ F = 1kHz F = 20Hz to 20kHz | | 100 80 100 80 | | dB |
| C_I | Input Capacitance | | 1 | | pF |
| GBP | Gain Bandwidth Product ($R_L = 32\Omega$) | 1.35 | 2.2 | | MHz |
| SR | Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$) | 0.45 | 0.7 | | V/ μ s |

1. Fig. 68 to 79 show dispersion of these parameters.

Table 4. Electrical characteristics when $V_{CC} = +3.3V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified) ⁽¹⁾

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|--|--------------|--------------------------|--------------|------------|
| I_{CC} | Supply Current No input signal, no load | | 5.3 | 7.2 | mA |
| V_{IO} | Input Offset Voltage ($V_{ICM} = V_{CC}/2$) | | 1 | 5 | mV |
| I_{IB} | Input Bias Current ($V_{ICM} = V_{CC}/2$) | | 200 | 500 | nA |
| P_O | Output Power THD+N = 0.1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 0.1% Max, F = 1kHz, $R_L = 16\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 16\Omega$ | 23 | 27 28 38 42 | | mW |
| THD + N | Total Harmonic Distortion + Noise ($A_v=-1$) ⁽¹⁾ $R_L = 32\Omega$, $P_{out} = 16mW$, $20Hz \leq F \leq 20kHz$ $R_L = 16\Omega$, $P_{out} = 35mW$, $20Hz \leq F \leq 20kHz$ | | 0.03 0.03 | | % |
| PSRR | Power Supply Rejection Ratio ($A_v=1$), inputs floating F = 100Hz, Vripple = 100mVpp | | 80 | | dB |
| I_O | Max Output Current THD +N < 1%, $R_L = 16\Omega$ connected between out and $V_{CC}/2$ | 64 | 75 | | mA |
| V_O | Output Swing V_{OL} : $R_L = 32\Omega$ V_{OH} : $R_L = 32\Omega$ V_{OL} : $R_L = 16\Omega$ V_{OH} : $R_L = 16\Omega$ | 2.85 2.68 | 0.3 3 0.45 2.85 | 0.38 0.52 | V |
| SNR | Signal-to-Noise Ratio (Filter Type A, $A_v=-1$) $R_L = 32\Omega$, THD +N < 0.2%, $20Hz \leq F \leq 20kHz$ | 92 | 107 | | dB |
| Crosstalk | Channel Separation, $R_L = 32\Omega$ F = 1kHz F = 20Hz to 20kHz Channel Separation, $R_L = 16\Omega$ F = 1kHz F = 20Hz to 20kHz | | 100 80 100 80 | | dB |
| C_I | Input Capacitance | | 1 | | pF |
| GBP | Gain Bandwidth Product ($R_L = 32\Omega$) | 1.2 | 2 | | MHz |
| SR | Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$) | 0.45 | 0.7 | | V/ μ s |

1. Fig. 68 to 79 show dispersion of these parameters.

1. All electrical values are guaranteed with correlation measurements at 2V and 5V.

Table 5. Electrical characteristics when $V_{CC} = +2.5V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)⁽²⁾

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|--|--------------|------------------------------|---------------|------------|
| I_{CC} | Supply Current No input signal, no load | | 5.1 | 7.2 | mA |
| V_{IO} | Input Offset Voltage ($V_{ICM} = V_{CC}/2$) | | 1 | 5 | mV |
| I_{IB} | Input Bias Current ($V_{ICM} = V_{CC}/2$) | | 200 | 500 | nA |
| P_O | Output Power THD+N = 0.1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 0.1% Max, F = 1kHz, $R_L = 16\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 16\Omega$ | 12.5 17.5 | 13.5 14.5 20.5 22 | | mW |
| THD + N | Total Harmonic Distortion + Noise ($A_V = -1$) ⁽¹⁾ $R_L = 32\Omega$, $P_{out} = 10mW$, $20Hz \leq F \leq 20kHz$ $R_L = 16\Omega$, $P_{out} = 16mW$, $20Hz \leq F \leq 20kHz$ | | 0.03 0.03 | | % |
| PSRR | Power Supply Rejection Ratio ($A_V = 1$), inputs floating F = 100Hz, Vripple = 100mVpp | | 75 | | dB |
| I_O | Max Output Current THD + N < 1%, $R_L = 16\Omega$ connected between out and $V_{CC}/2$ | 45 | 56 | | mA |
| V_O | Output Swing V_{OL} : $R_L = 32\Omega$ V_{OH} : $R_L = 32\Omega$ V_{OL} : $R_L = 16\Omega$ V_{OH} : $R_L = 16\Omega$ | 2.14 1.97 | 0.25 2.25 0.35 2.15 | 0.325 0.45 | V |
| SNR | Signal-to-Noise Ratio (Filter Type A, $A_V = -1$) $R_L = 32\Omega$, THD + N < 0.2%, $20Hz \leq F \leq 20kHz$ | 89 | 102 | | dB |
| Crosstalk | Channel Separation, $R_L = 32\Omega$ F = 1kHz F = 20Hz to 20kHz Channel Separation, $R_L = 16\Omega$ F = 1kHz F = 20Hz to 20kHz | | 100 80 100 80 | | dB |
| C_I | Input Capacitance | | 1 | | pF |
| GBP | Gain Bandwidth Product ($R_L = 32\Omega$) | 1.2 | 2 | | MHz |
| SR | Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$) | 0.45 | 0.7 | | V/ μ s |

1. Fig. 68 to 79 show dispersion of these parameters.

2. All electrical values are guaranteed with correlation measurements at 2V and 5V.

Table 6. Electrical characteristics when $V_{CC} = +2V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------|--|--------------|------------------------------|---------------|------------|
| I_{CC} | Supply Current No input signal, no load | | 5 | 7.2 | mA |
| V_{IO} | Input Offset Voltage ($V_{ICM} = V_{CC}/2$) | | 1 | 5 | mV |
| I_{IB} | Input Bias Current ($V_{ICM} = V_{CC}/2$) | | 200 | 500 | nA |
| P_O | Output Power THD+N = 0.1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 32\Omega$ THD+N = 0.1% Max, F = 1kHz, $R_L = 16\Omega$ THD+N = 1% Max, F = 1kHz, $R_L = 16\Omega$ | 7 9.5 | 8 9 11.5 13 | | mW |
| THD + N | Total Harmonic Distortion + Noise ($A_v=-1$) ⁽¹⁾ $R_L = 32\Omega$, $P_{out} = 6.5mW$, $20Hz \leq F \leq 20kHz$ $R_L = 16\Omega$, $P_{out} = 8mW$, $20Hz \leq F \leq 20kHz$ | | 0.02 0.025 | | % |
| PSRR | Power Supply Rejection Ratio ($A_v=1$), inputs floating F = 100Hz, Vripple = 100mVpp | | 75 | | dB |
| I_O | Max Output Current THD +N < 1%, $R_L = 16\Omega$ connected between out and $V_{CC}/2$ | 33 | 41.5 | | mA |
| V_O | Output Swing V_{OL} : $R_L = 32\Omega$ V_{OH} : $R_L = 32\Omega$ V_{OL} : $R_L = 16\Omega$ V_{OH} : $R_L = 16\Omega$ | 1.67 1.53 | 0.24 1.73 0.33 1.63 | 0.295 0.41 | V |
| SNR | Signal-to-Noise Ratio (Filter Type A, $A_v=-1$) $R_L = 32\Omega$, THD +N < 0.2%, $20Hz \leq F \leq 20kHz$ | 88 | 101 | | dB |
| Crosstalk | Channel Separation, $R_L = 32\Omega$ F = 1kHz F = 20Hz to 20kHz Channel Separation, $R_L = 16\Omega$ F = 1kHz F = 20Hz to 20kHz | | 100 80 100 80 | | dB |
| C_I | Input Capacitance | | 1 | | pF |
| GBP | Gain Bandwidth Product ($R_L = 32\Omega$) | 1.2 | 2 | | MHz |
| SR | Slew Rate, Unity Gain Inverting ($R_L = 16\Omega$) | 0.42 | 0.65 | | V/ μ s |

1. Fig. 68 to 79 show dispersion of these parameters.

Table 7. Components description

| Components | Functional Description |
|------------|---|
| Rin | Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin ($f_c = 1 / (2 \times \pi \times R_{in} \times C_{in})$) |
| Cin | Input coupling capacitor which blocks the DC voltage at the amplifier input terminal |
| Rfeed | Feed back resistor which sets the closed loop gain in conjunction with Rin |
| Cs | Supply Bypass capacitor which provides power supply filtering |
| Cb | Bypass capacitor which provides half supply filtering |
| Cout | Output coupling capacitor which blocks the DC voltage at the load input terminal This capacitor also forms a high pass filter with RL ($f_c = 1 / (2 \times \pi \times R_L \times C_{out})$) |
| Rpol | These 2 resistors form a voltage divider which provide a DC biasing voltage ($V_{cc}/2$) for the 2 amplifiers. |
| Av | Closed loop gain = $-R_{feed} / R_{in}$ |

Table 8. Index of graphics

| Description | Figure | Page |
|--|------------------------|----------------------|
| <i>Open loop gain and phase vs. frequency response</i> | <i>Figure 1 to 10</i> | <i>Page 9 to 10</i> |
| <i>Phase and Gain Margin vs. Power Supply Voltage</i> | <i>Figure 11 to 20</i> | <i>Page 10 to 12</i> |
| <i>Output power vs. power supply voltage</i> | <i>Figure 21 to 23</i> | <i>Page 12</i> |
| <i>Output power vs. load resistance</i> | <i>Figure 24 to 27</i> | <i>Page 12 to 13</i> |
| <i>Power dissipation vs. output power</i> | <i>Figure 28 to 31</i> | <i>Page 13 to 14</i> |
| <i>Power derating vs. ambient temperature</i> | <i>Figure 32</i> | <i>Page 14</i> |
| <i>Current consumption vs. power supply voltage</i> | <i>Figure 33</i> | <i>Page 14</i> |
| <i>Power supply rejection ratio vs. frequency</i> | <i>Figure 34</i> | <i>Page 14</i> |
| <i>THD + N vs. output power</i> | <i>Figure 35 to 49</i> | <i>Page 14 to 17</i> |
| <i>THD + N vs. frequency</i> | <i>Figure 50 to 54</i> | <i>Page 17</i> |
| <i>Signal to noise ratio</i> | <i>Figure 55 to 58</i> | <i>Page 18</i> |
| <i>Equivalent input noise voltage vs. frequency</i> | <i>Figure 59</i> | <i>Page 18</i> |
| <i>Output voltage swing vs. power supply</i> | <i>Figure 60</i> | <i>Page 18</i> |
| <i>Crosstalk vs. frequency</i> | <i>Figure 61 to 65</i> | <i>Page 19</i> |
| <i>Lower cut off frequency vs. output capacitor</i> | <i>Figure 66</i> | <i>Page 19</i> |
| <i>Lower cut off frequency vs. input capacitor</i> | <i>Figure 67</i> | <i>Page 20</i> |
| <i>Typical distribution of TDH + N</i> | <i>Figure 68 to 79</i> | <i>Page 20 to 22</i> |

Figure 1. Open loop gain and phase vs. frequency response

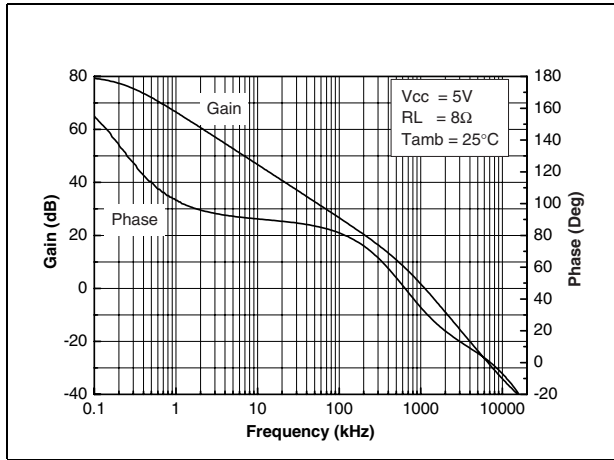


Figure 2. Open loop gain and phase vs. frequency response

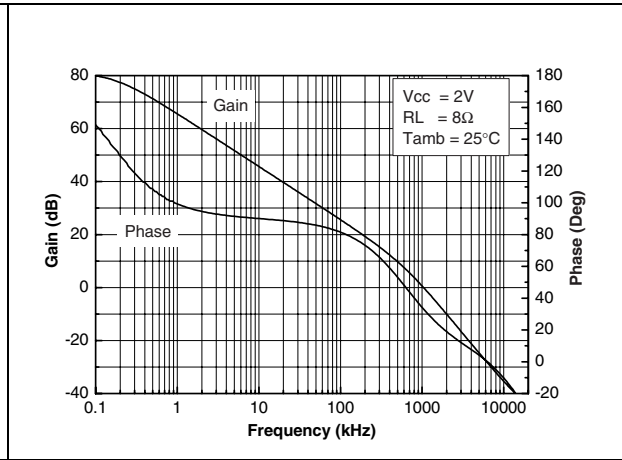


Figure 3. Open loop gain and phase vs. frequency response

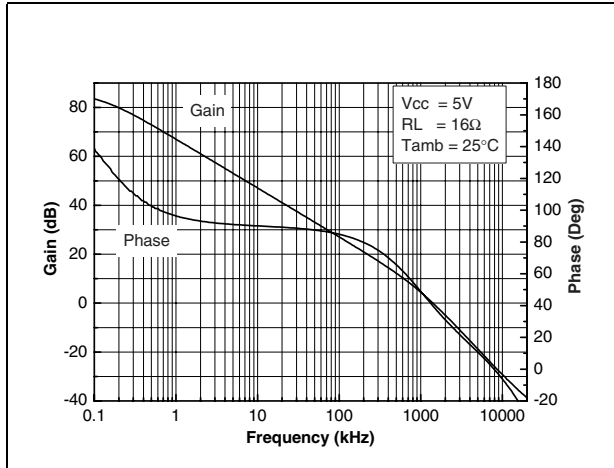


Figure 4. Open loop gain and phase vs. frequency response

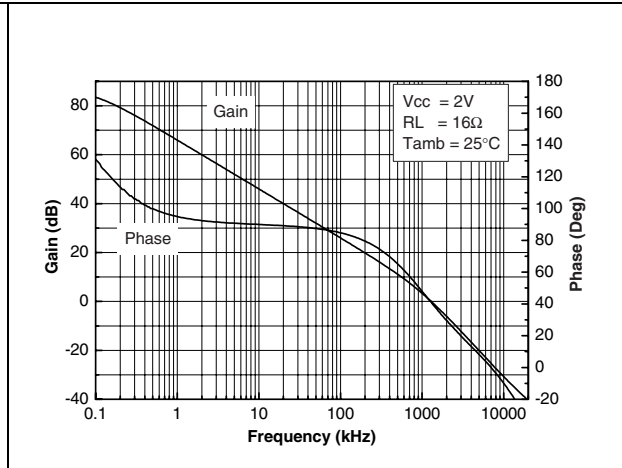


Figure 5. Open loop gain and phase vs. frequency response

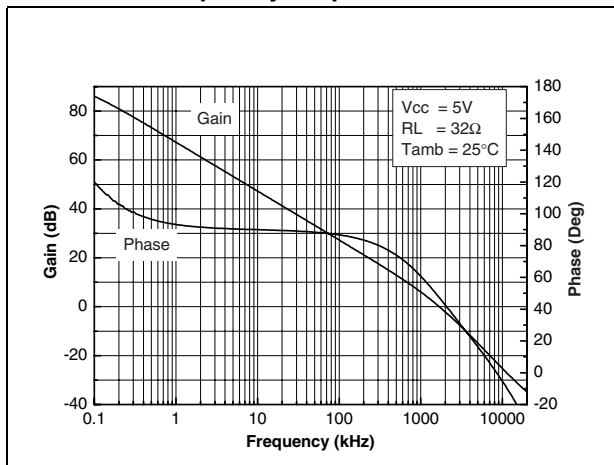


Figure 6. Open loop gain and phase vs. frequency response

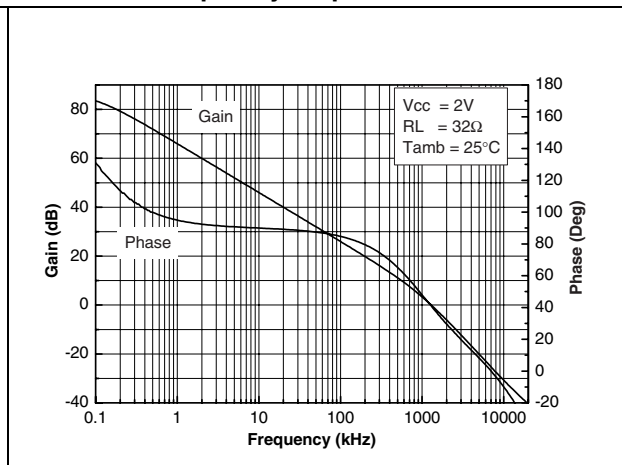


Figure 7. Open loop gain and phase vs. frequency response

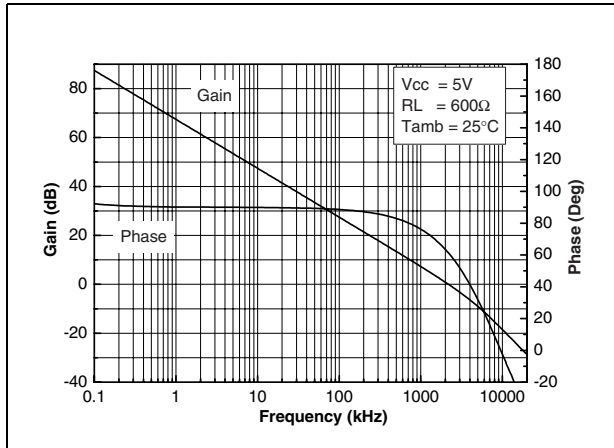


Figure 8. Open loop gain and phase vs. frequency response

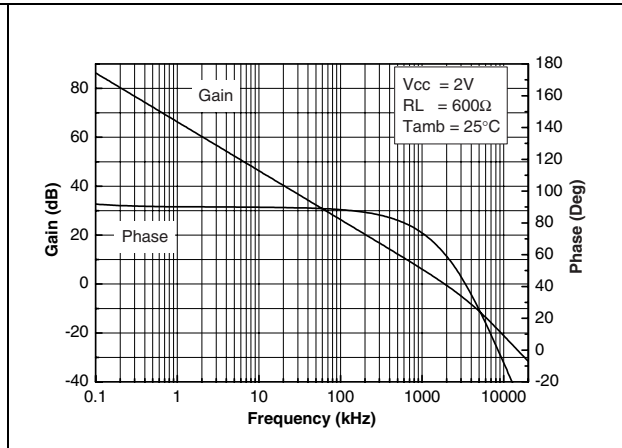


Figure 9. Open loop gain and phase vs. frequency response

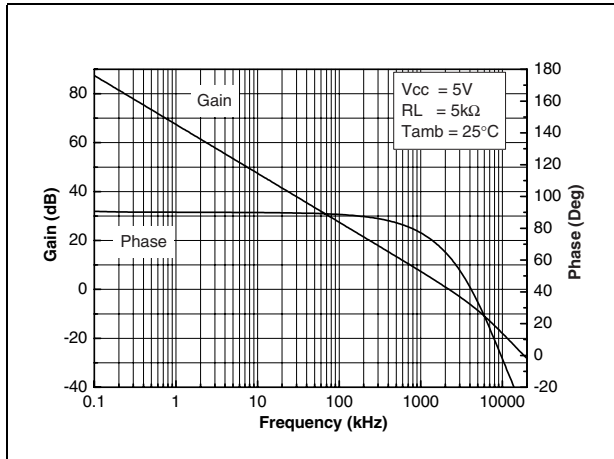


Figure 10. Open loop gain and phase vs. frequency response

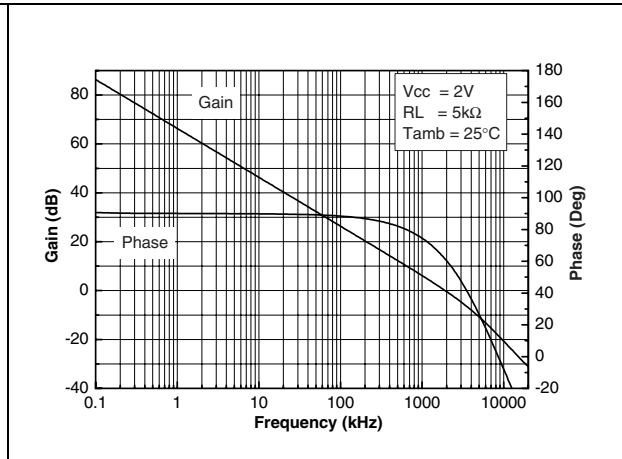


Figure 11. Phase margin vs. power supply voltage

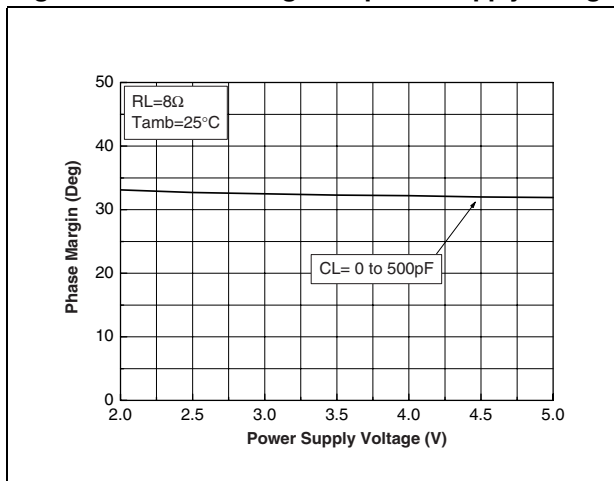


Figure 12. Gain margin vs. power supply voltage

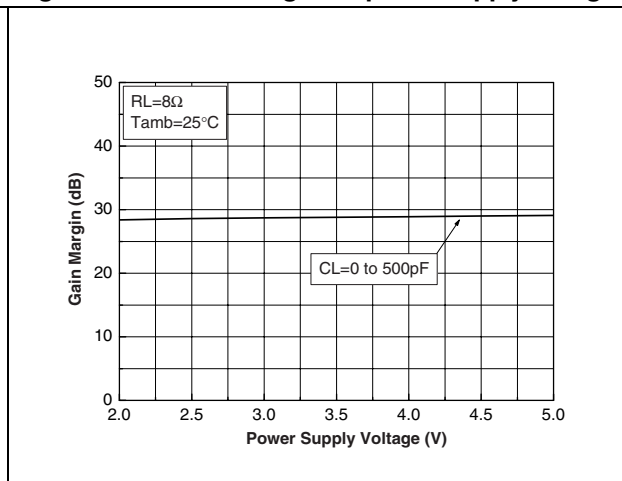


Figure 13. Phase margin vs. power supply voltage Figure 14. Gain margin vs. power supply voltage

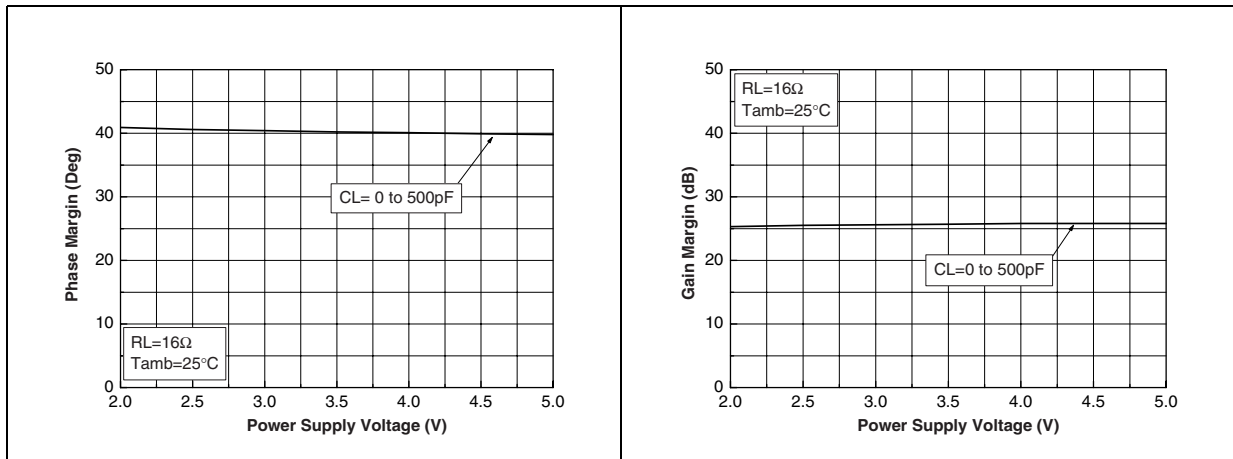


Figure 15. Phase margin vs. power supply voltage Figure 16. Gain margin vs. power supply voltage

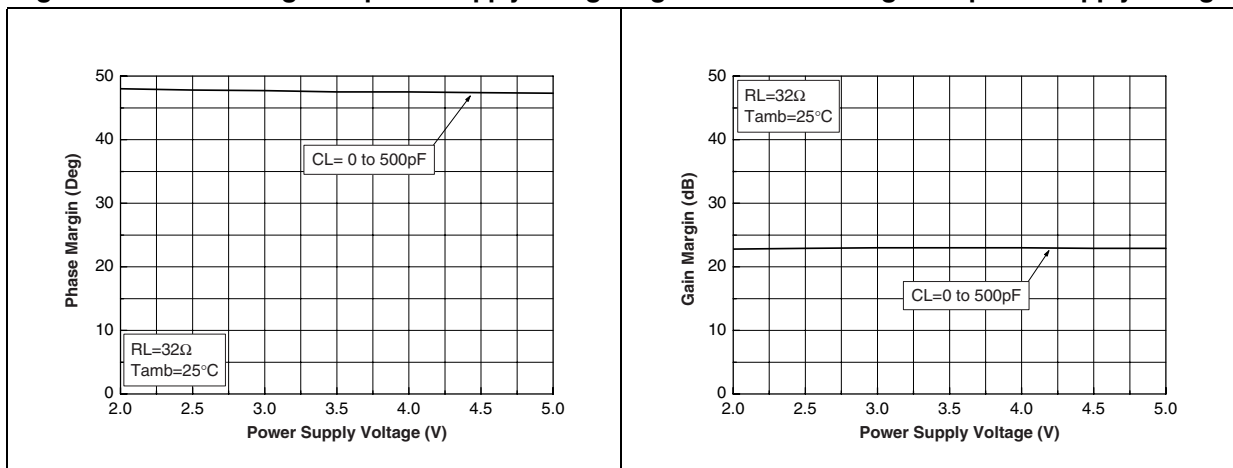


Figure 17. Phase margin vs. power supply voltage Figure 18. Gain margin vs. power supply voltage

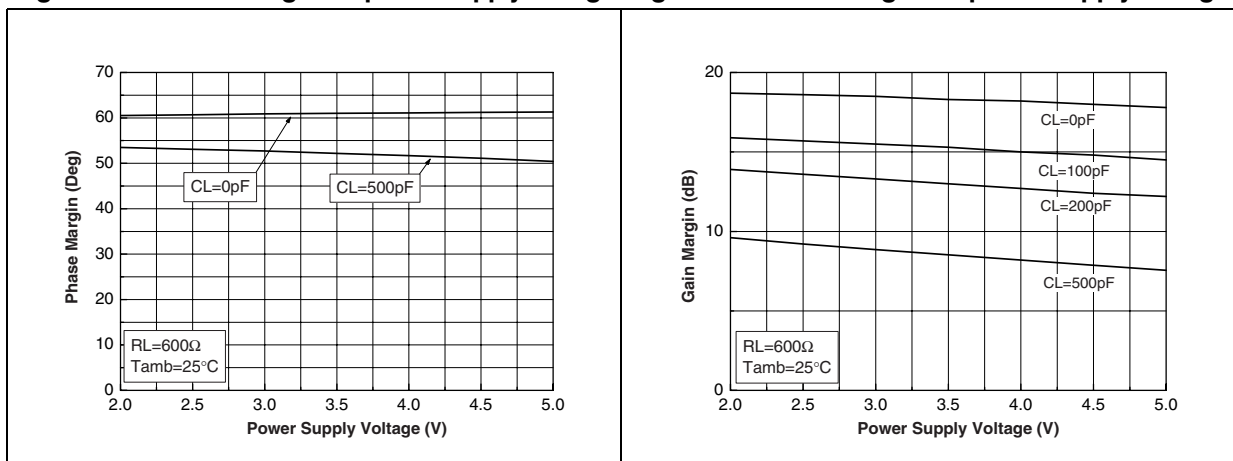


Figure 19. Phase margin vs. power supply voltage Figure 20. Gain margin vs. power supply voltage

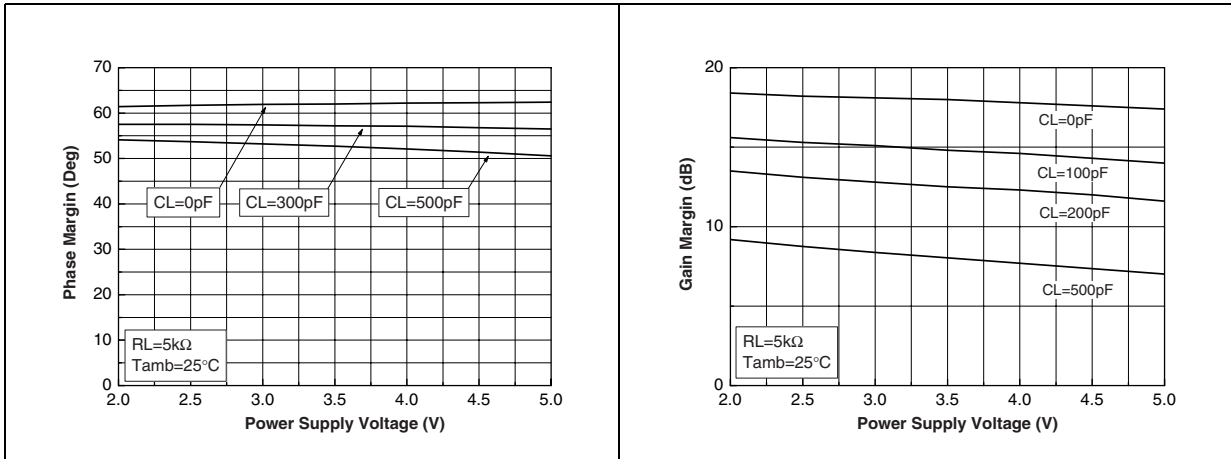


Figure 21. Output power vs. power supply voltage Figure 22. Output power vs. power supply voltage

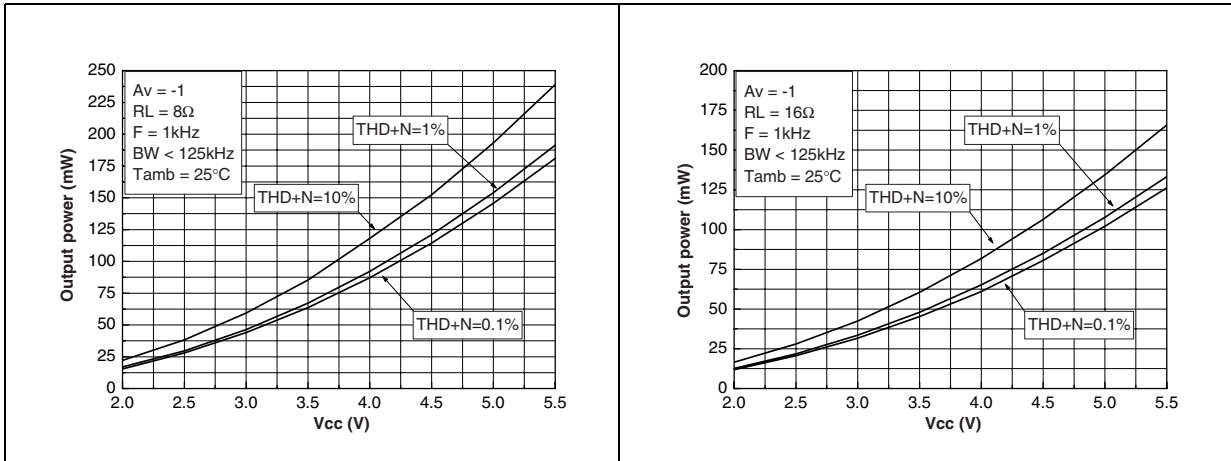


Figure 23. Output power vs. power supply voltage Figure 24. Output power vs. load resistance

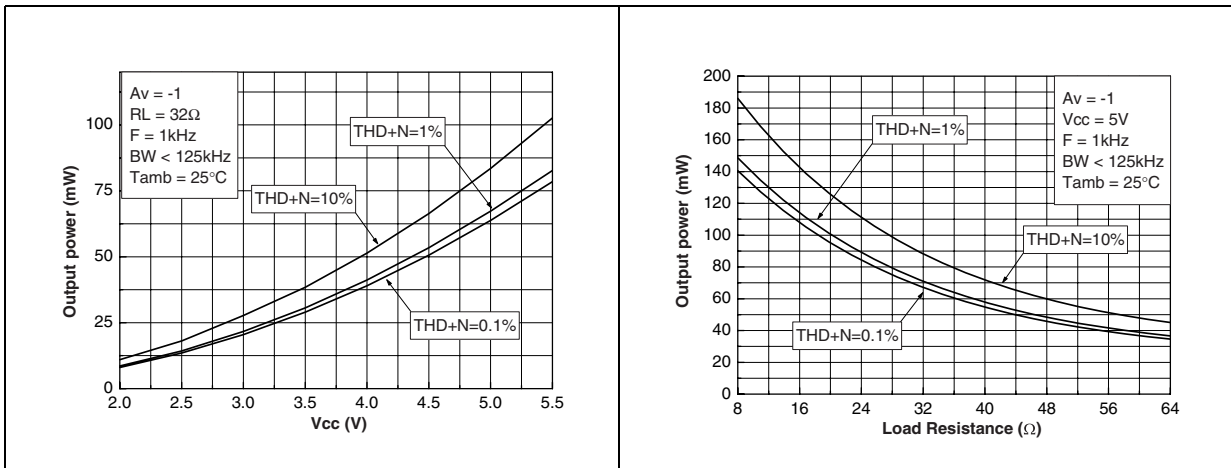


Figure 25. Output power vs. load resistance

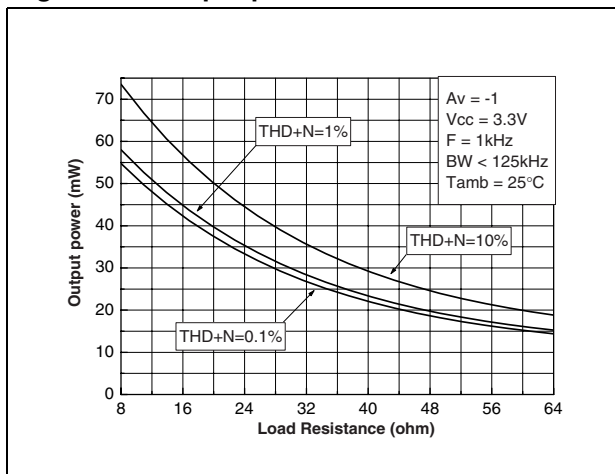


Figure 26. Output power vs. load resistance

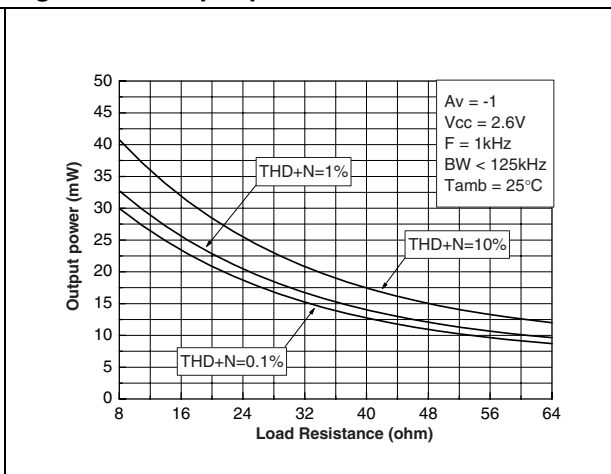


Figure 27. Output power vs. load resistance

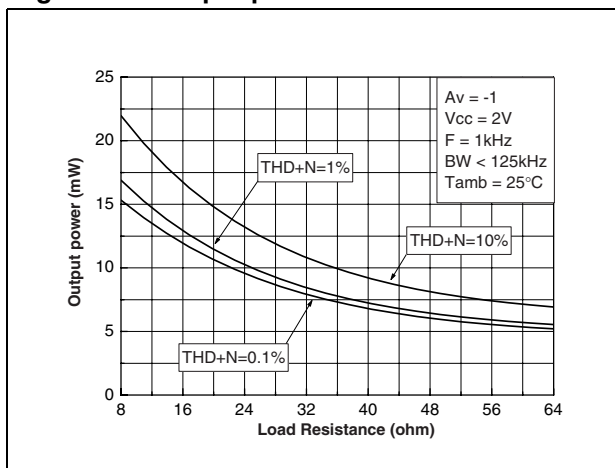


Figure 28. Power dissipation vs. output power

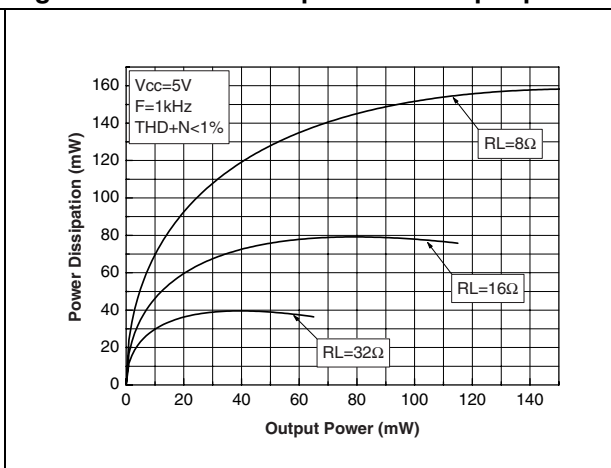


Figure 29. Power dissipation vs. output power

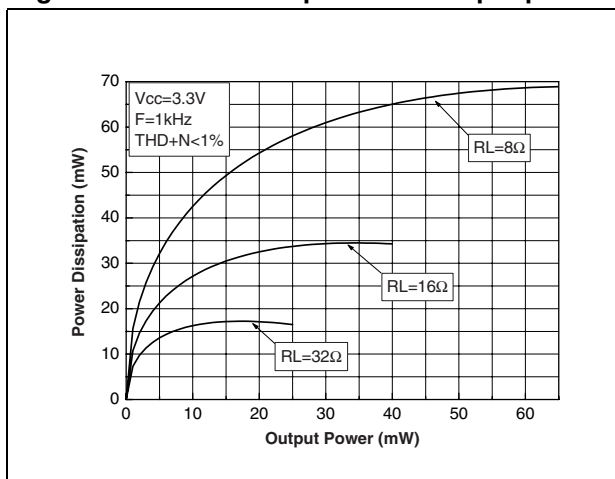


Figure 30. Power dissipation vs. output power

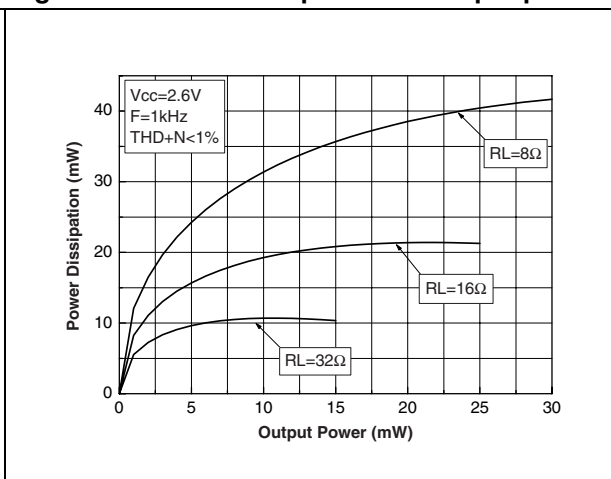


Figure 31. Power dissipation vs. output power Figure 32. Power derating vs. ambient temperature

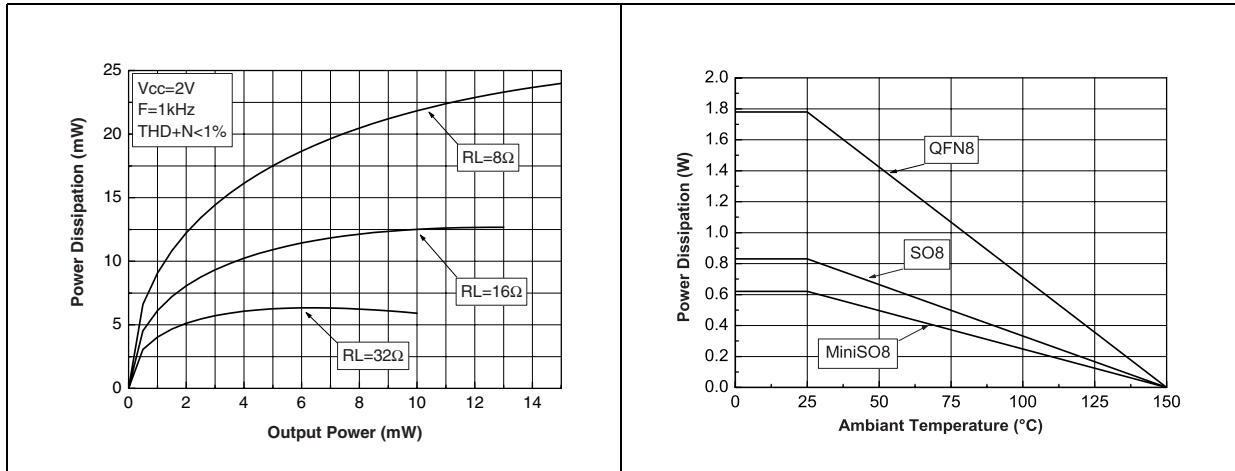


Figure 33. Current consumption vs. power supply voltage Figure 34. Power supply rejection ratio vs. frequency

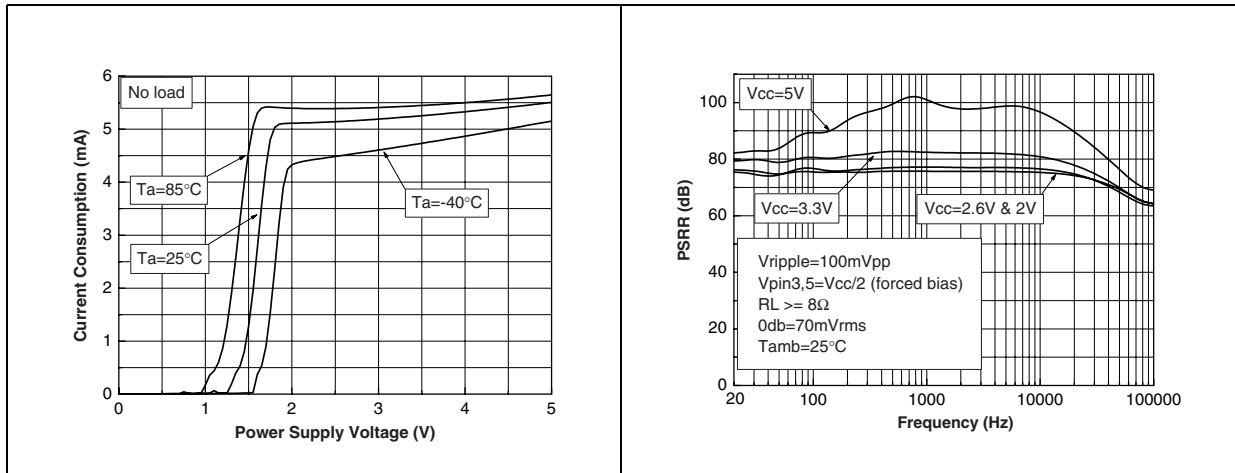


Figure 35. THD + N vs. output power Figure 36. THD + N vs. output power

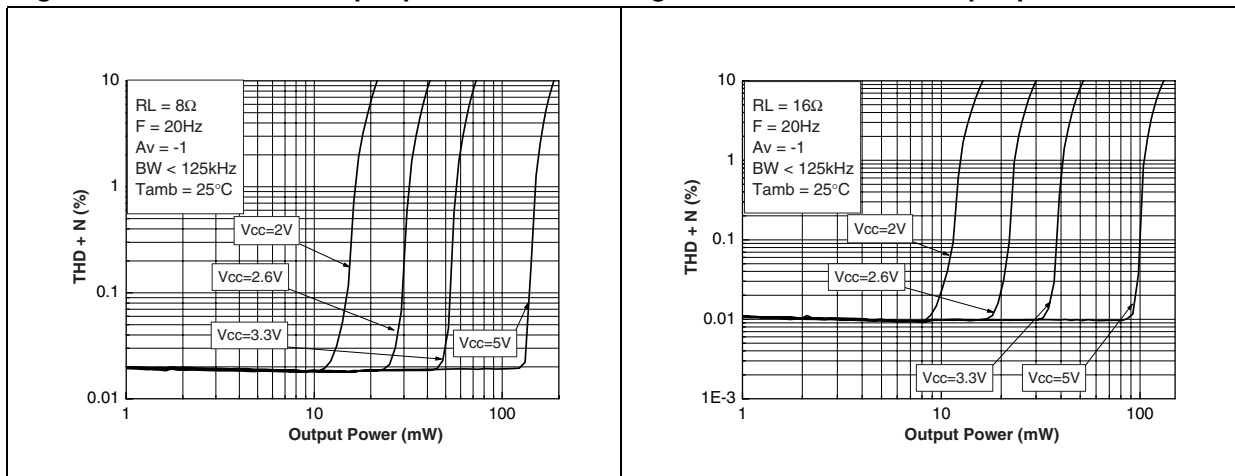


Figure 37. THD + N vs. output power

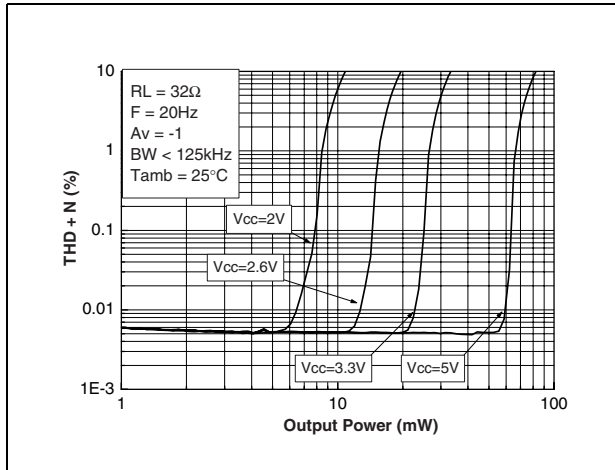


Figure 38. THD + N vs. output power

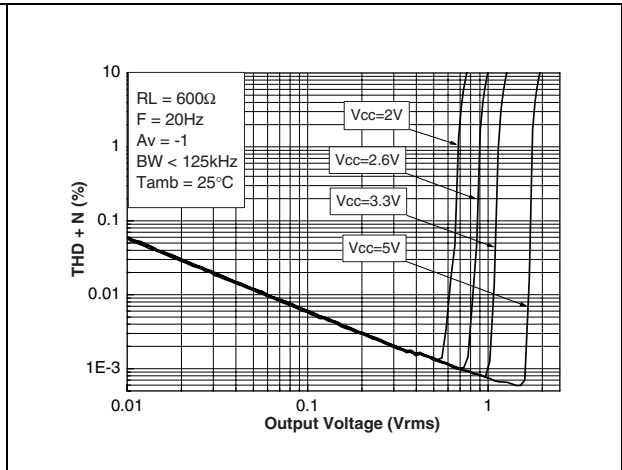


Figure 39. THD + N vs. output power

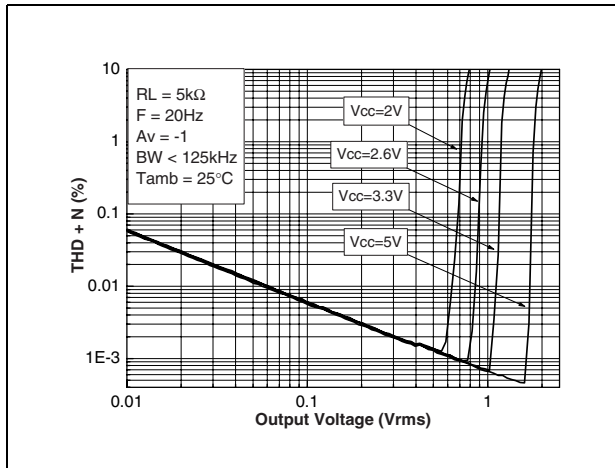


Figure 40. THD + N vs. output power

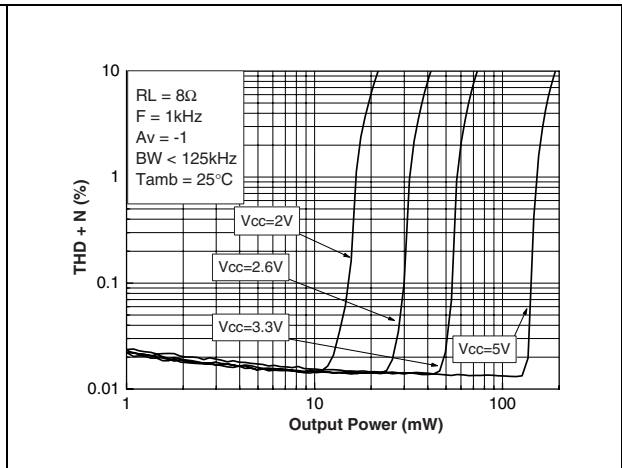


Figure 41. THD + N vs. output power

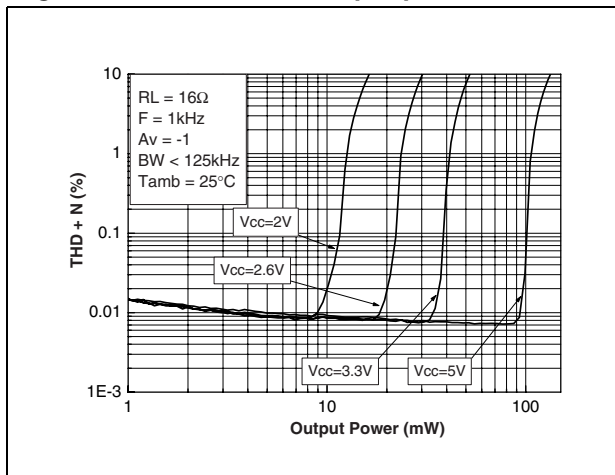


Figure 42. THD + N vs. output power

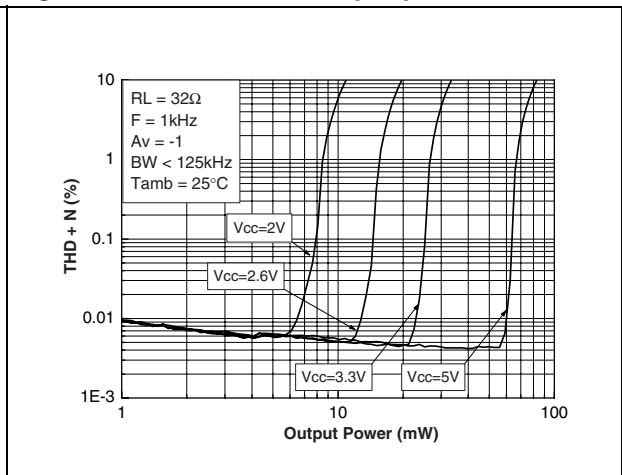


Figure 43. THD + N vs. output power

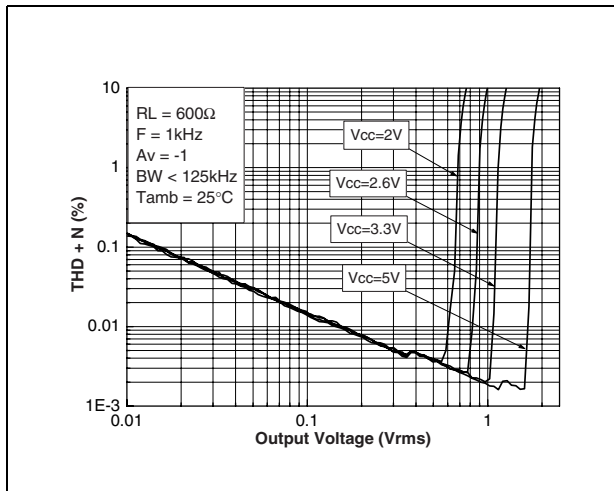


Figure 44. THD + N vs. output power

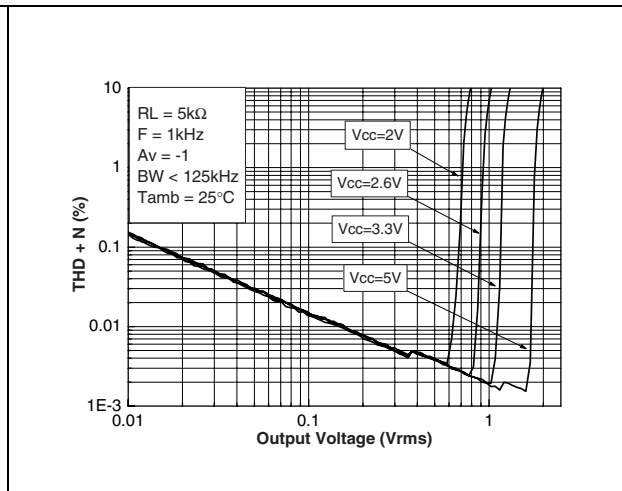


Figure 45. THD + N vs. output power

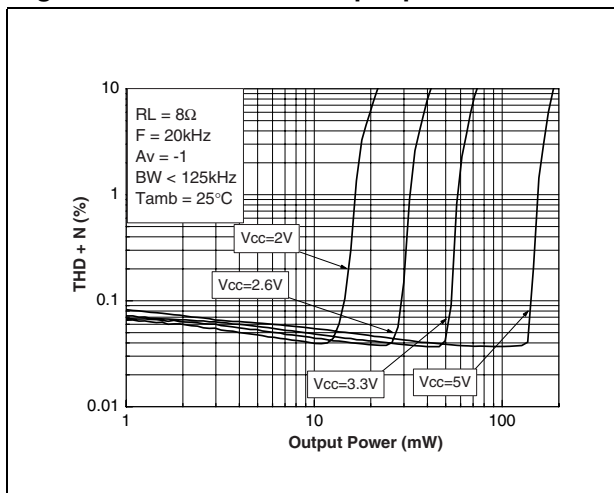


Figure 46. THD + N vs. output power

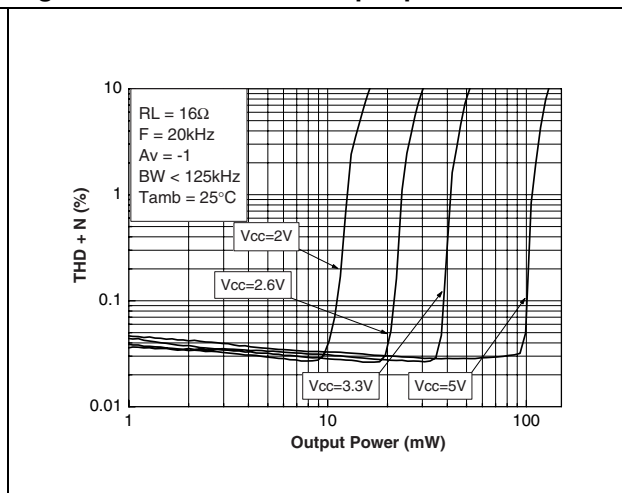


Figure 47. THD + N vs. output power

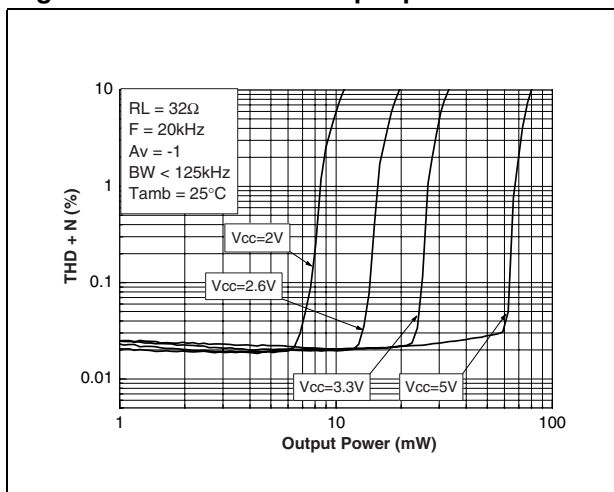


Figure 48. THD + N vs. output power

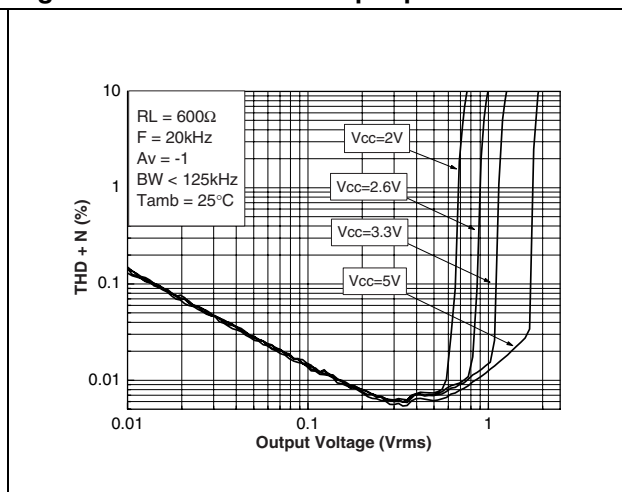


Figure 49. THD + N vs. output power

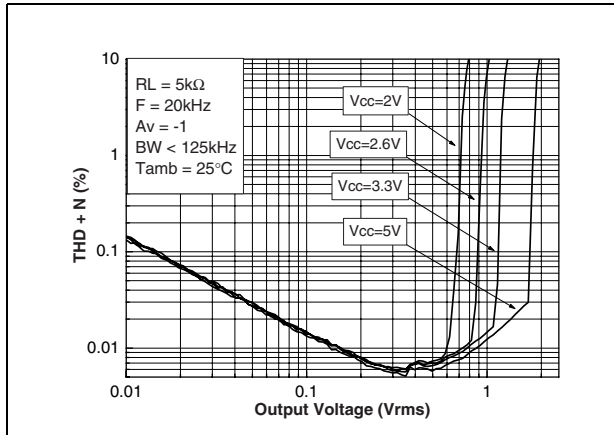


Figure 50. THD + N vs. frequency

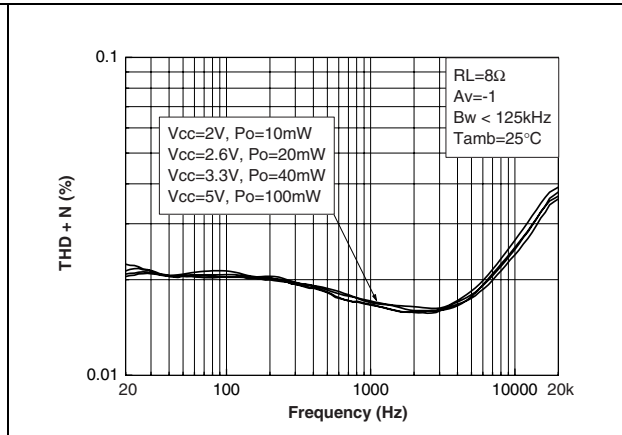


Figure 51. THD + N vs. frequency

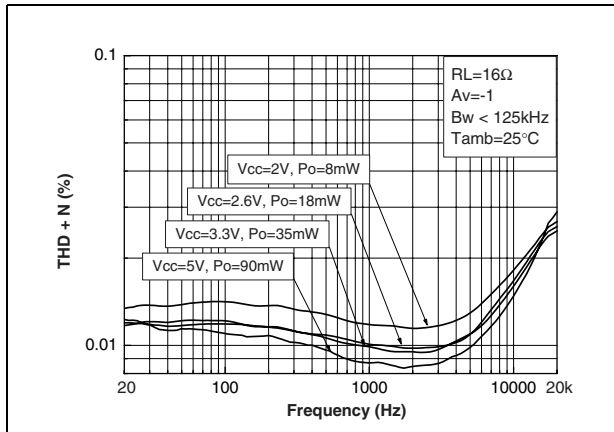


Figure 52. THD + N vs. frequency

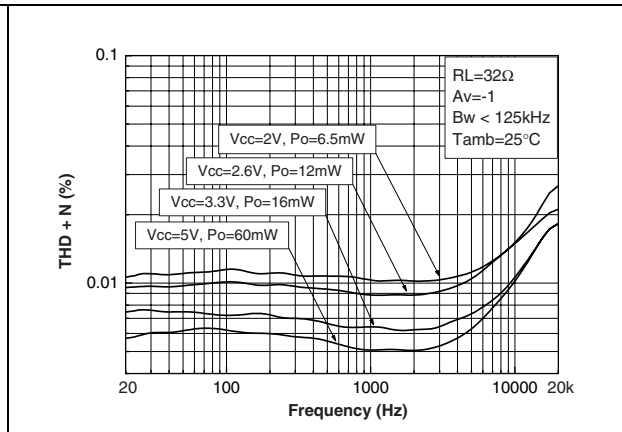


Figure 53. THD + N vs. frequency

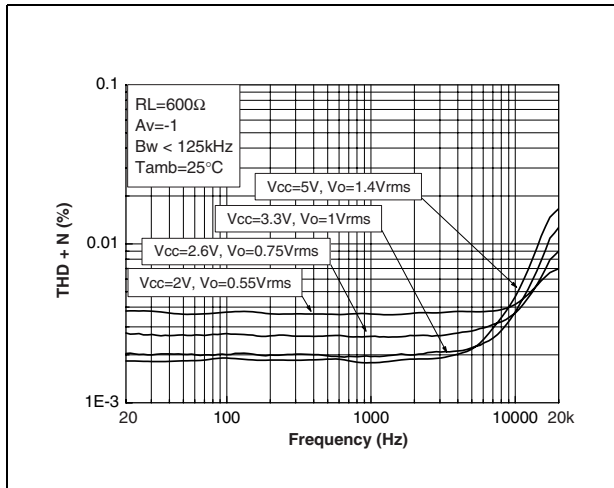


Figure 54. THD + N vs. frequency

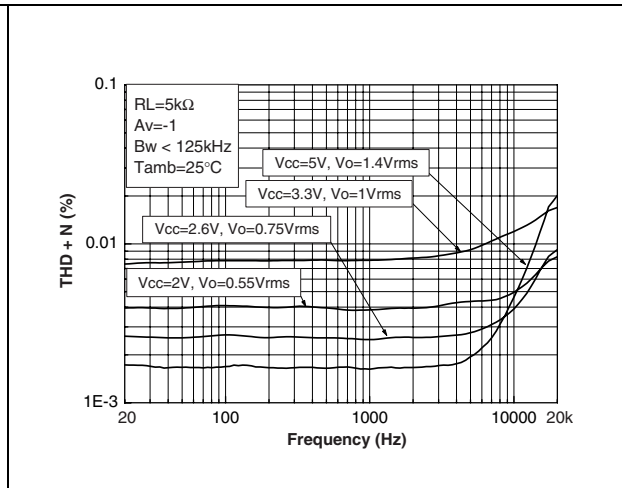


Figure 55. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

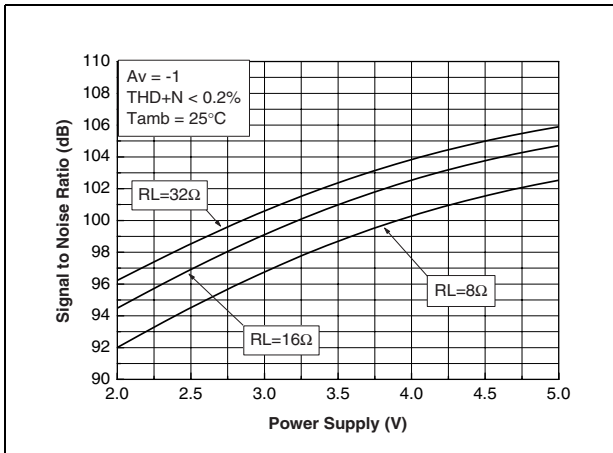


Figure 56. Signal to noise ratio vs. power supply with unweighted filter (20Hz to 20kHz)

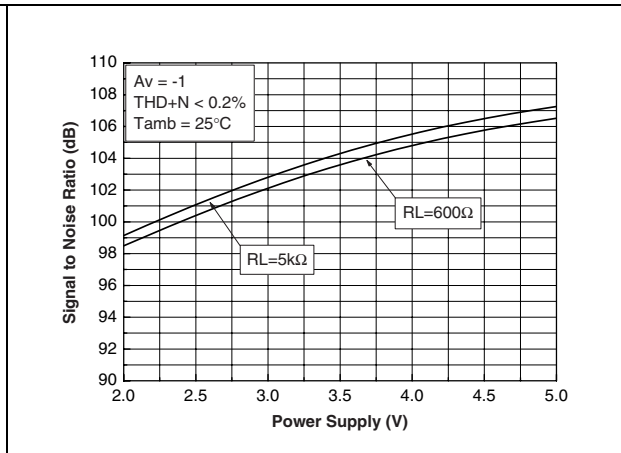


Figure 57. Signal to noise ratio vs. power supply with A weighted filter

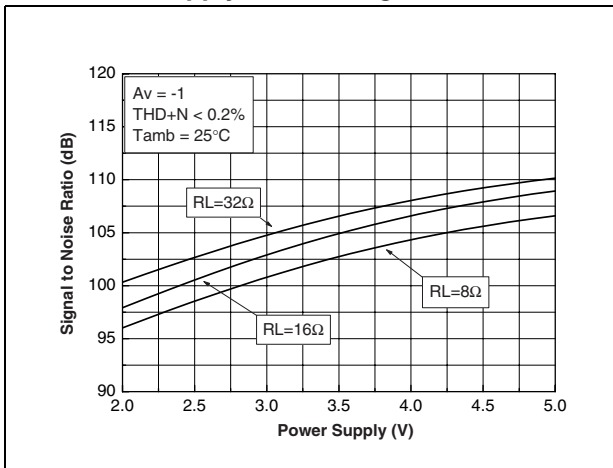


Figure 58. Signal to noise ratio vs. power supply with A weighted filter

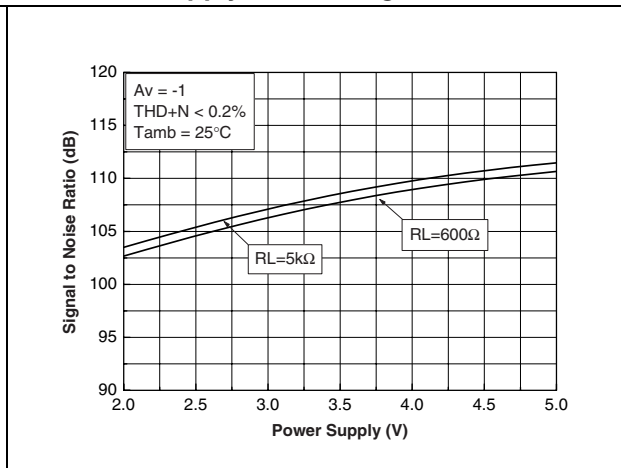


Figure 59. Equivalent input noise voltage vs. frequency

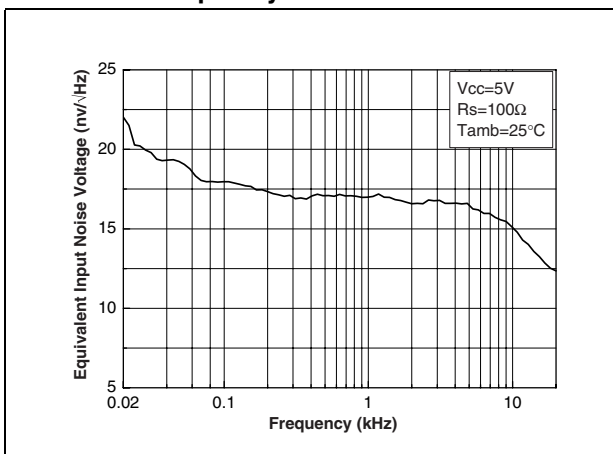


Figure 60. Output voltage swing vs. power supply

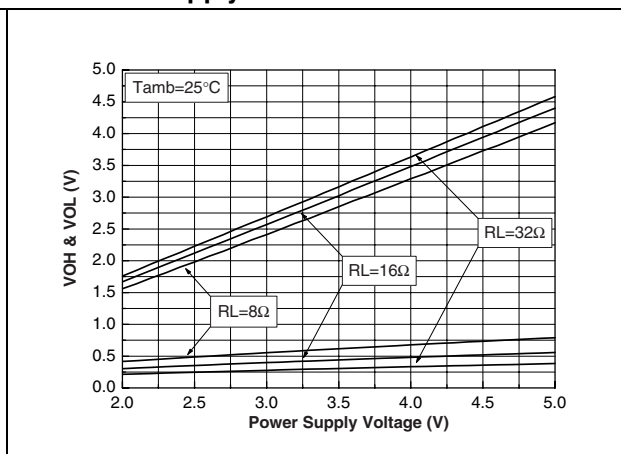


Figure 61. Crosstalk vs. frequency

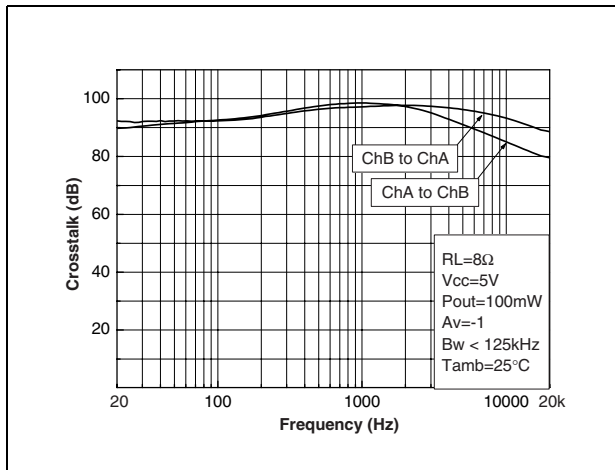


Figure 62. Crosstalk vs. frequency

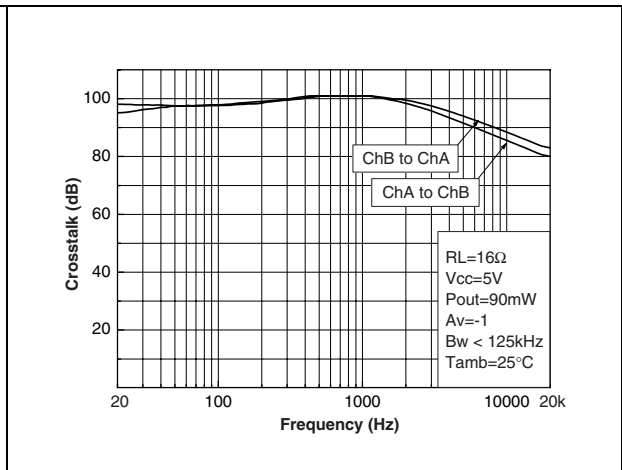


Figure 63. Crosstalk vs. frequency

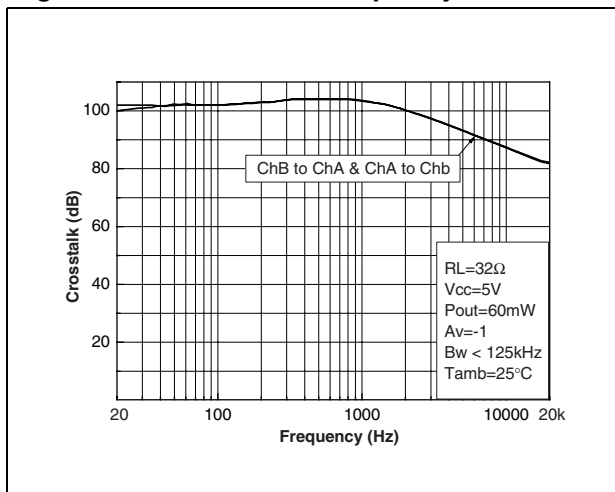


Figure 64. Crosstalk vs. frequency

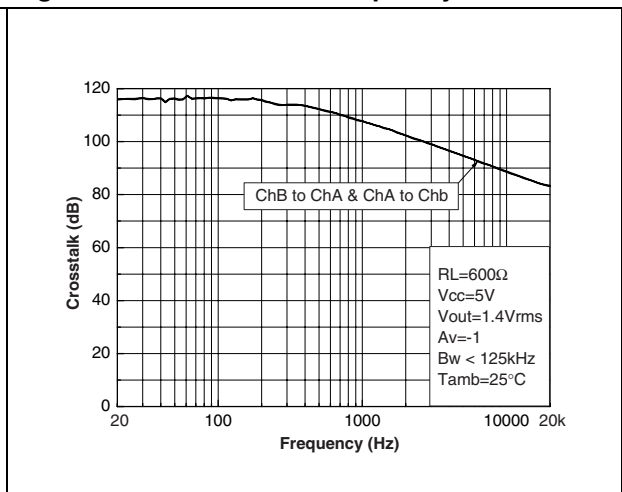


Figure 65. Crosstalk vs. frequency

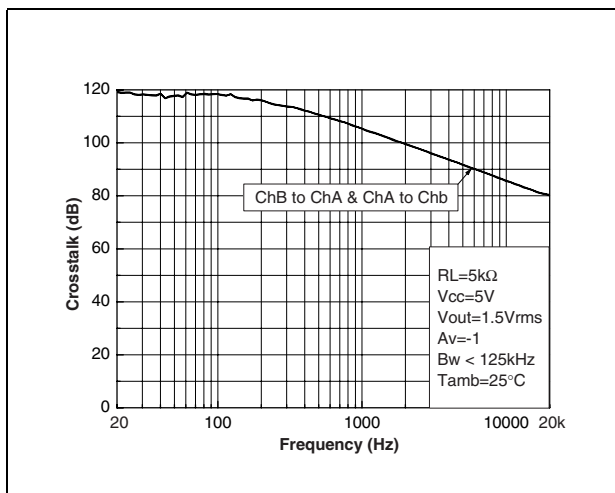


Figure 66. Lower cut off frequency vs. output capacitor

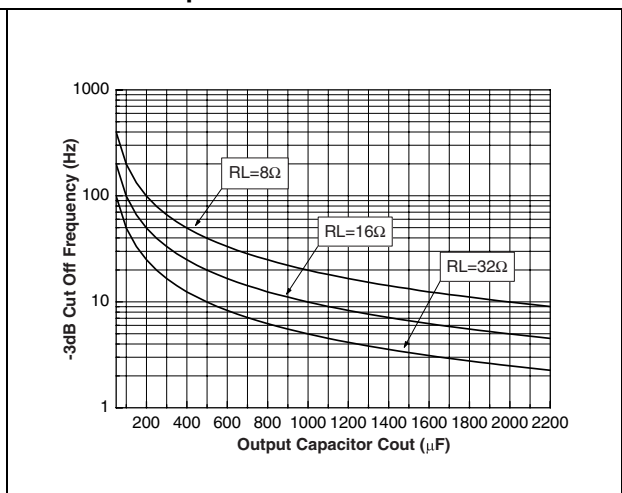


Figure 67. Lower cut off frequency vs. input capacitor

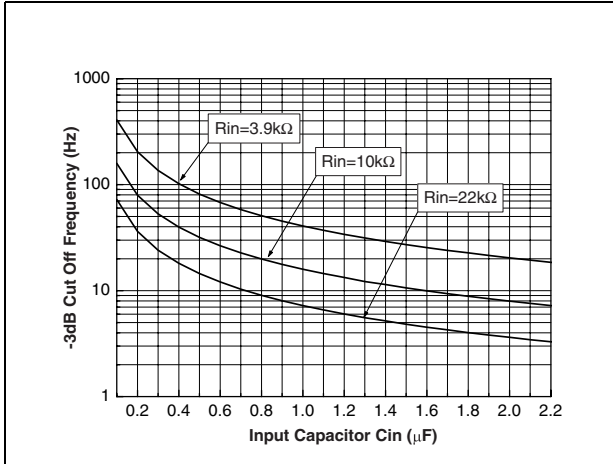


Figure 68. Typical distribution of THD + N

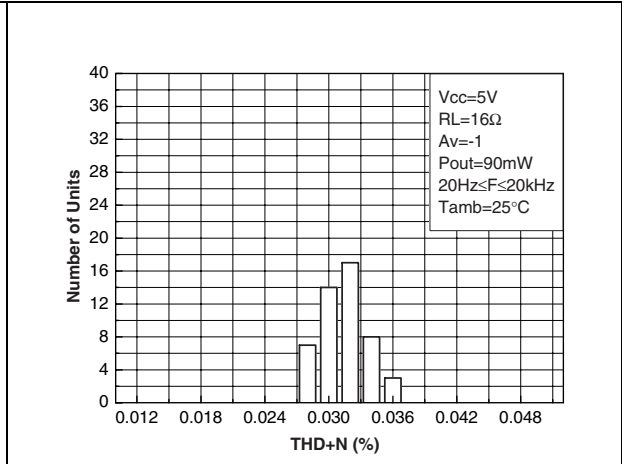


Figure 69. Best case distribution of THD + N

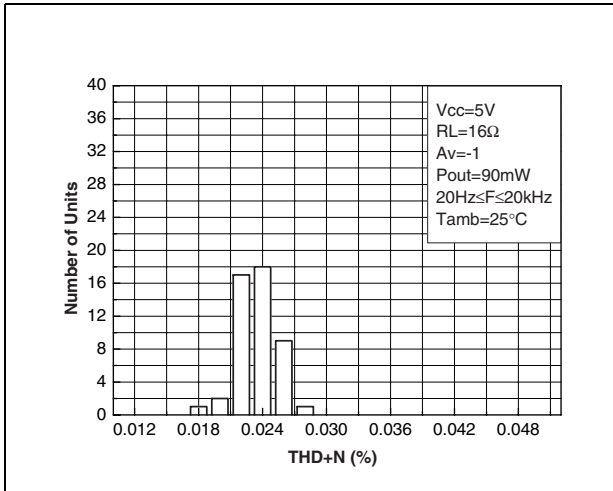


Figure 70. Worst case distribution of THD + N

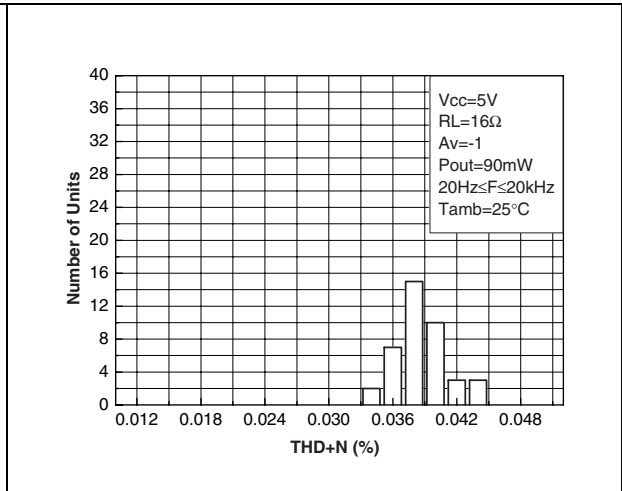


Figure 71. Typical distribution of THD + N

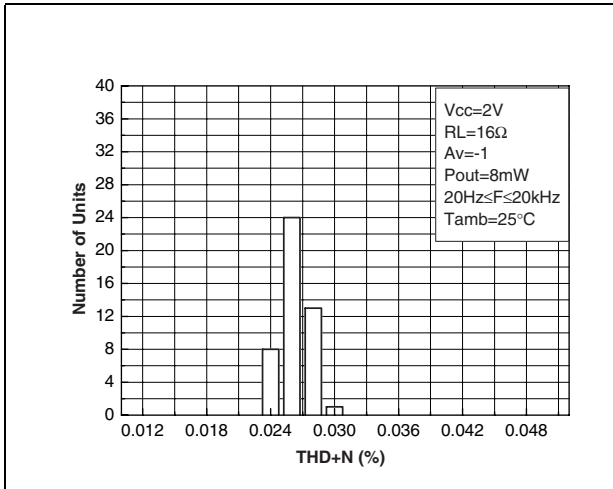


Figure 72. Best case distribution of THD + N

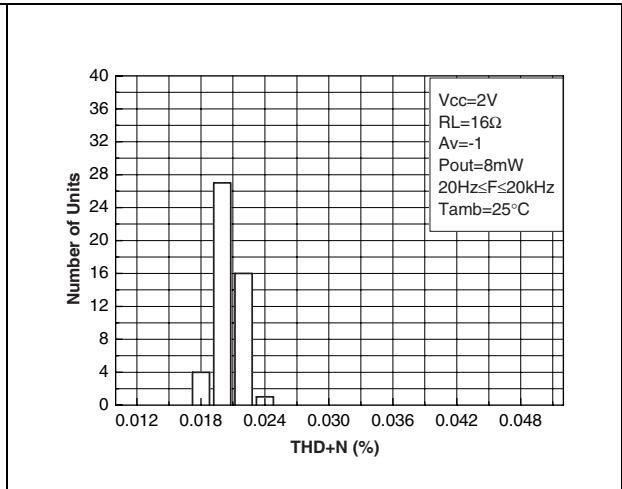


Figure 73. Worst case distribution of THD + N

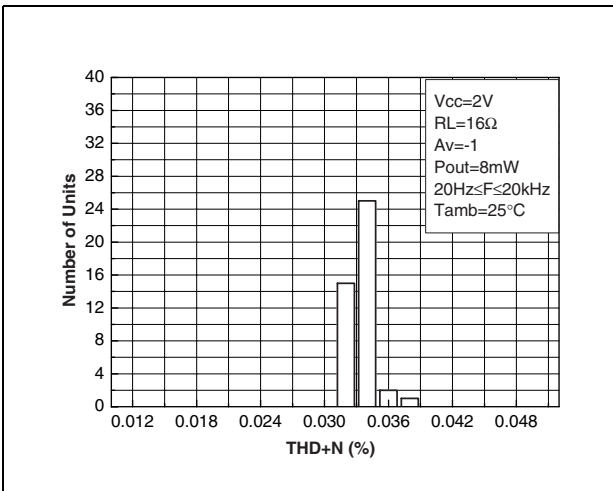


Figure 74. Typical distribution of TDH + N

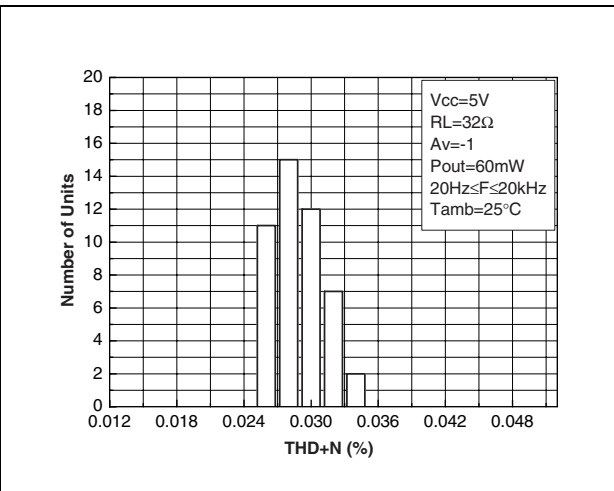


Figure 75. Best case distribution of THD + N

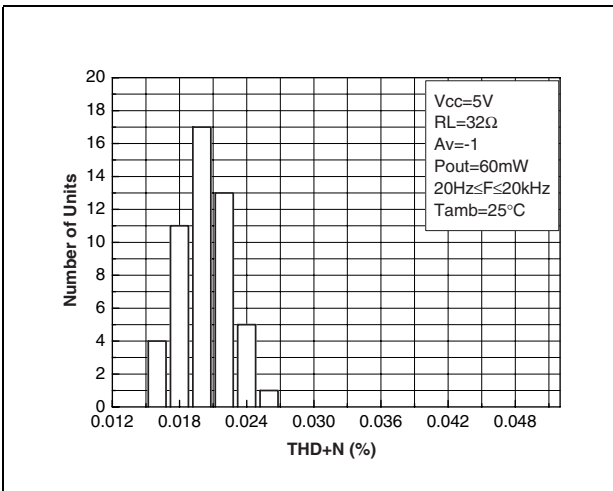


Figure 76. Worst case distribution of THD + N

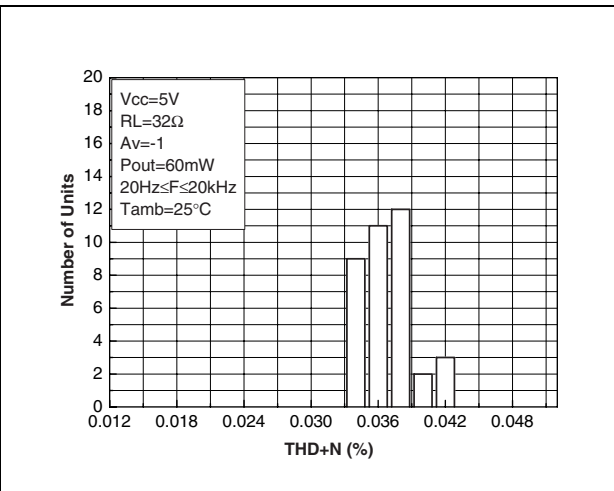


Figure 77. Typical distribution of TDH + N

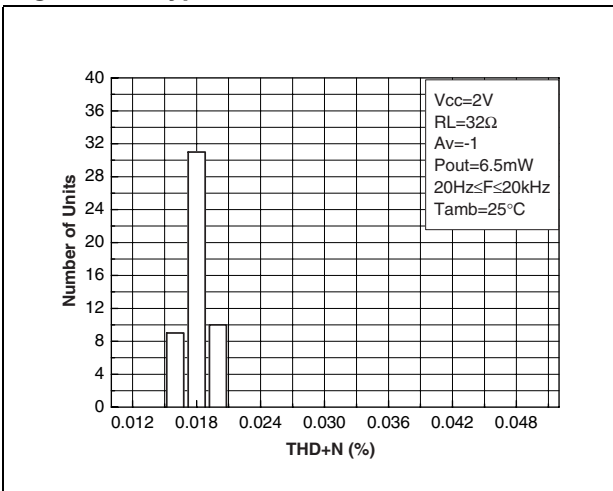


Figure 78. Best case distribution of THD + N

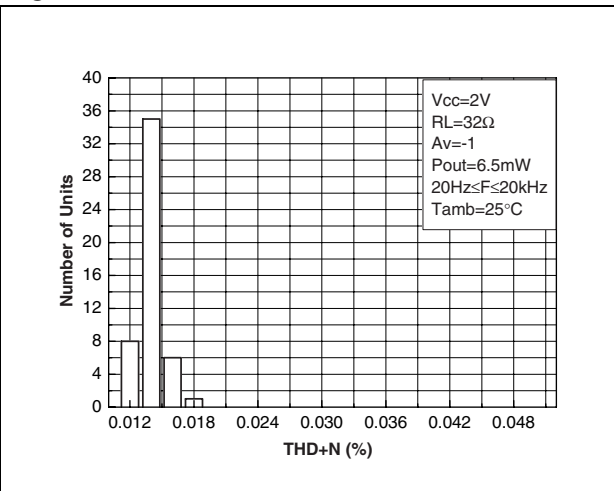
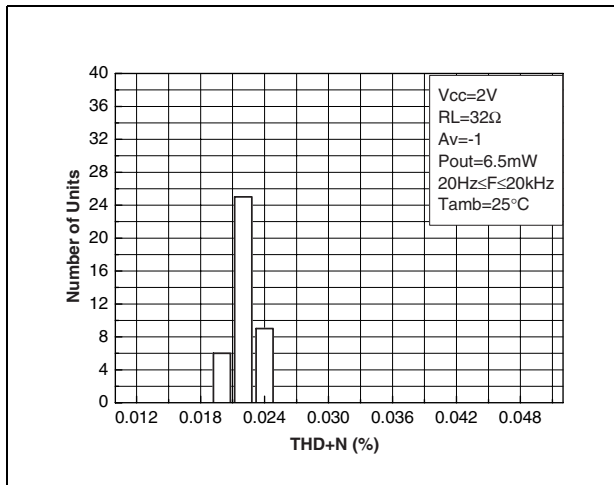


Figure 79. Worst case distribution of THD + N

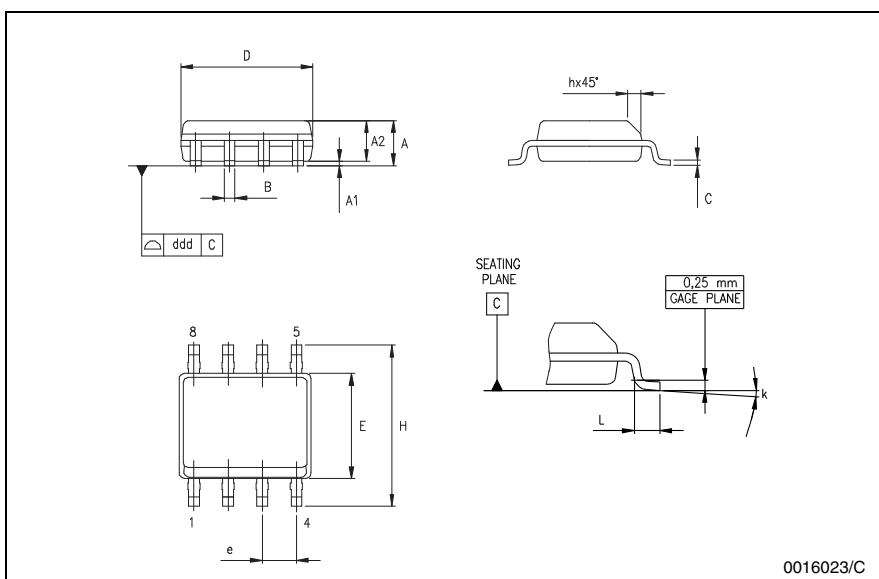


3 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

3.1 SO-8 Package

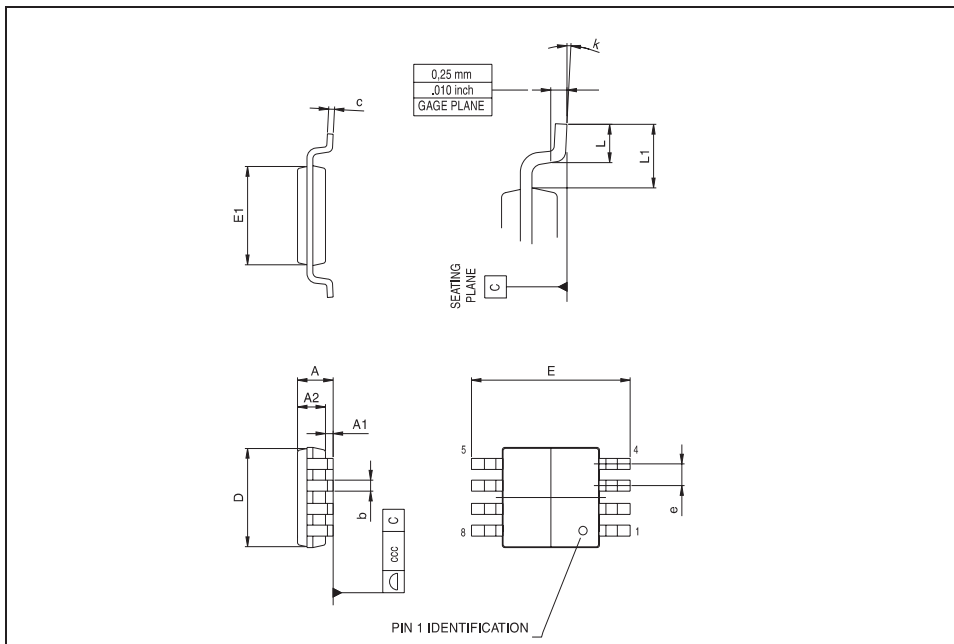
| SO-8 MECHANICAL DATA | | | | | | |
|----------------------|-----------|------|------|-------|-------|-------|
| DIM. | mm. | | | inch | | |
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.10 | | 0.25 | 0.04 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D | 4.80 | | 5.00 | 0.189 | | 0.197 |
| E | 3.80 | | 4.00 | 0.150 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.80 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 8° (max.) | | | | | |
| ddd | | | 0.1 | | | 0.04 |



0016023/C

3.2 MiniSO-8 Package

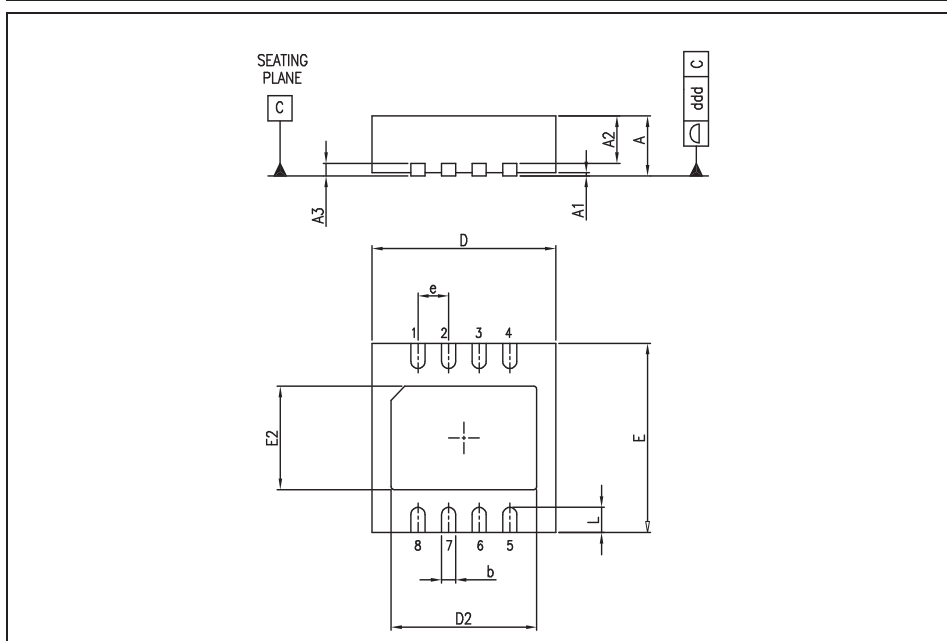
| miniSO-8 MECHANICAL DATA | | | | | | |
|--------------------------|------|------|------|-------|-------|-------|
| DIM. | mm. | | | inch | | |
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.1 | | | 0.043 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.78 | 0.86 | 0.94 | 0.031 | 0.031 | 0.037 |
| b | 0.25 | 0.33 | 0.40 | 0.010 | 0.13 | 0.013 |
| c | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 4.75 | 4.90 | 5.05 | 0.187 | 0.193 | 0.199 |
| E1 | 2.90 | 3.00 | 3.10 | .0114 | 0.118 | 0.122 |
| e | | 0.65 | | | 0.026 | |
| K | 0° | | 6° | 0° | | 6° |
| L | 0.40 | 0.55 | 0.70 | 0.016 | 0.022 | 0.028 |
| L1 | | | 0.10 | | | 0.004 |



3.3 DFN8 Package

DFN8 (3x3) MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|-------|------|-------|------|-------|------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 0.80 | 0.90 | 1.00 | 31.5 | 35.4 | 39.4 |
| A1 | | 0.02 | 0.05 | | 0.8 | 2.0 |
| A2 | | 0.70 | | | 27.6 | |
| A3 | | 0.20 | | | 7.9 | |
| b | 0.18 | 0.23 | 0.30 | 7.1 | 9.1 | 11.8 |
| D | 2.875 | 3.00 | 3.125 | | 118.1 | |
| D2 | 2.23 | 2.38 | 2.48 | 87.8 | 93.7 | 97.7 |
| E | 2.875 | 3.00 | 3.125 | | 118.1 | |
| E2 | 1.49 | 1.64 | 1.74 | 58.7 | 64.6 | 68.5 |
| e | | 0.50 | | | 19.7 | |
| L | 0.30 | 0.40 | 0.50 | 11.8 | 15.7 | 19.7 |



4 Revision history

| Date | Revision | Changes |
|-----------|----------|---|
| June 2003 | 1 | Initial release. |
| Nov. 2005 | 2 | The following changes were made in this revision: <ul style="list-style-type: none">– Lead temperature for lead-free added see Table 1: Key parameters and their absolute maximum ratings on page 2.– Formatting changes throughout. |

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