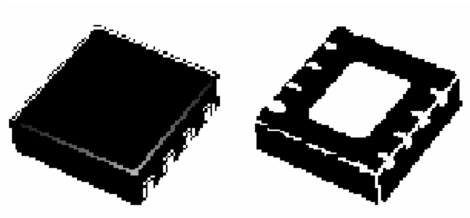
TS4962

2.8 W filter-free mono class D audio power amplifier

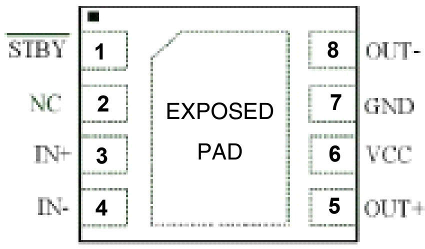
Features

- Operating from V_{CC} = 2.4 V to 5.5 V
- Standby mode active low
- Output power: 2.8 W into 4 Ω and 1.7 W into 8 Ω with 10% THD+N maximum and 5 V power supply
- Output power: 2.2 W at 5 V or 0.7 W at 3.0 V into 4 Ω with 1% THD+N maximum
- Output power: 1.4 W at 5 V or 0.5 W at 3.0 V into 8 Ω with 1% THD+N maximum
- Adjustable gain via external resistors
- Low current consumption 2 mA at 3 V
- Efficiency: 88% typical
- Signal to noise ratio: 85 dB typical
- PSRR: 63 dB typical at 217 Hz with 6 dB gain
- PWM base frequency: 280 kHz
- Low pop & click noise
- Thermal shutdown protection
- Available in DFN8 3 x 3 mm package

DFN8 3 x 3 mm



TS4962IQT pinout



Applications

- Cellular phones
- PDAs
- Notebook PCs

Description

The TS4962 is a differential class-D BTL power amplifier. It can drive up to 2.2 W into a 4 Ω load and 1.4 W into an 8 Ω load at 5 V. It achieves outstanding efficiency (88% typ.) compared to standard AB-class audio amps.

The gain of the device can be controlled via two external gain setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5 ms. A standby function (active low) enables the current consumption to be reduced to 10 nA typical.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1) (2)	6	V
V_i	Input voltage (3)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient DFN8 package	120	°C/W
Pd	Power dissipation	Internally limited (4)	
ESD	Human body model(5)	2	kV
	Machine model(6)	200	V
	Charged device model(7)		
Latch-up	Latch-up immunity	200	mA
V_{STBY}	Standby pin maximum voltage (8)	GND to V_{CC}	V
	Lead temperature (soldering, 10sec)	260	°C

1. Caution: this device is not protected in the event of abnormal operating conditions such as short-circuiting between any one output pin and ground or between any one output pin and V_{CC}, and between individual output pins.
2. All voltage values are measured with respect to the ground pin.
3. The magnitude of the input signal must never exceed V_{CC} + 0.3 V/GND - 0.3 V.
4. Exceeding the power derating curves during a long period will provoke abnormal operation.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.
8. The magnitude of the standby signal must never exceed V_{CC} + 0.3 V/GND - 0.3 V.

Table 2. Dissipation ratings

Package	Derating factor	Power rating at 25°C	Power rating at 85°C
DFN8	20 mW/°C	2.5 W	1.3 W

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	2.4 to 5.5	V
V_{IC}	Common mode input voltage range (2)	0.5 to V_{CC}-0.8	V
V_{STBY}	Standby voltage input: (3) Device ON Device OFF	$1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ (4)	V
R_L	Load resistor	≥ 4	Ω
R_{thja}	Thermal resistance junction to ambient DFN8 package (5)	50	°C/W

1. For V_{CC} between 2.4 V and 2.5 V, the operating temperature range is reduced to $0°C \leq T_{amb} \leq 70°C$.
2. For V_{CC} between 2.4V and 2.5V, the common mode input range must be set at $V_{CC}/2$.
3. Without any signal on V_{STBY}, the device will be in standby.
4. Minimum current consumption is obtained when V_{STBY} = GND.
5. When mounted on a 4-layer PCB.

2 Application overview

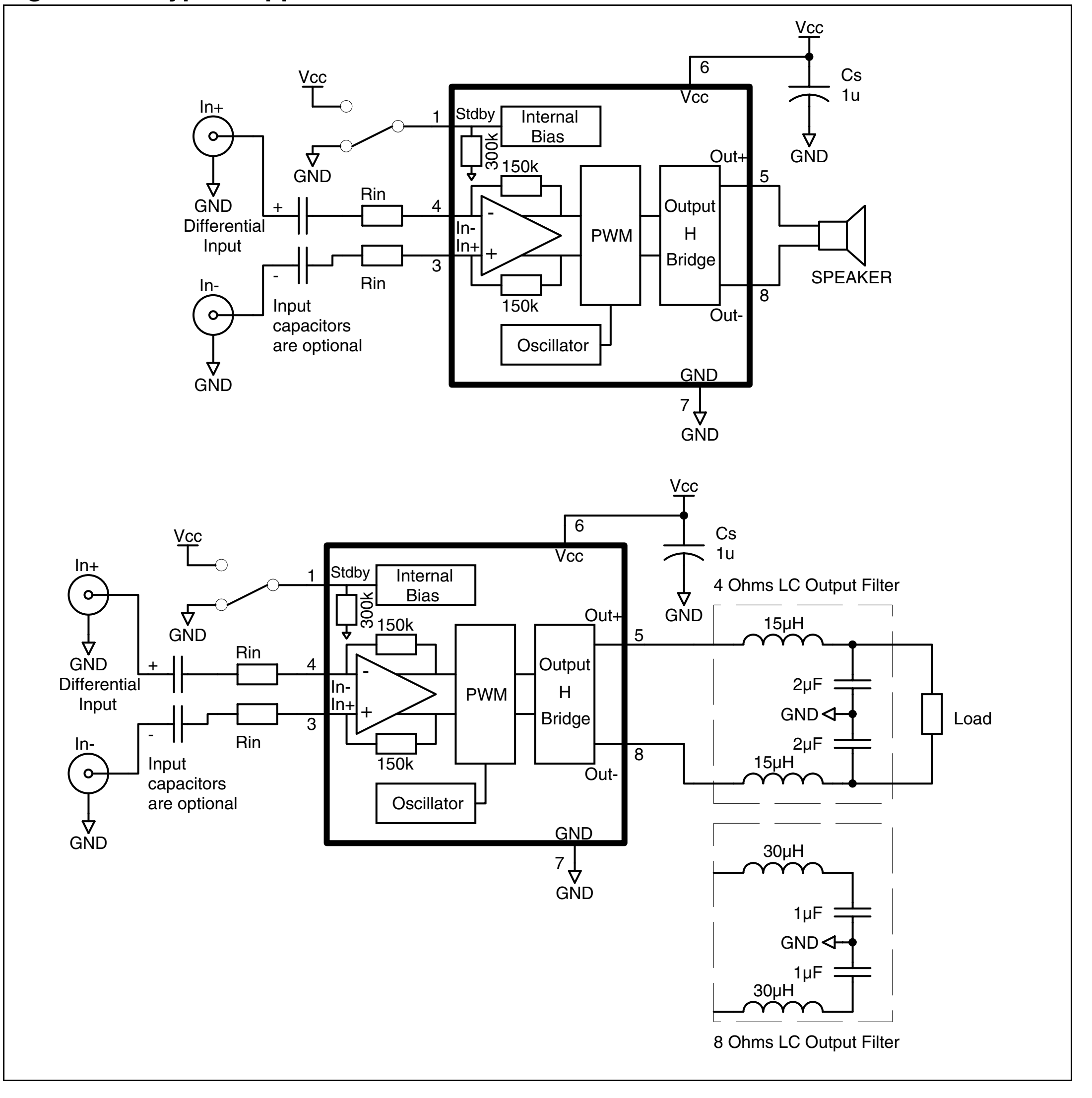
Table 4. External component information

Component	Functional description
C_S	Bypass supply capacitor. Install as close as possible to the TS4962 to minimize high-frequency ripple. A 100 nF ceramic capacitor should be added to enhance the power supply filtering at high frequencies.
R_{in}	Input resistor used to program the TS4962's differential gain (gain = 300 kΩ/R_{in} with R_{in} in kΩ).
Input capacitor	Because of common-mode feedback, these input capacitors are optional. However, they can be added to form with R_{in} a 1st order high-pass filter with -3 dB cut-off frequency = $1/(2*\pi*R_{in}*C_{in})$.

Table 5. Pin description

Pin number	Pin name	Description
1	STBY	Standby input pin (active low)
2	NC	No internal connection pin
3	IN+	Positive input pin
4	IN-	Negative input pin
5	OUT+	Positive output pin
6	VCC	Power supply input pin
7	GND	Ground input pin
8	OUT-	Negative output pin
	Exposed pad	Exposed pad can be connected to ground (pin 7) or left floating

Figure 1. Typical application schematics



3 Electrical characteristics

Table 6. Electrical characteristics at V_{CC} = +5 V, with GND = 0 V, V_{icm} = 2.5 V, and T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2.3	3.3	mA
I_{STBY}	Standby current (1) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power, G = 6 dB THD = 1% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		2.2 2.8 1.4 1.7		W
THD + N	Total harmonic distortion + noise P_{out} = 850 mW_{RMS}, G = 6 dB, 20 Hz < f < 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 1 W_{RMS}, G = 6 dB, f = 1 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz		2 0.4		%
Efficiency	Efficiency P_{out} = 2 W_{RMS}, R_L = 4 Ω +≥ 15 µH P_{out} = 1.2 W_{RMS}, R_L = 8 Ω+≥ 15 µH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded (2) f = 217 Hz, R_L = 8 Ω, G = 6 dB, V_{ripple} = 200 mV_{pp}		63		dB
CMRR	Common mode rejection ratio f = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔVic = 200 mV_{pp}		57		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency	200	280	360	kHz
SNR	Signal to noise ratio (A weighting), P_{out} = 1.2 W, R_L = 8 Ω		85		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 6. Electrical characteristics at V_{CC} = +5 V, with GND = 0 V, V_{icm} = 2.5 V, and T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20 Hz to 20 kHz, G = 6 dB Unweighted R_L = 4 Ω A-weighted R_L = 4 Ω Unweighted R_L = 8 Ω A-weighted R_L = 8 Ω Unweighted R_L = 4 Ω + 15 µH A-weighted R_L = 4 Ω + 15 µH Unweighted R_L = 4 Ω + 30 µH A-weighted R_L = 4 Ω + 30 µH Unweighted R_L = 8 Ω + 30 µH A-weighted R_L = 8 Ω + 30 µH Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		 85 60 86 62 83 60 88 64 78 57 87 65 82 59		μV_{RMS}

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} at f = 217 Hz.

Table 7. Electrical characteristics at V_{CC} = +4.2 V with GND = 0 V, V_{icm} = 2.1 V and T_{amb} = 25°C (unless otherwise specified)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2.1	3	mA
I_{STBY}	Standby current (2) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power, G = 6 dB THD = 1% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		1.5 1.95 0.9 1.1		W
THD + N	Total harmonic distortion + noise P_{out} = 600 mW_{RMS}, G = 6 dB, 20 Hz < f < 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 700 mW_{RMS}, G = 6 dB, f = 1 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz		2 0.35		%
Efficiency	Efficiency P_{out} = 1.45 W_{RMS}, R_L = 4 Ω +≥ 15 µH P_{out} = 0.9 W_{RMS}, R_L = 8 Ω+≥ 15 µH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded (3) f = 217 Hz, R_L = 8 Ω, G = 6 dB, V_{ripple} = 200 mV_{pp}		63		dB
CMRR	Common mode rejection ratio f = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔVic = 200 mV_{pp}		57		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency	200	280	360	kHz
SNR	Signal to noise ratio (A-weighting) P_{out} = 0.8 W, R_L = 8 Ω		85		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 7. Electrical characteristics at V_{CC} = +4.2 V with GND = 0 V, V_{icm} = 2.1 V and T_{amb} = 25°C (unless otherwise specified)(1) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20 Hz to 20 kHz, G = 6 dB Unweighted R_L = 4 Ω A-weighted R_L = 4 Ω Unweighted R_L = 8 Ω A-weighted R_L = 8 Ω Unweighted R_L = 4 Ω + 15 µH A-weighted R_L = 4 Ω + 15 µH Unweighted R_L = 4 Ω + 30 µH A-weighted R_L = 4 Ω + 30 µH Unweighted R_L = 8 Ω + 30 µH A-weighted R_L = 8 Ω + 30 µH Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		 85 60 86 62 83 60 88 64 78 57 87 65 82 59		μV_{RMS}

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} at f = 217 Hz.

Table 8. Electrical characteristics at V_{CC} = +3.6 V with GND = 0 V, V_{icm} = 1.8 V, T_{amb} = 25°C (unless otherwise specified)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2	2.8	mA
I_{STBY}	Standby current (2) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power, G = 6 dB THD = 1% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		 1.1 1.4 0.7 0.85		W
THD + N	Total harmonic distortion + noise P_{out} = 450 mW$_{RMS}$, G = 6 dB, 20 Hz < f < 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 500 mW$_{RMS}$, G = 6 dB, f = 1 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz		2 0.1		%
Efficiency	Efficiency P_{out} = 1 W$_{RMS}$, R_L = 4 Ω +≥ 15 µH P_{out} = 0.65 W$_{RMS}$, R_L = 8 Ω+≥ 15 µH		 78 88		%
PSRR	Power supply rejection ratio with inputs grounded (3) f = 217 Hz, R_L = 8 Ω, G = 6 dB, V_{ripple} = 200 mV$_{pp}$		62		dB
CMRR	Common mode rejection ratio f = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔVic = 200 mV$_{pp}$		56		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency	200	280	360	kHz
SNR	Signal to noise ratio (A-weighting) P_{out} = 0.6 W, R_L = 8 Ω		83		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 8. Electrical characteristics at V_{CC} = +3.6 V with GND = 0 V, V_{icm} = 1.8 V, T_{amb} = 25°C (unless otherwise specified)(1) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20 Hz to 20 kHz, G = 6 dB				
	Unweighted R_L = 4 Ω		83		
	A-weighted R_L = 4 Ω		57		
	Unweighted R_L = 8 Ω		83		
	A-weighted R_L = 8 Ω		61		
	Unweighted R_L = 4 Ω + 15 µH		81		
	A-weighted R_L = 4 Ω + 15 µH		58		
	Unweighted R_L = 4 Ω + 30 µH		87		μV_{RMS}
	A-weighted R_L = 4 Ω + 30 µH		62		
	Unweighted R_L = 8 Ω + 30 µH		77		
	A-weighted R_L = 8 Ω + 30 µH		56		
	Unweighted R_L = 4 Ω + filter		85		
	A-weighted R_L = 4 Ω + filter		63		
	Unweighted R_L = 4 Ω + filter		80		
	A-weighted R_L = 4 Ω + filter		57		

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is activated when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} at f = 217 Hz.

Table 9. Electrical characteristics at V_{CC} = +3.0 V with GND = 0 V, V_{icm} = 1.5 V, T_{amb} = 25°C (unless otherwise specified)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.9	2.7	mA
I_{STBY}	Standby current (2) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power, G = 6 dB THD = 1% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		0.7 1 0.5 0.6		W
THD + N	Total harmonic distortion + noise P_{out} = 300 mW_{RMS}, G = 6 dB, 20 Hz < f < 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 350 mW_{RMS}, G = 6 dB, f = 1 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz		2 0.1		%
Efficiency	Efficiency P_{out} = 0.7 W_{RMS}, R_L = 4 Ω +≥ 15 µH P_{out} = 0.45 W_{RMS}, R_L = 8 Ω+≥ 15 µH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded (3) f = 217 Hz, R_L = 8 Ω, G = 6 dB, V_{ripple} = 200 mV_{pp}		60		dB
CMRR	Common mode rejection ratio f = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔV_{ic} = 200 mV_{pp}		54		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency	200	280	360	kHz
SNR	Signal to noise ratio (A-weighting) P_{out} = 0.4 W, R_L = 8 Ω		82		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 9. Electrical characteristics at V_{CC} = +3.0 V with GND = 0 V, V_{icm} = 1.5 V, T_{amb} = 25°C (unless otherwise specified)(1) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20 Hz to 20 kHz, G = 6 dB				
	Unweighted R_L = 4 Ω		83		
	A-weighted R_L = 4 Ω		57		
	Unweighted R_L = 8 Ω		83		
	A-weighted R_L = 8 Ω		61		
	Unweighted R_L = 4 Ω + 15 µH		81		
	A-weighted R_L = 4 Ω + 15 µH		58		
	Unweighted R_L = 4 Ω + 30 µH		87		μV_{RMS}
	A-weighted R_L = 4 Ω + 30 µH		62		
	Unweighted R_L = 8 Ω + 30 µH		77		
	A-weighted R_L = 8 Ω + 30 µH		56		
	Unweighted R_L = 4 Ω + filter		85		
	A-weighted R_L = 4 Ω + filter		63		
	Unweighted R_L = 4 Ω + filter		80		
	A-weighted R_L = 4 Ω + filter		57		

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} at f = 217 Hz.

Table 10. Electrical characteristics at V_{CC} = +2.5 V with GND = 0 V, V_{icm} = 1.25V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.7	2.4	mA
I_{STBY}	Standby current (1) No input signal, V_{STBY} = GND		10	1000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power, G = 6 dB THD = 1% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		0.5 0.65 0.33 0.41		W
THD + N	Total harmonic distortion + noise P_{out} = 180 mW_{RMS}, G = 6 dB, 20 Hz < f < 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 200 mW_{RMS}, G = 6 dB, f = 1 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz		1 0.05		%
Efficiency	Efficiency P_{out} = 0.47 W_{RMS}, R_L = 4 Ω +≥ 15 µH P_{out} = 0.3 W_{RMS}, R_L = 8 Ω+≥ 15 µH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded (2) f = 217 Hz, R_L = 8 Ω, G = 6 dB, V_{ripple} = 200 mV_{pp}		60		dB
CMRR	Common mode rejection ratio f = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔV_{ic} = 200 mV_{pp}		54		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency	200	280	360	kHz
SNR	Signal to noise ratio (A-weighting) P_{out} = 0.3 W, R_L = 8 Ω		80		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 10. Electrical characteristics at V_{CC} = +2.5 V with GND = 0 V, V_{icm} = 1.25V, T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20 Hz to 20 kHz, G = 6 dB				μV_{RMS}
	Unweighted R_L = 4 Ω		85		
	A-weighted R_L = 4 Ω		60		
	Unweighted R_L = 8 Ω		86		
	A-weighted R_L = 8 Ω		62		
	Unweighted R_L = 4 Ω + 15 µH		76		
	A-weighted R_L = 4 Ω + 15 µH		56		
	Unweighted R_L = 4 Ω + 30 µH		82		
	A-weighted R_L = 4 Ω + 30 µH		60		
	Unweighted R_L = 8 Ω + 30 µH		67		
	A-weighted R_L = 8 Ω + 30 µH		53		
	Unweighted R_L = 4 Ω + filter		78		
	A-weighted R_L = 4 Ω + filter		57		
	Unweighted R_L = 4 Ω + filter		74		
	A-weighted R_L = 4 Ω + filter		54		

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} at f = 217 Hz.

Table 11. Electrical characteristics at V_{CC} +2.4 V with GND = 0 V, V_{icm} = 1.2 V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.7		mA
I_{STBY}	Standby current (1) No input signal, V_{STBY} = GND		10		nA
V_{oo}	Output offset voltage No input signal, R_L = 8 Ω		3		mV
P_{out}	Output power, G = 6 dB THD = 1% max, f = 1 kHz, R_L = 4 Ω THD = 10% max, f = 1 kHz, R_L = 4 Ω THD = 1% max, f = 1 kHz, R_L = 8 Ω THD = 10% max, f = 1 kHz, R_L = 8 Ω		0.42 0.61 0.3 0.38		W
THD + N	Total harmonic distortion + noise P_{out} = 150 mW_{RMS}, G = 6 dB, 20 Hz < f < 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz		1		%
Efficiency	Efficiency P_{out} = 0.38 W_{RMS}, R_L = 4 Ω +≥ 15 µH P_{out} = 0.25 W_{RMS}, R_L = 8 Ω+≥ 15 µH		77 86		%
CMRR	Common mode rejection ratio f = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔV_{ic} = 200 mV_{pp}		54		dB
Gain	Gain value (R_{in} in kΩ)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency		280		kHz
SNR	Signal to noise ratio (A-weighting) P_{out} = 0.25 W, R_L = 8 Ω		80		dB
t_{WU}	Wake-up time		5		ms
t_{STBY}	Standby time		5		ms

Table 11. Electrical characteristics at V_{CC} +2.4 V with GND = 0 V, V_{icm} = 1.2 V, T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20 Hz to 20 kHz, G = 6 dB				μV_{RMS}
	Unweighted R_L = 4 Ω		85		
	A-weighted R_L = 4 Ω		60		
	Unweighted R_L = 8 Ω		86		
	A-weighted R_L = 8 Ω		62		
	Unweighted R_L = 4 Ω + 15 µH		76		
	A-weighted R_L = 4 Ω + 15 µH		56		
	Unweighted R_L = 4 Ω + 30 µH		82		
	A-weighted R_L = 4 Ω + 30 µH		60		
	Unweighted R_L = 8 Ω + 30 µH		67		
	A-weighted R_L = 8 Ω + 30 µH		53		
	Unweighted R_L = 4 Ω + filter		78		
	A-weighted R_L = 4 Ω + filter		57		
	Unweighted R_L = 4 Ω + filter		74		
	A-weighted R_L = 4 Ω + filter		54		

1. Standby mode is active when V_{STBY} is tied to GND.

3.1 Electrical characteristics curves

The graphs shown in this section use the following abbreviations.

- R_L + 15 µH or 30 µH = pure resistor + very low series resistance inductor
- Filter = LC output filter (1 µF + 30 µH for 4 Ω and 0. 5µF + 60 µH for 8 Ω)

All measurements are done with C_{S1} = 1 µF and C_{S2} = 100 nF (see *Figure 2*), except for the PSRR where C_{S1} is removed (see *Figure 3*).

Figure 2. Schematic used for test measurements

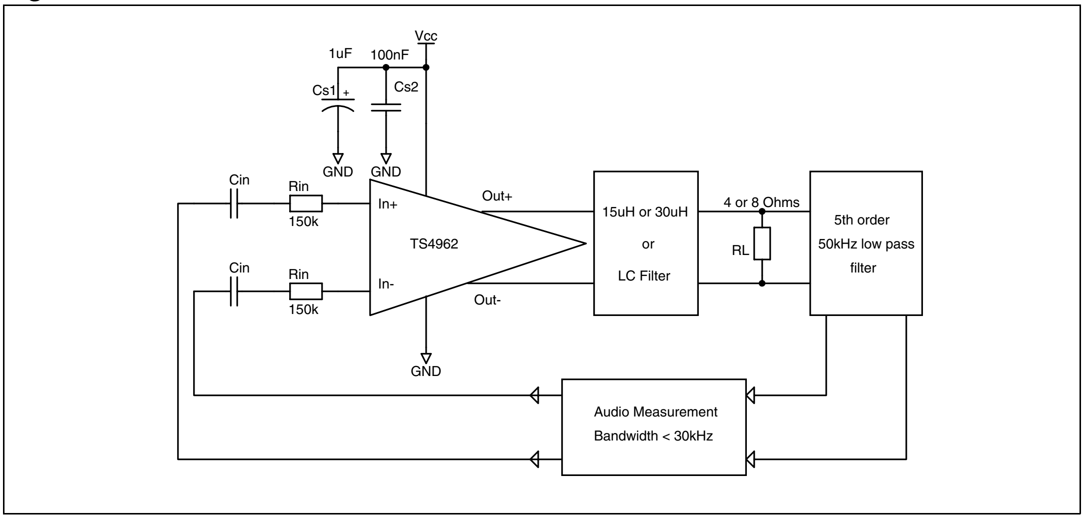


Figure 3. Schematic used for PSSR measurements

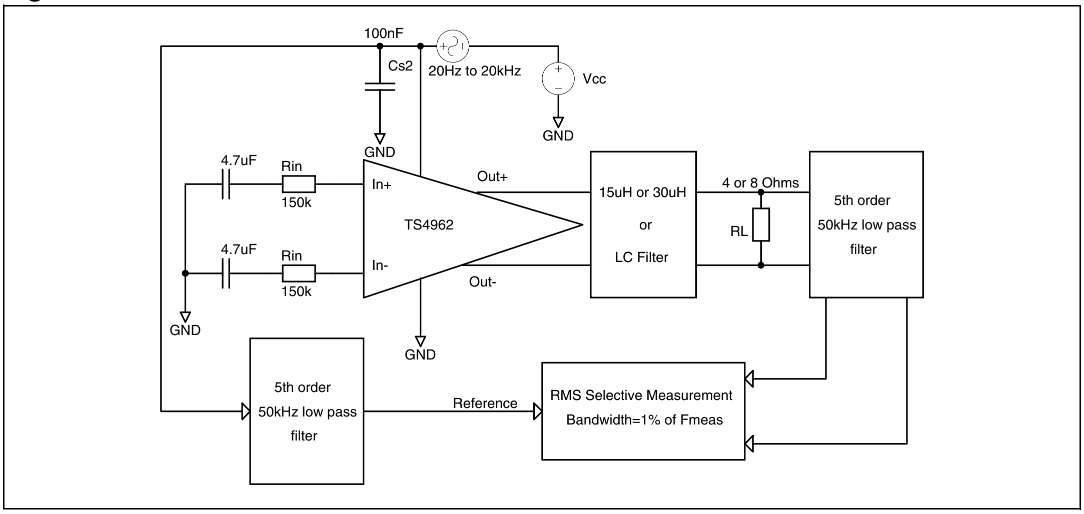


Figure 4. Current consumption vs. power supply voltage

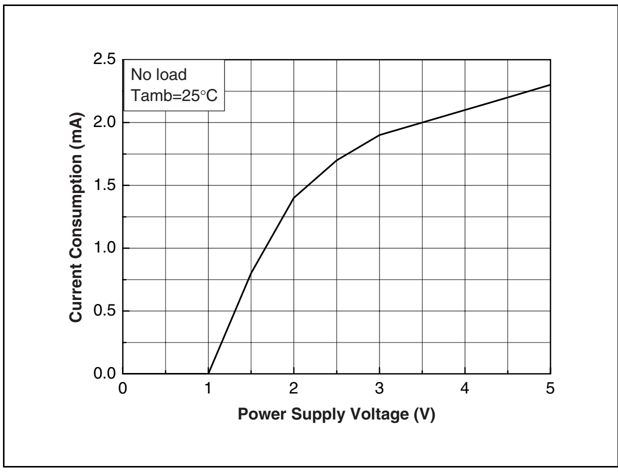


Figure 5. Current consumption vs. standby voltage

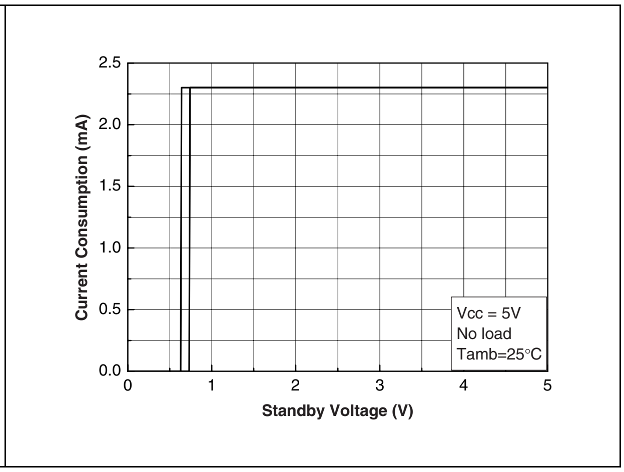


Figure 6. Current consumption vs. standby voltage

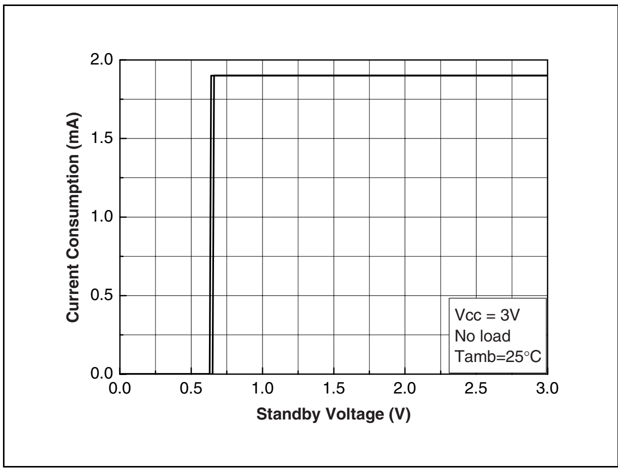


Figure 7. Output offset voltage vs. common mode input voltage

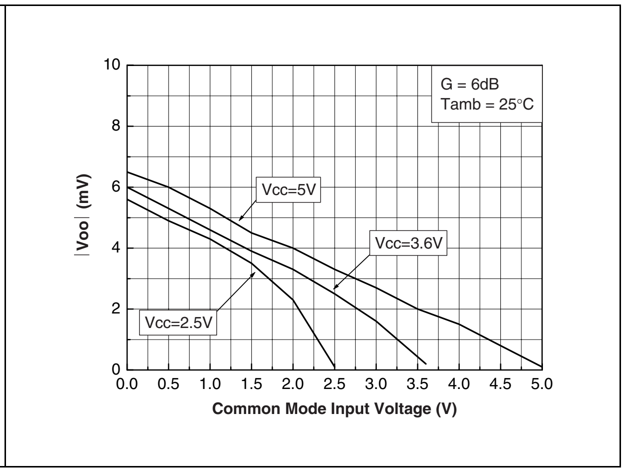


Figure 8. Efficiency vs. output power

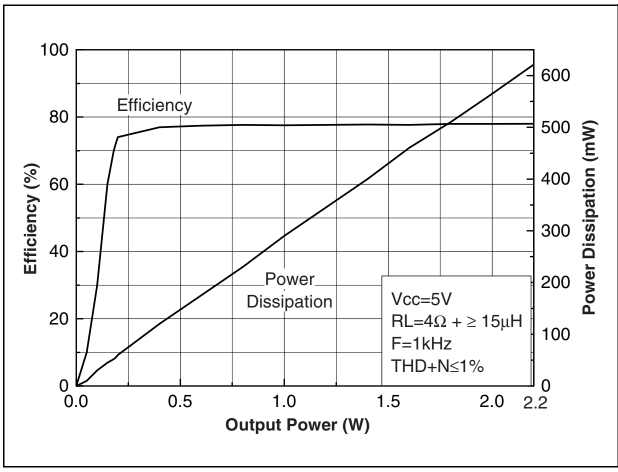


Figure 9. Efficiency vs. output power

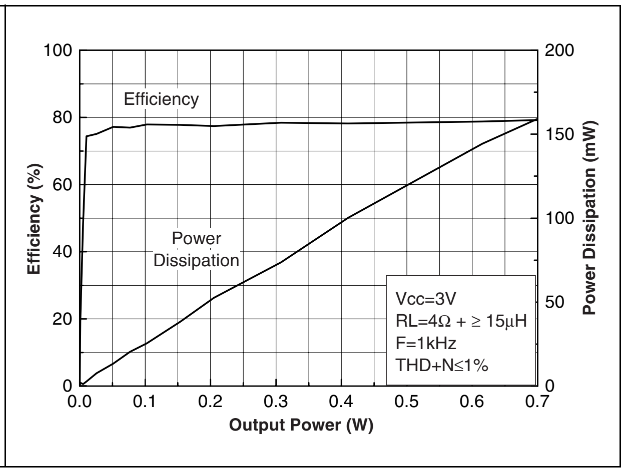


Figure 10. Efficiency vs. output power

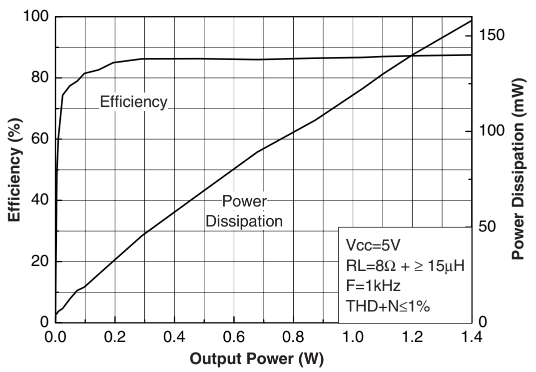


Figure 11. Efficiency vs. output power

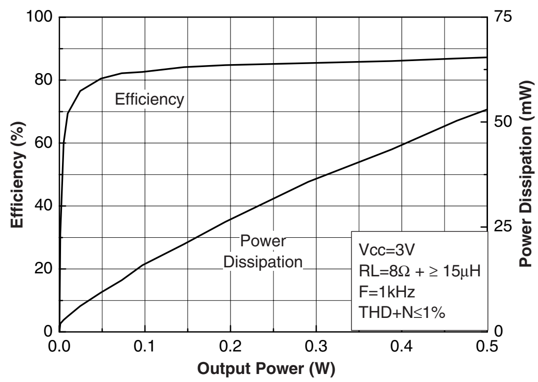


Figure 12. Output power vs. power supply voltage

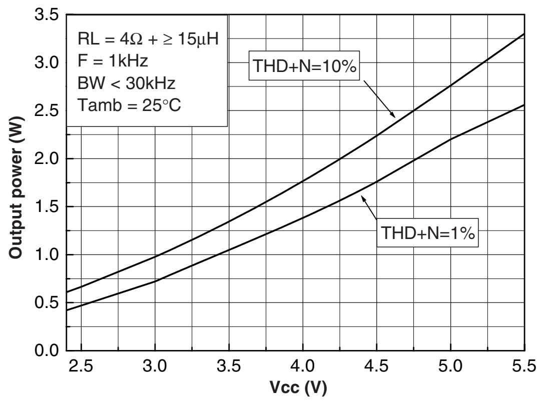


Figure 13. Output power vs. power supply voltage

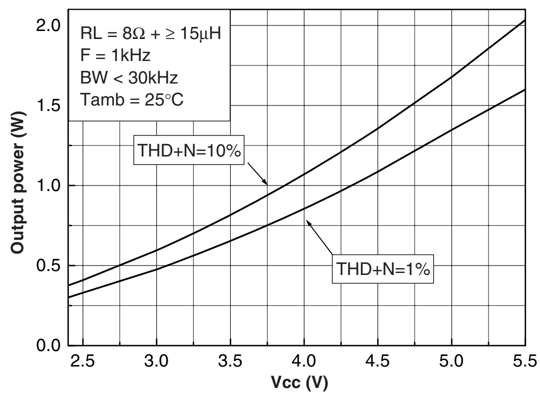


Figure 14. PSRR vs. frequency

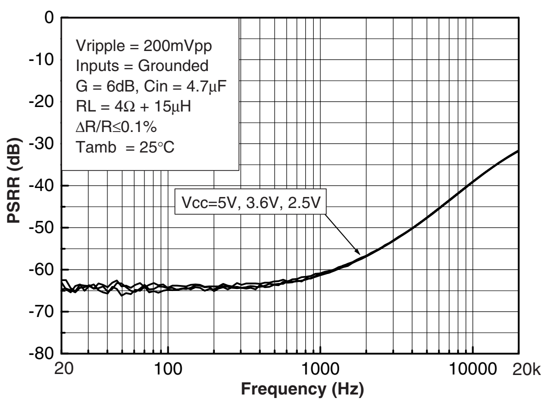


Figure 15. PSRR vs. frequency

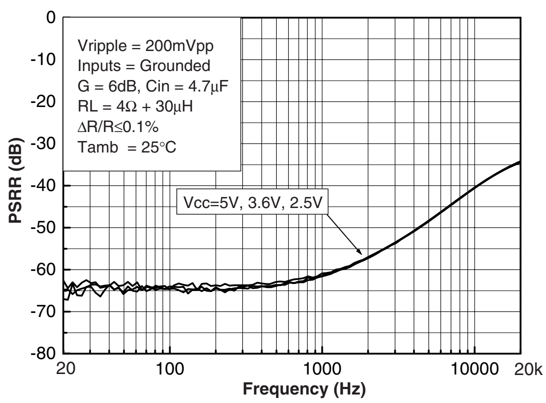


Figure 16. PSRR vs. frequency

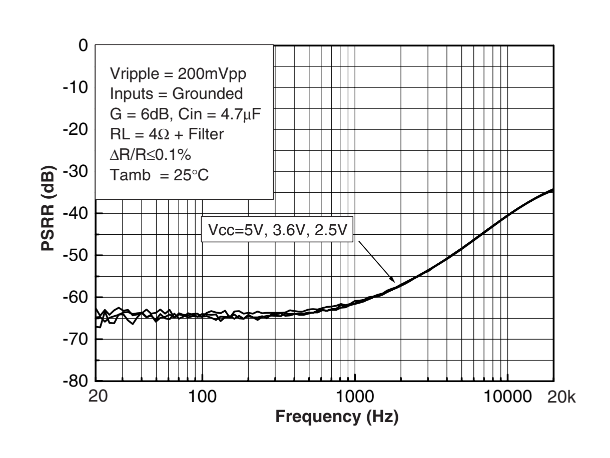


Figure 17. PSRR vs. frequency

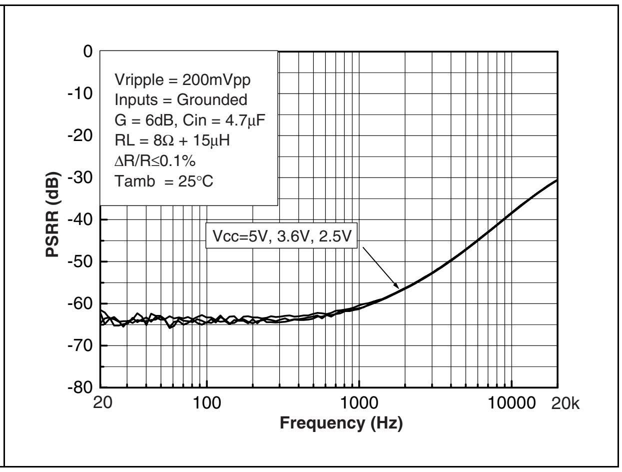


Figure 18. PSRR vs. frequency

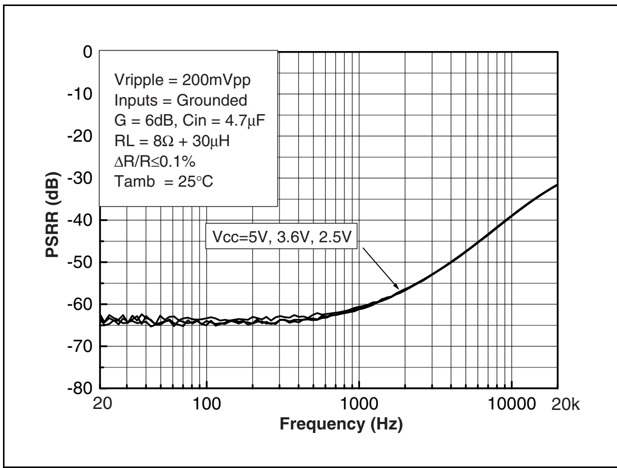


Figure 19. PSRR vs. frequency

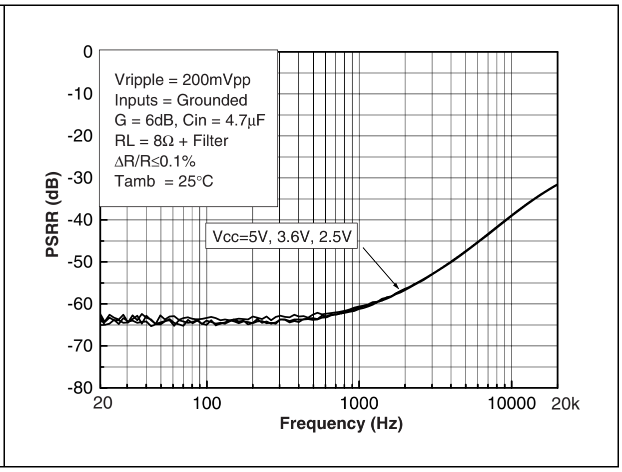


Figure 20. PSRR vs. common mode input voltage

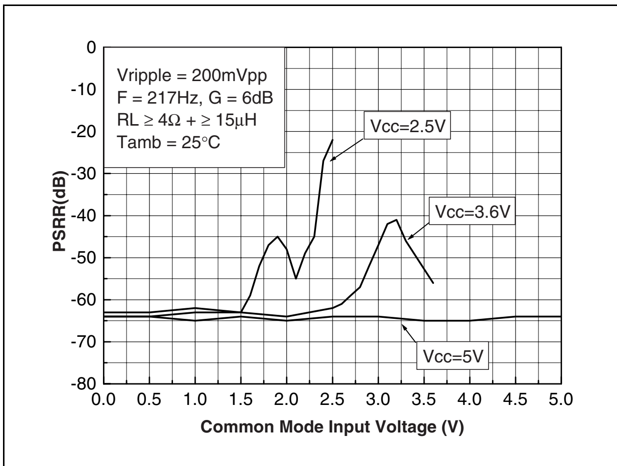


Figure 21. CMRR vs. frequency

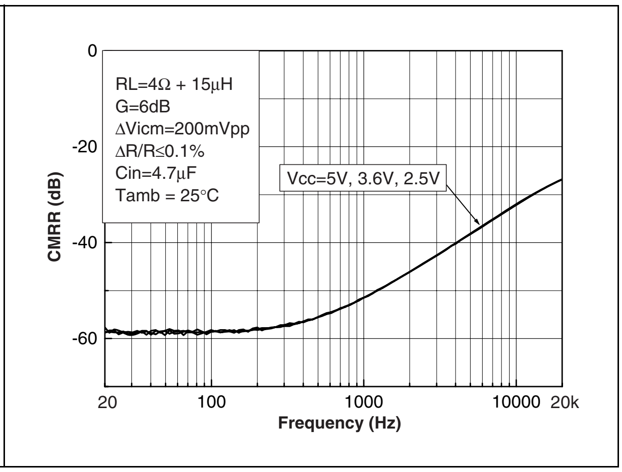


Figure 22. CMRR vs. frequency

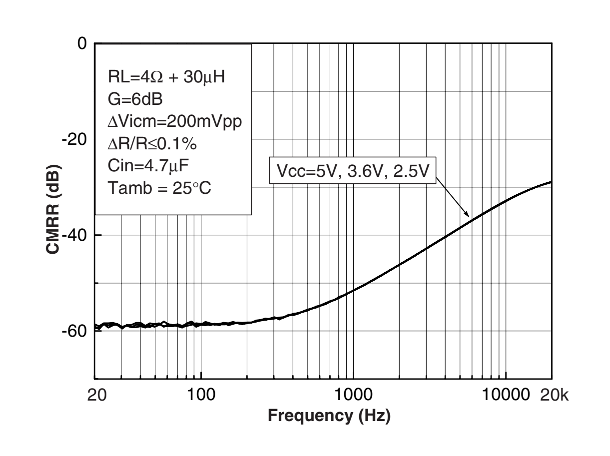


Figure 23. CMRR vs. frequency

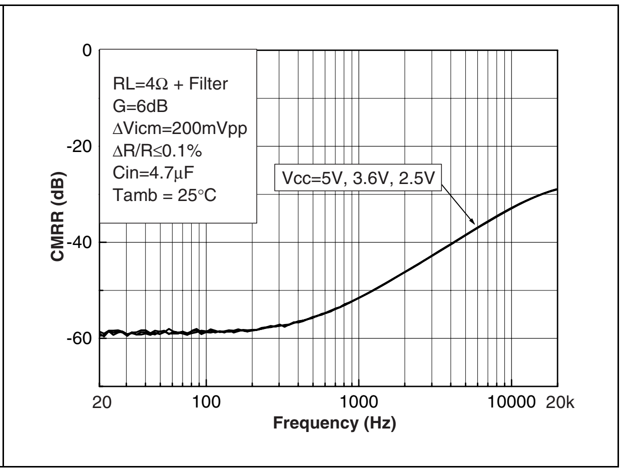


Figure 24. CMRR vs. frequency

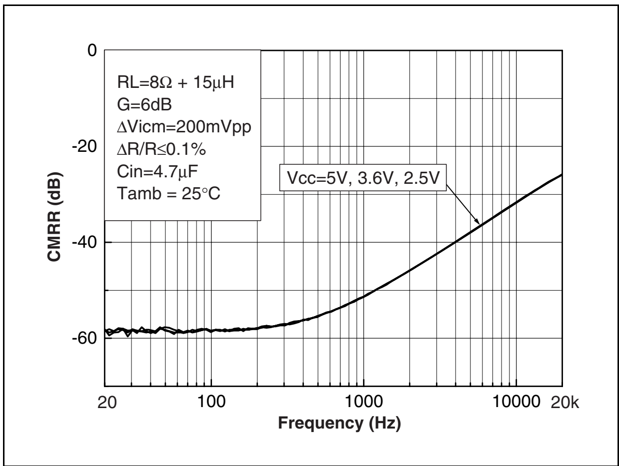


Figure 25. CMRR vs. frequency

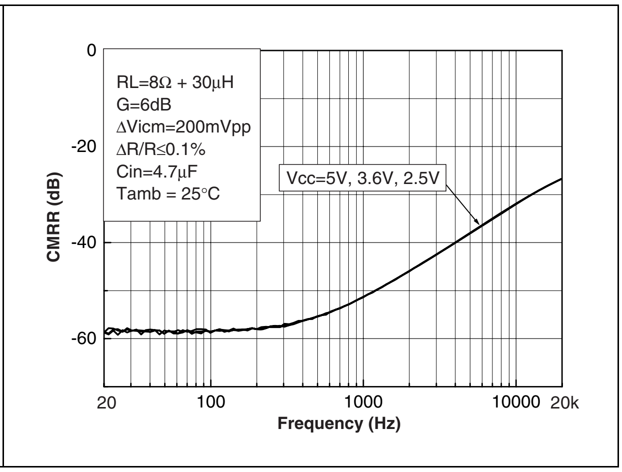


Figure 26. CMRR vs. frequency

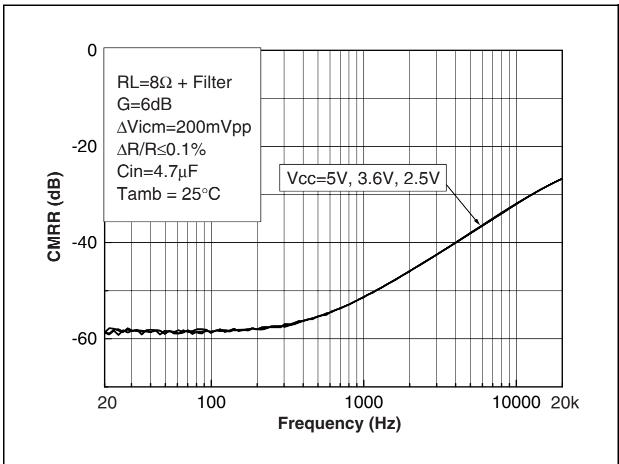


Figure 27. CMRR vs. common mode input voltage

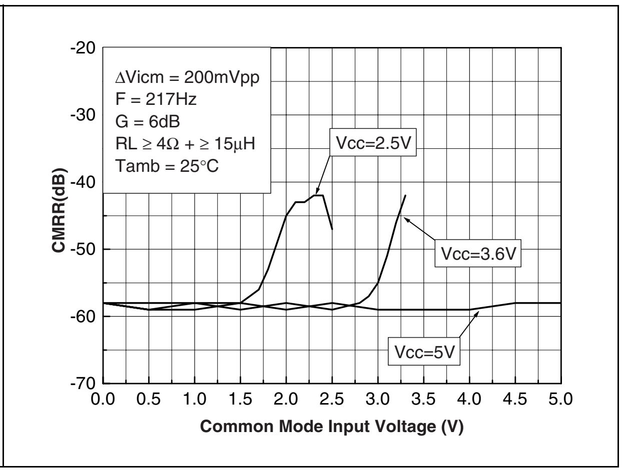


Figure 28. THD+N vs. output power

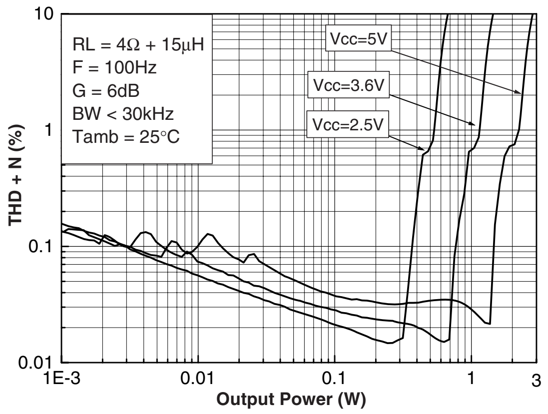


Figure 29. THD+N vs. output power

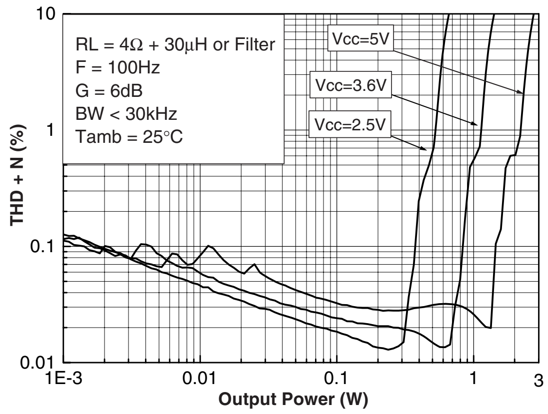


Figure 30. THD+N vs. output power

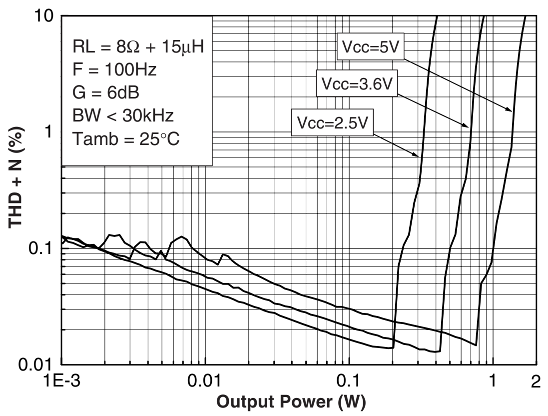


Figure 31. THD+N vs. output power

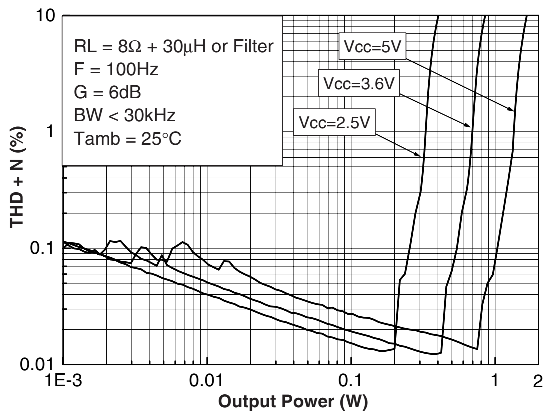


Figure 32. THD+N vs. output power

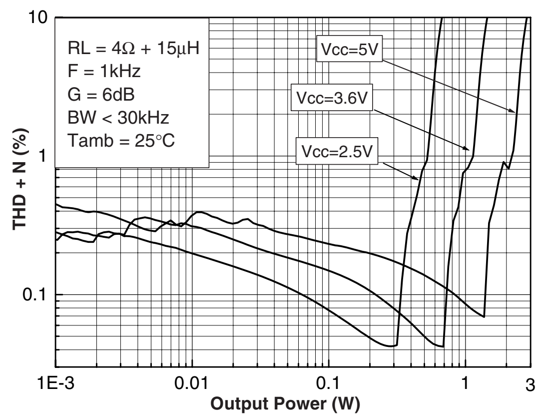


Figure 33. THD+N vs. output power

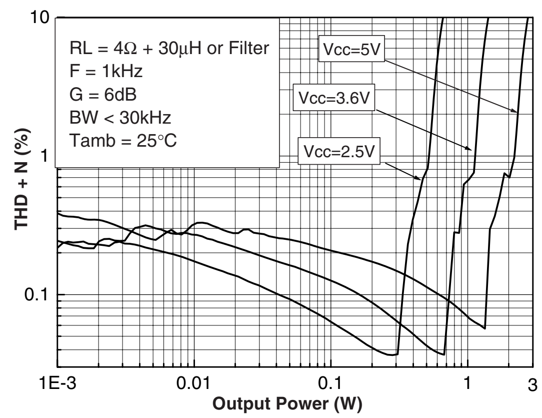


Figure 34. THD+N vs. output power

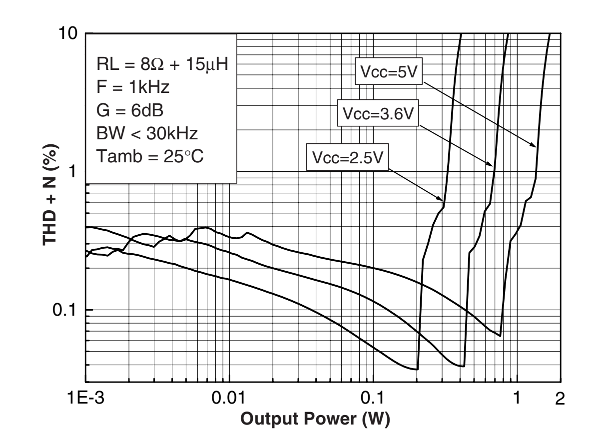


Figure 35. THD+N vs. output power

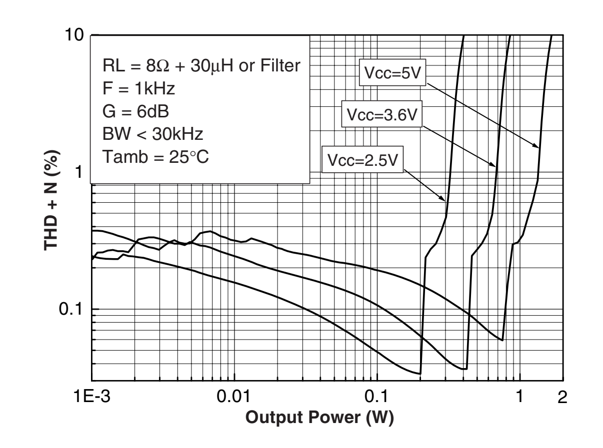


Figure 36. THD+N vs. frequency

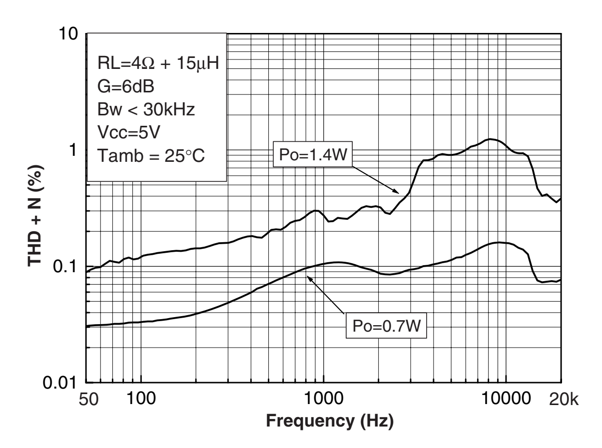


Figure 37. THD+N vs. frequency

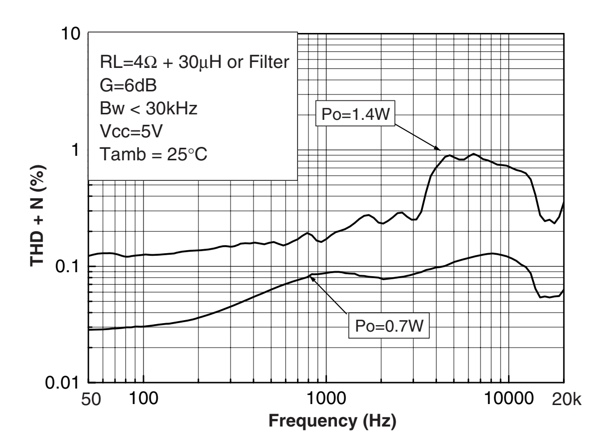


Figure 38. THD+N vs. frequency

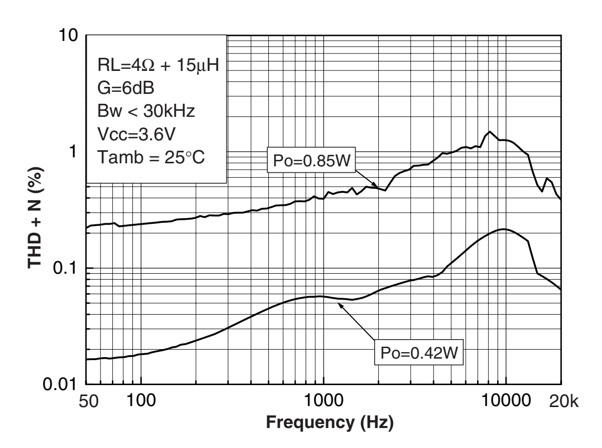


Figure 39. THD+N vs. frequency

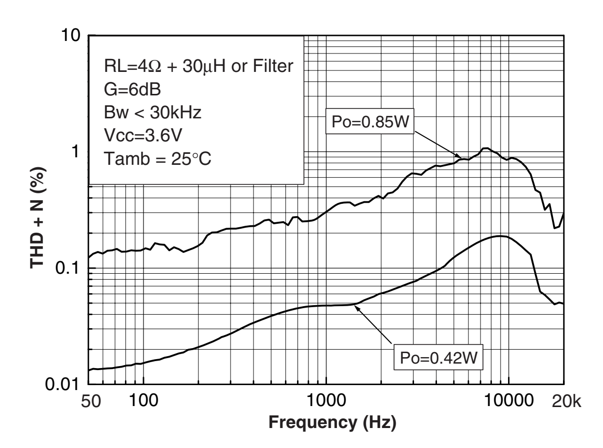


Figure 40. THD+N vs. frequency

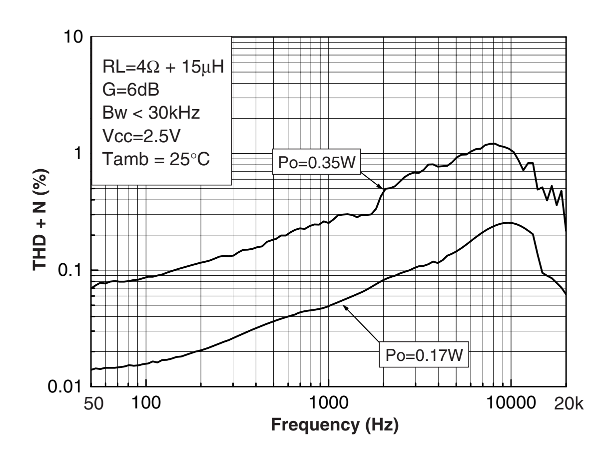


Figure 41. THD+N vs. frequency

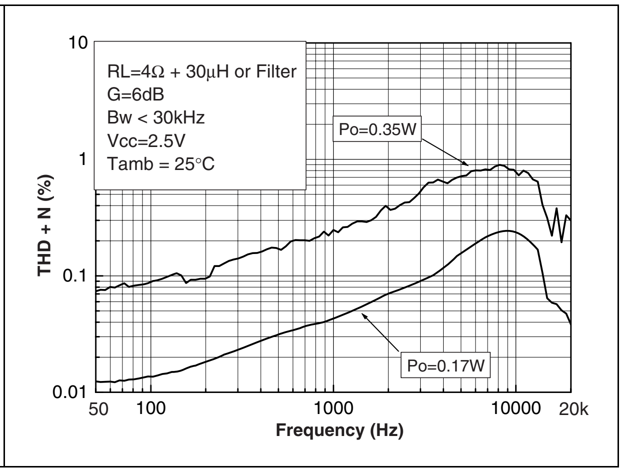


Figure 42. THD+N vs. frequency

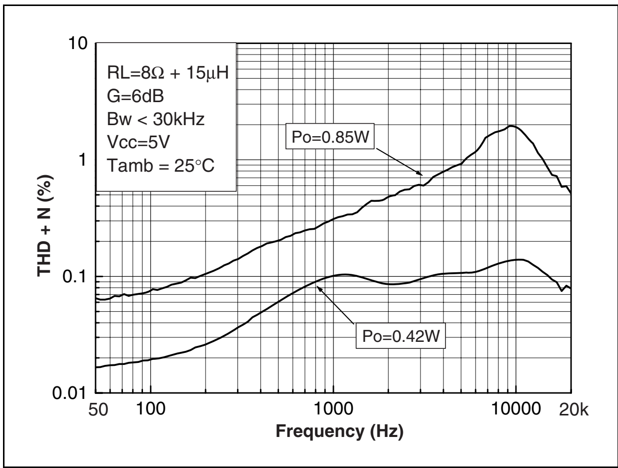


Figure 43. THD+N vs. frequency

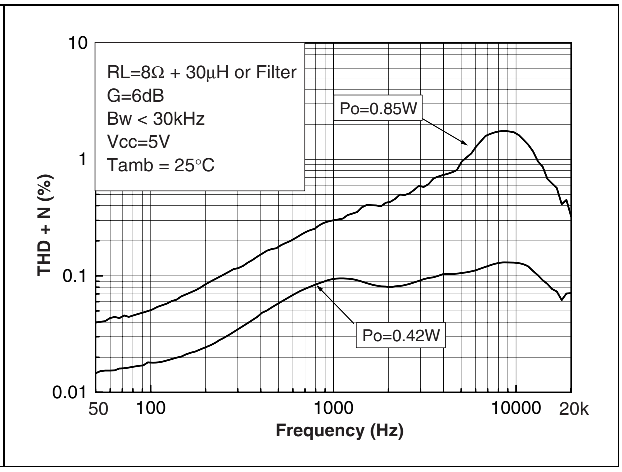


Figure 44. THD+N vs. frequency

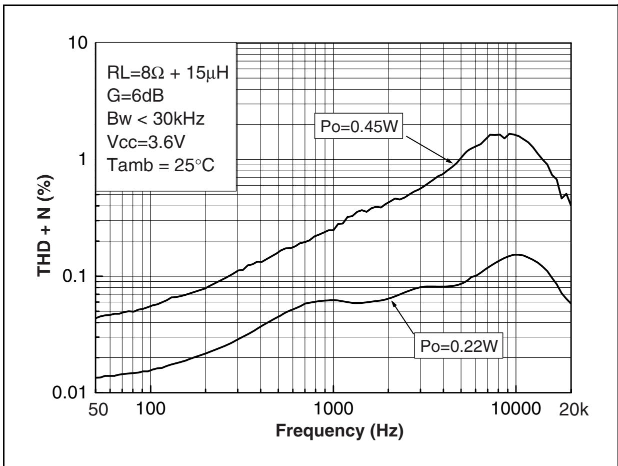


Figure 45. THD+N vs. frequency

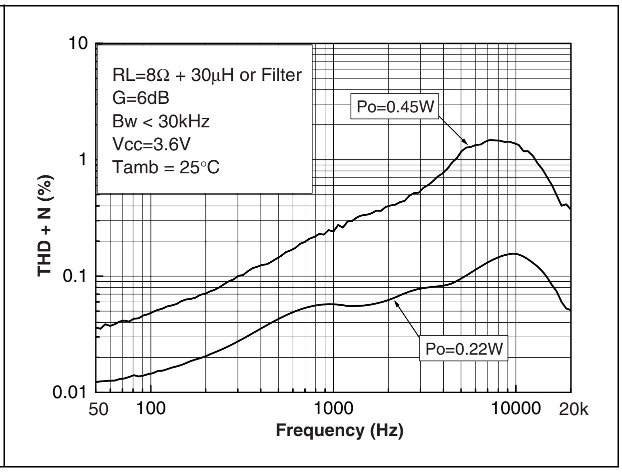


Figure 46. THD+N vs. frequency

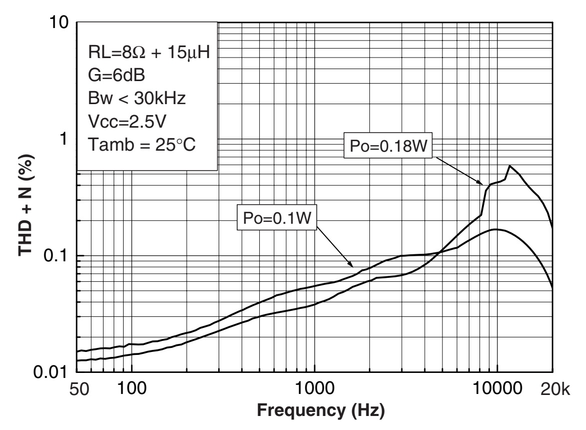


Figure 47. THD+N vs. frequency

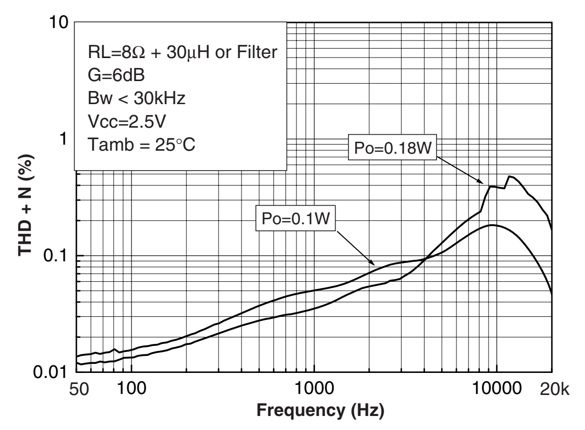


Figure 48. Gain vs. frequency

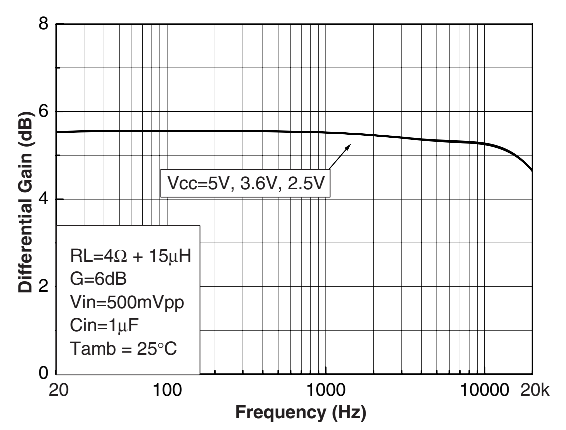


Figure 49. Gain vs. frequency

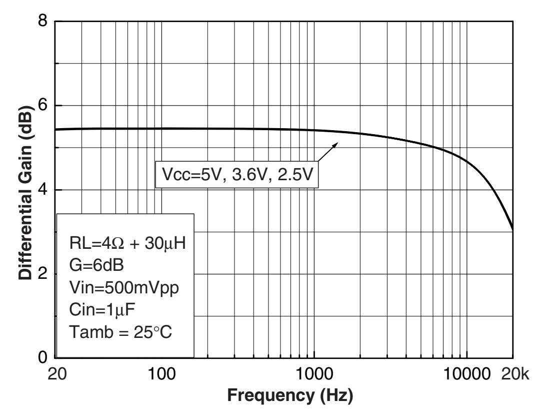


Figure 50. Gain vs. frequency

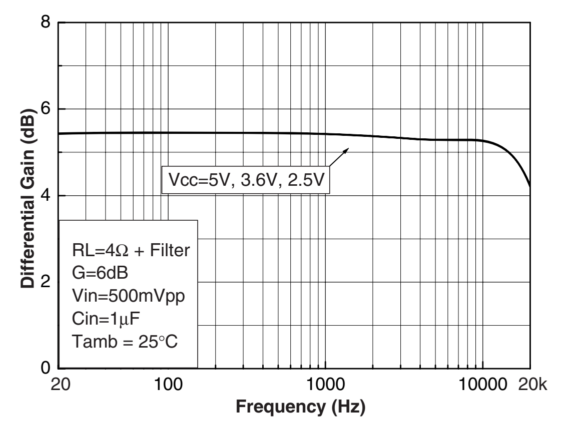


Figure 51. Gain vs. frequency

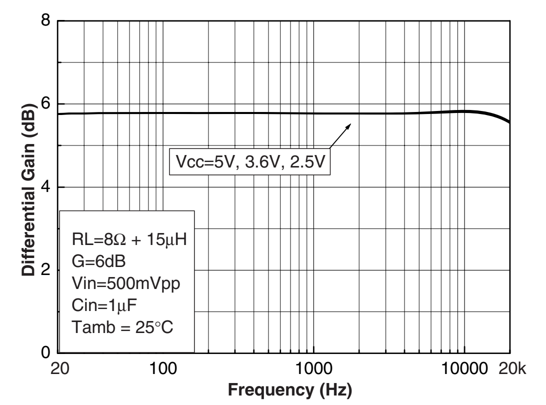


Figure 52. Gain vs. frequency

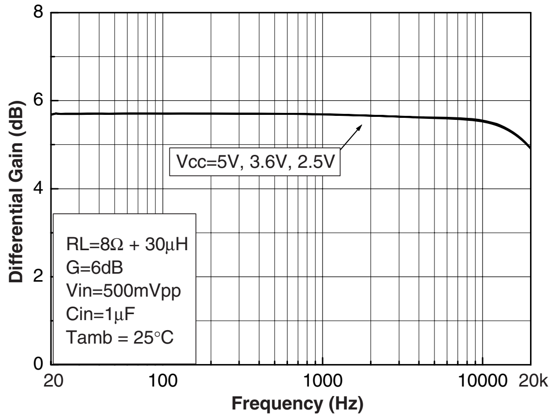


Figure 53. Gain vs. frequency

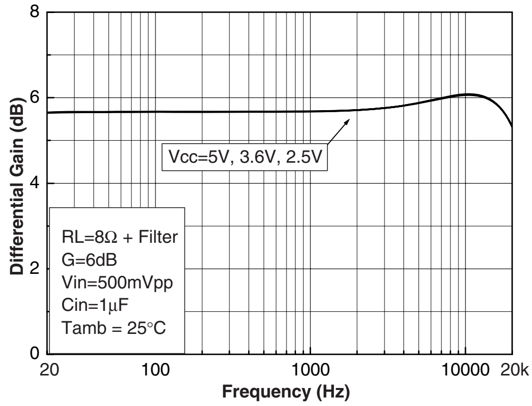


Figure 54. Gain vs. frequency

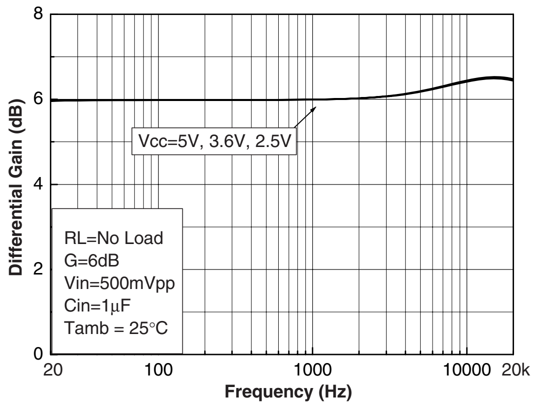


Figure 55. Startup and shutdown times V_{CC} = 5V, G = 6dB, C_{in}= 1µF (5ms/div)

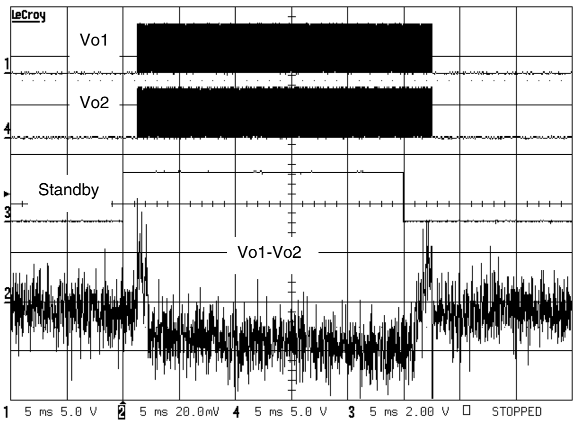


Figure 56. Startup and shutdown times V_{CC} = 3V, G = 6dB, C_{in}= 1µF (5ms/div)

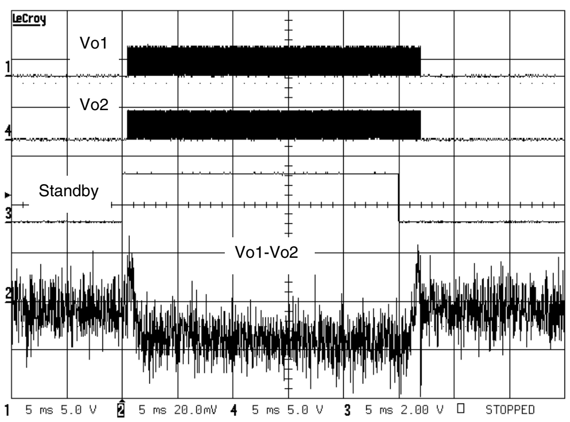


Figure 57. Startup and shutdown times V_{CC} = 5V, G = 6dB, C_{in}= 100nF (5ms/div)

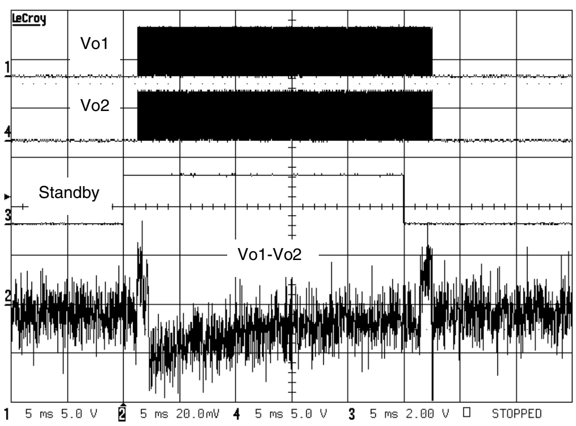


Figure 58. Startup and shutdown times V_{CC} = 3V, G = 6dB, C_{in}= 100nF (5ms/div)

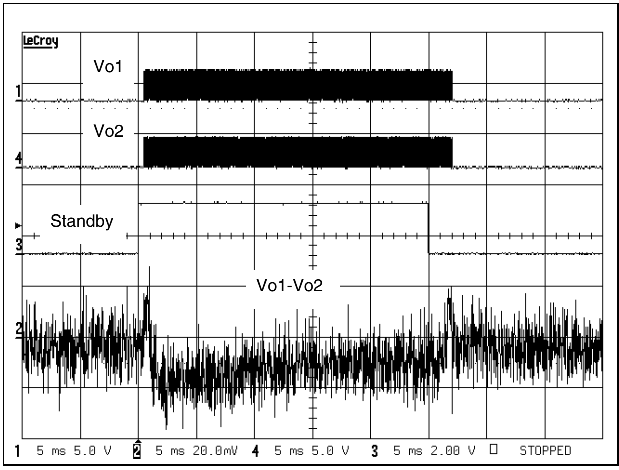


Figure 59. Startup and shutdown times V_{CC} = 5V, G = 6dB, No C_{in} (5ms/div)

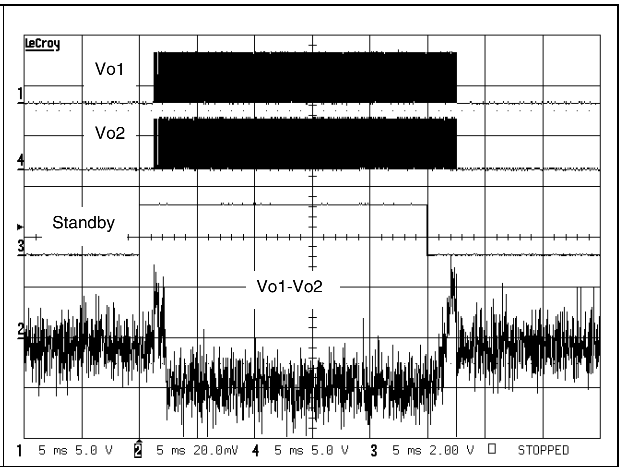
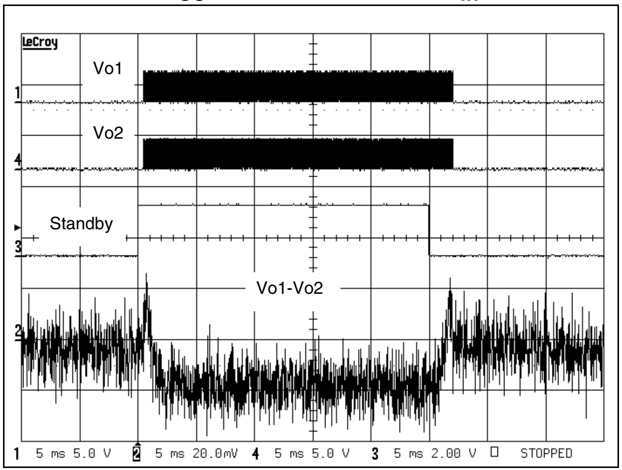


Figure 60. Startup and shutdown times V_{CC} = 3V, G = 6dB, No C_{in} (5ms/div)



4 Application information

4.1 Differential configuration principle

The TS4962 is a monolithic, fully differential input/output class D power amplifier. The TS4962 also includes a common-mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common-mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The advantages of a fully differential amplifier are:

- high PSRR (power supply rejection ratio).
- high common mode noise rejection.
- virtually zero pop without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers.
- easier interfacing with differential output audio DAC.
- no input coupling capacitors required because of common-mode feedback loop.

The main disadvantage is that, since the differential function is directly linked to the external resistor mismatching, particular attention should be paid to this mismatching in order to obtain the best performance from the amplifier.

4.2 Gain in typical application schematic

Typical differential applications are shown in *Figure 1 on page 6*.

In the flat region of the frequency-response curve (no input coupling capacitor effect), the differential gain is expressed by the relation:

$$A_{V_{diff}} = \frac{Out^+ - Out^-}{In^+ - In^-} = \frac{300}{R_{in}}$$

with R_{in} expressed in kΩ.

Due to the tolerance of the internal 150 kΩ feedback resistor, the differential gain is in the range (no tolerance on R_{in}):

$$\frac{273}{R_{in}} \le A_{V_{diff}} \le \frac{327}{R_{in}}$$

4.3 Common-mode feedback loop limitations

As explained previously, the common-mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common-mode bias input voltage.

However, due to a V_{icm} limitation in the input stage (see *Table 3: Operating conditions on page 4*), the common-mode feedback loop can play its role only within a defined range. This range depends upon the values of V_{CC} and R_{in} (A_{Vdiff}). To have a good estimation of the V_{icm} value, we can apply this formula (no tolerance on R_{in}):

$$V_{icm} = \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 150k\Omega}{2 \times (R_{in} + 150k\Omega)} \quad (V)$$

with

$$V_{IC} = \frac{In^{+} + In^{-}}{2} \quad (V)$$

And the result of the calculation must be in the range:

$$0.5V \le V_{icm} \le V_{CC} - 0.8V$$

Due to the +/-9% tolerance on the 150 kΩ resistor, it is also important to check V_{icm} in these conditions.

$$\frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 136.5k\Omega}{2 \times (R_{in} + 136.5k\Omega)} \le V_{icm} \le \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 163.5k\Omega}{2 \times (R_{in} + 163.5k\Omega)}$$

If the result of the V_{icm} calculation is not in the previous range, input coupling capacitors must be used. With V_{CC} between 2.4 and 2.5 V, input coupling capacitors are mandatory.

For example:

With V_{CC} = 3 V, R_{in} = 150 k and V_{IC} = 2.5 V, we typically find V_{icm} = 2 V, which is lower than 3 V-0.8 V = 2.2 V. With 136.5 kΩ we find 1.97 V and with 163.5 kΩ we have 2.02 V. Therefore, no input coupling capacitors are required.

4.4 Low frequency response

If a low frequency bandwidth limitation is requested, it is possible to use input coupling capacitors.

In the low frequency region, C_{in} (input coupling capacitor) starts to have an effect. C_{in} forms, with R_{in}, a first order high-pass filter with a -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2\pi \times R_{in} \times C_{in}} \quad (Hz)$$

So, for a desired cut-off frequency we can calculate C_{in},

$$C_{in} = \frac{1}{2\pi \times R_{in} \times F_{CL}} \quad (F)$$

with R_{in} in Ω and F_{CL} in Hz.

4.5 Decoupling of the circuit

A power supply capacitor, referred to as C_S, is needed to correctly bypass the TS4962.

The TS4962 has a typical switching frequency at 250 kHz and output fall and rise time about 5 ns. Due to these very fast transients, careful decoupling is mandatory.

A 1 µF ceramic capacitor is enough, but it must be located very close to the TS4962 in order to avoid any extra parasitic inductance being created by an overly long track wire. In relation with dI/dt, this parasitic inductance introduces an overvoltage that decreases the global efficiency and, if it is too high, may cause a breakdown of the device.

In addition, even if a ceramic capacitor has an adequate high frequency ESR value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4 Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1 µF/6.3 V capacitor used at 5 V loses about 50% of its value. In fact, with a 5 V power supply voltage, the decoupling value is about 0.5 µF instead of 1 µF. As C_S has particular influence on the THD+N in the medium-high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots, which can be problematic if they reach the power supply AMR value (6 V).

4.6 Wake-up time (t_{WU})

When the standby is released to set the device ON, there is a wait of about 5 ms. The TS4962 has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

4.7 Shutdown time (t_{STBY})

When the standby command is set, the time required to put the two output stages into high impedance and to put the internal circuitry in standby mode is about 5 ms. This time is used to decrease the gain and avoid any pop noise during the shutdown phase.

4.8 Consumption in standby mode

Between the standby pin and GND there is an internal 300 kΩ resistor. This resistor forces the TS4962 to be in standby mode when the standby input pin is left floating.

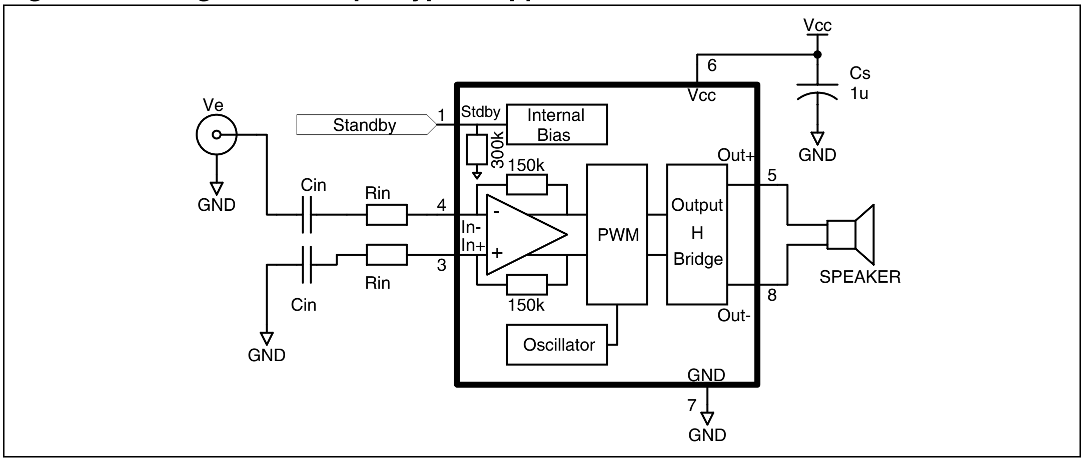
However, this resistor also introduces additional power consumption if the standby pin voltage is not 0 V.

For example, with a 0.4 V standby voltage pin, *Table 3 on page 4* shows that you must add 0.4 V/300 kΩ = 1.3 µA typical (0.4 V/273 kΩ = 1.46 µA maximum) to the standby current specified in *Table 5 on page 5*.

4.9 Single-ended input configuration

It is possible to use the TS4962 in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. *Figure 61* shows a typical single-ended input application.

Figure 61. Single-ended input typical application



All formulas are identical except for the gain with R_{in} in kΩ

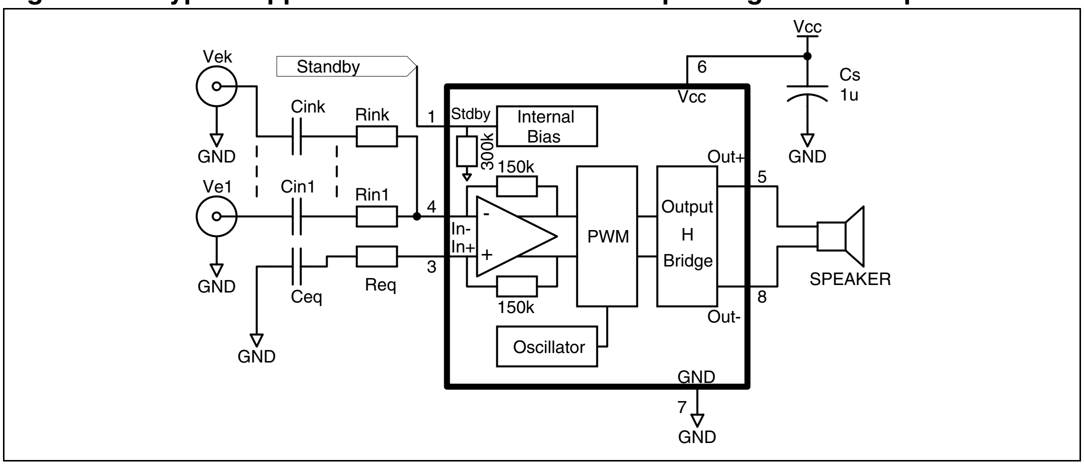
$$A_{V_{single}} = \frac{V_e}{Out^+ - Out^-} = \frac{300}{R_{in}}$$

Due to the internal resistor tolerance we have:

$$\frac{273}{R_{in}} \leq A_{V_{single}} \leq \frac{327}{R_{in}}$$

In the event that multiple single-ended inputs are summed, it is important that the impedance on both TS4962 inputs (In^- and In^+) be equal.

Figure 62. Typical application schematic with multiple single-ended inputs



We have the following equations.

$$\text{Out}^+ - \text{Out}^- = V_{e1} \times \frac{300}{R_{in1}} + \ldots + V_{ek} \times \frac{300}{R_{ink}} \quad (V)$$

$$C_{eq} = \sum_{j=1}^{k} C_{ini}$$

$$C_{ini} = \frac{1}{2 \times \pi \times R_{ini} \times F_{CLi}} \quad (F)$$

$$R_{eq} = \frac{1}{\sum_{j=1}^{k} \frac{1}{R_{ini}}}$$

In general, for mixed situations (single-ended and differential inputs) it is best to use the same rule, that is, equalize impedance on both TS4962 inputs.

4.10 Output filter considerations

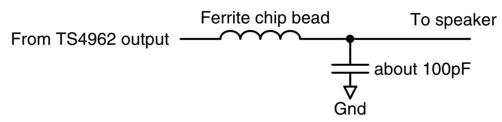
The TS4962 is designed to operate without an output filter. However, due to very sharp transients on the TS4962 output, EMI-radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS4962 outputs and the loudspeaker terminal is long (typically more than 50 mm, or 100 mm in both directions, to the speaker terminals). As the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow.

- Reduce, as much as possible, the distance between the TS4962 output pins and the speaker terminals.
- Use ground planes for "shielding" sensitive wires.
- Place, as close as possible to the TS4962 and in series with each output, a ferrite bead with a rated current of at least 2.5 A and an impedance greater than 50 Ω at frequencies above 30 MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit.
- Allow enough footprint to place, if necessary, a capacitor to short perturbations to ground (see *Figure 63*).

Figure 63. Method for shorting perturbations to ground

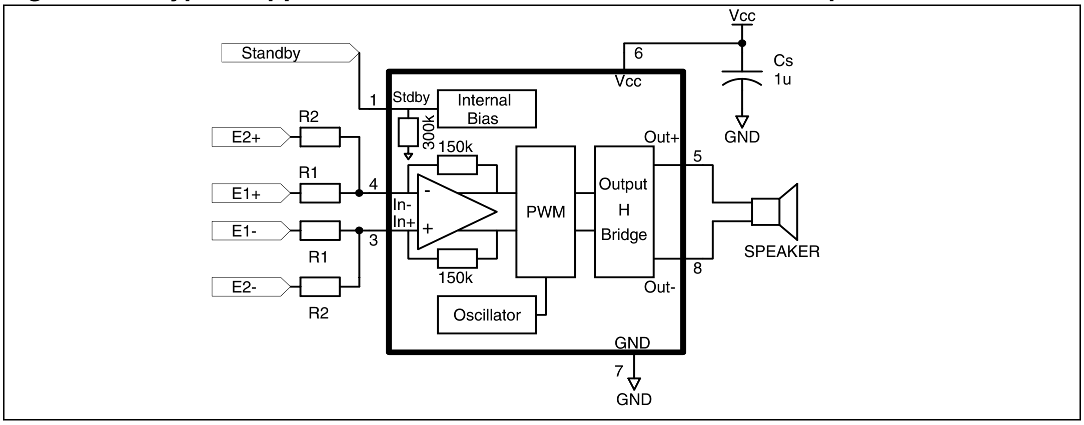


In the case where the distance between the TS4962 output and the speaker terminals is high, it is possible to observe low frequency EMI issues due to the fact that the typical operating frequency is 250 kHz. In this configuration, we recommend using an output filter (as represented in *Figure 1 on page 6*). It should be placed as close as possible to the device.

4.11 Several examples with summed inputs

4.11.1 Example 1: dual differential inputs

Figure 64. Typical application schematic with dual differential inputs



With (R_i in kΩ):

$$A_{V_1} = \frac{Out^+ - Out^-}{E_1^+ - E_1^-} = \frac{300}{R_1}$$

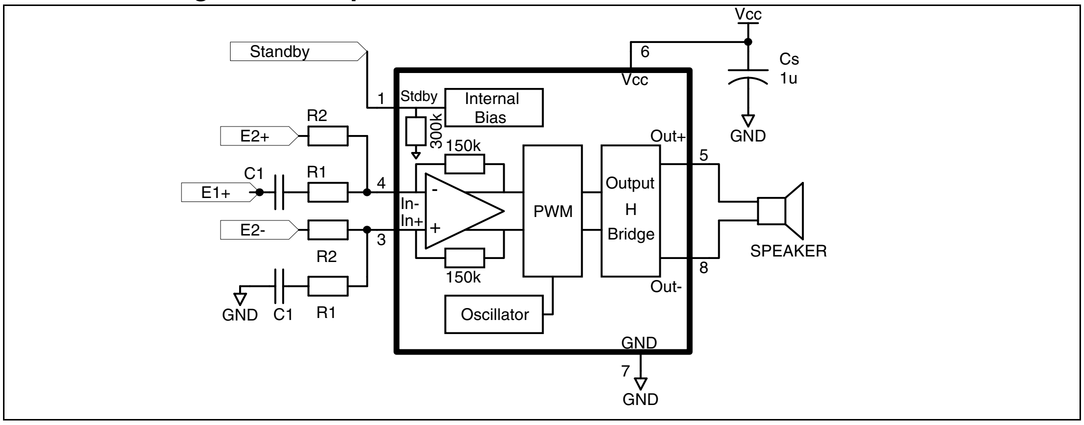
$$A_{V_2} = \frac{Out^+ - Out^-}{E_2^+ - E_2^-} = \frac{300}{R_2}$$

$$0.5V \le \frac{V_{CC} \times R_1 \times R_2 + 300 \times (V_{IC1} \times R_2 + V_{IC2} \times R_1)}{300 \times (R_1 + R_2) + 2 \times R_1 \times R_2} \le V_{CC} - 0.8V$$

$$V_{IC_1} = \frac{E_1^+ + E_1^-}{2} \text{ and } V_{IC_2} = \frac{E_2^+ + E_2^-}{2}$$

4.11.2 Example 2: one differential input plus one single-ended input

Figure 65. Typical application schematic with one differential input and one single-ended input



With (R_i in kΩ) :

$$A_{V_1} = \frac{Out^+ - Out^-}{E_1^+} = \frac{300}{R_1}$$

$$A_{V_2} = \frac{Out^+ - Out^-}{E_2^+ - E_2^-} = \frac{300}{R_2}$$

$$C_1 = \frac{1}{2\pi \times R_1 \times F_{CL}} \quad (F)$$

5 Demonstration board

A demonstration board for the TS4962 is available. For more information about this demonstration board, refer to the application note AN2406 "TS4962IQ class D audio amplifier evaluation board user guidelines" available on *www.st.com*.

Figure 66. Schematic diagram of mono class D demonstration board for the TS4962 DFN package

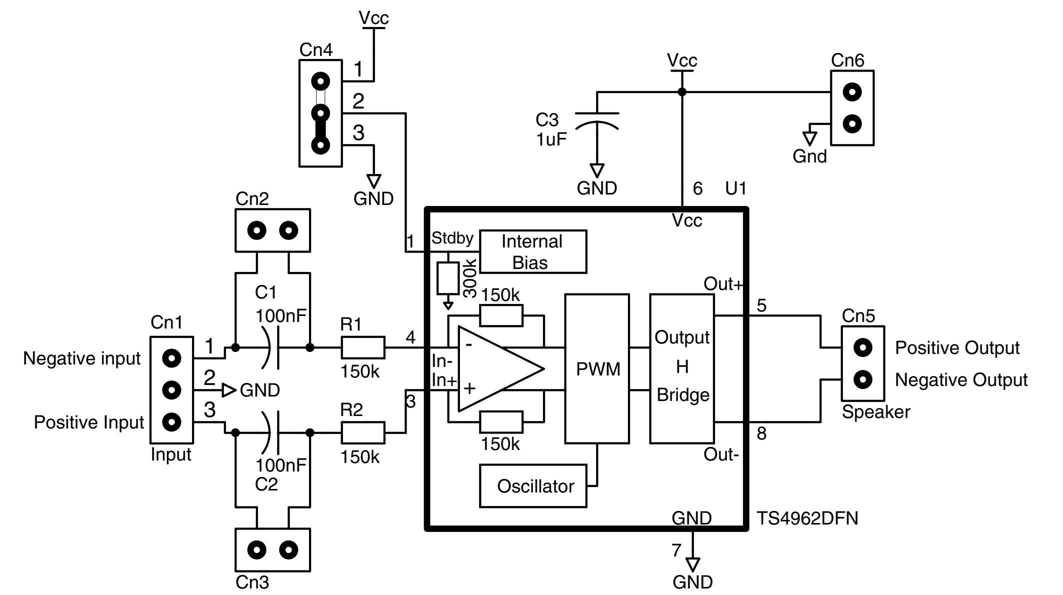


Figure 67. Top view

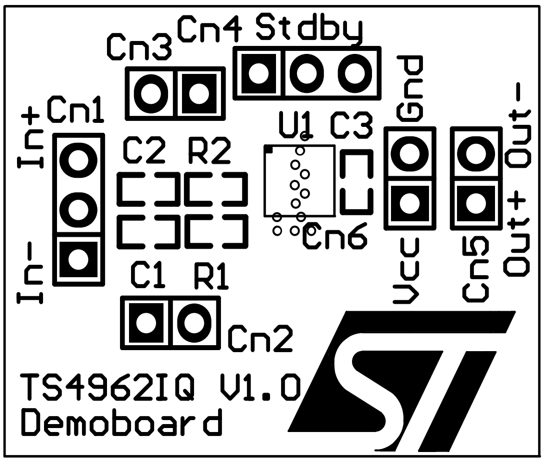


Figure 68. Bottom layer

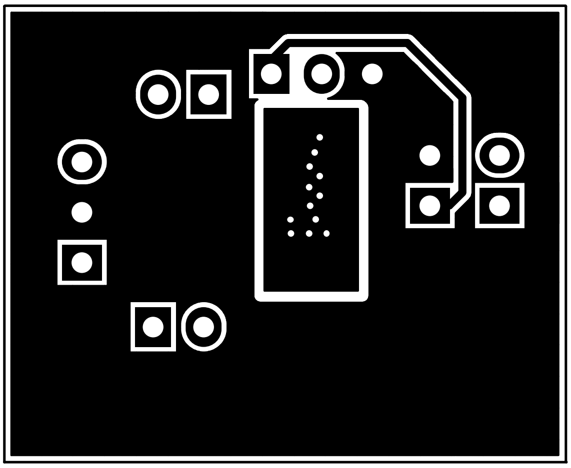
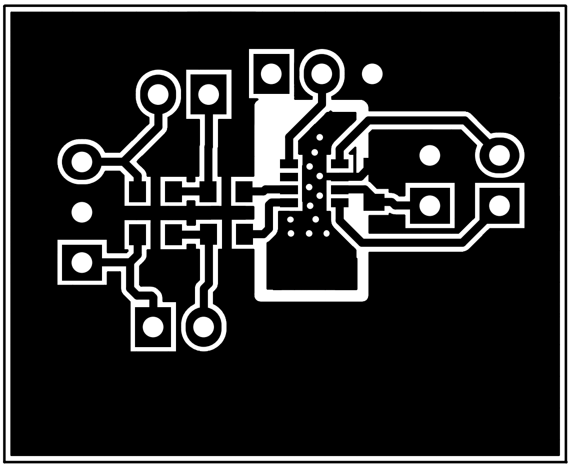
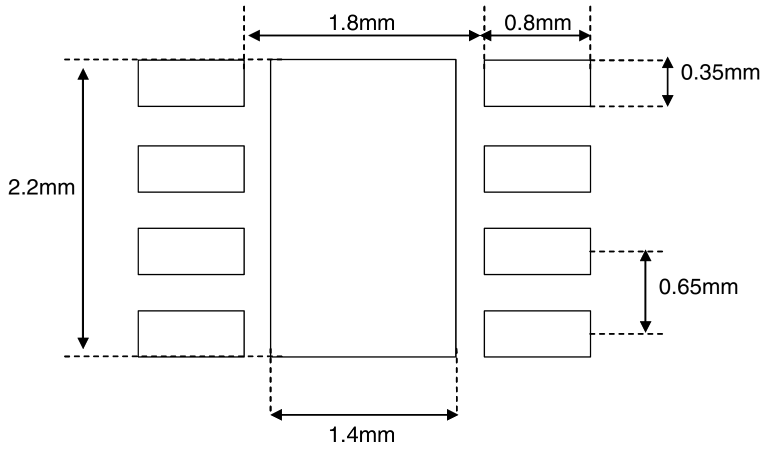


Figure 69. Top layer



6 Recommended footprint

Figure 70. Recommended footprint for TS4962 DFN package



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 71. DFN8 3 x 3 exposed pad package mechanical drawing (pitch 0.65 mm)

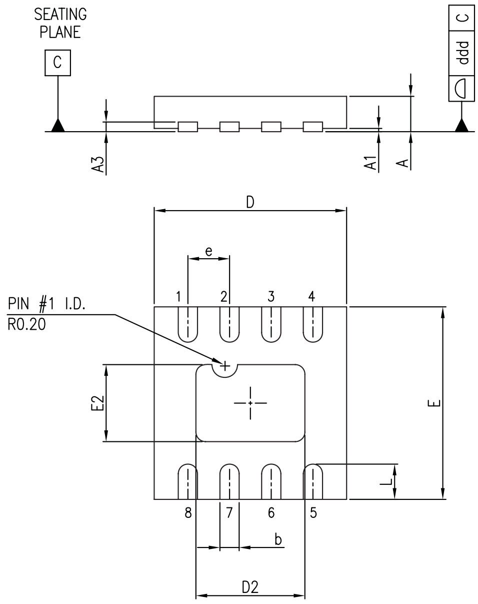


Table 12. DFN8 3 x 3 exposed pad package mechanical data (pitch 0.65 mm)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.60	0.65	0.020	0.024	0.026
A1		0.02	0.05		0.0008	0.002
A3			0.22			0.009
b	0.25	0.30	0.35	0.010	0.012	0.014
D	2.85	3.00	3.15	0.112	0.118	0.124
D2	1.60	1.70	1.80	0.063	0.067	0.071
E	2.85	3.00	3.15	0.112	0.118	0.124
E2	1.10	1.20	1.30	0.043	0.047	0.051
e		0.65			0.026	
L	0.50	0.55	0.60	0.020	0.022	0.024
ddd			0.08			0.003

Note: 1 *The pin 1 identifier must be visible on the top surface of the package by using an indentation mark or other feature of the package body. Exact shape and size of this feature are optional.*

2 *The dimension L does not conform with JEDEC MO-248, which recommends 0.40+/-0.10 mm.*

For enhanced thermal performance, the exposed pad must be soldered to a copper area on the PCB, acting as a heatsink. This copper area can be electrically connected to pin 7 or left floating.

8 Ordering information

Table 13. Order codes

Part number	Temperature range	Package	Packaging	Marking
TS4962IQT	-40°C, +85°C	DFN8	Tape & reel	K962

9 Revision history

Table 14. Document revision history

Date	Revision	Changes
31-May-2006	5	Modified package information. Now includes only standard DFN8 package.
16-Oct-2006	6	Added curves in *Section 3: Electrical characteristics*. Added evaluation board information in *Section 5: Demonstration board*. Added recommended footprint.
10-Jan-2007	7	Added paragraph about rated voltage of capacitor in *Section 4.5: Decoupling of the circuit*.
18-Jan-2010	8	Added *Table 5: Pin description*.