0.7-Ω DUAL SPDT ANALOG SWITCH WITH NEGATIVE RAIL CAPABILITY AND 1.8-V COMPATIBLE INPUT LOGIC

Check for Samples: TS5A22366

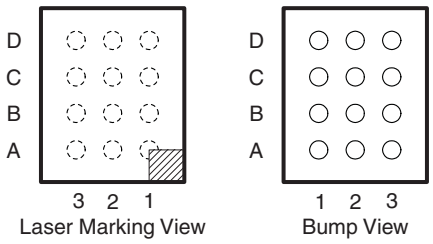
FEATURES

- **Negative Signaling Capability: Maximum Swing From –2.75 V to 2.75 V (V_+ = 2.75 V)**
- **Low ON-State Resistance (0.7 Ω Typ)**
- **Excellent ON-State Resistance Matching**
- **1.8-V Compatible Control Input Threshold Independent of V_+**
- **Control Inputs Are 5.5-V Tolerant**
- **2.25-V to 5.5-V Power Supply (V_+)**
- **Low Charge Injection**
- **Specified Break-Before-Make Switching**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2500-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
  - **200-V Machine Model (A115-A)**

APPLICATIONS

- **Cell Phones**
- **PDAs**
- **Portable Instrumentation**
- **Audio Routing**
- **Portable Media Players**

YFC PACKAGE



YFC PACKAGE TERMINAL ASSIGNMENTS

D	NC1	V_+	NC2
C	COM1	GND	COM2
B	NO1	GND	NO2
A	IN1	N.C.(1)	IN2
	1	**2**	**3**

(1) N.C. –No internal connection

DESCRIPTION

The TS5A22366 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device features negative signal capability that allows signals below ground to pass through the switch without distortion.

The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

The TS5A22366 is available is a ultra small 1.6 mm × 1.2 mm wafer-chip-scale package (WCSP) (0.4 mm pitch).

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

Table 1. SUMMARY OF CHARACTERISTICS

V_+ = 3.3 V, T_A = 25°C

Configuration	2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance (r_{on})	0.8 Ω
ON-state resistance match (Δr_{on})	0.08 Ω
ON-state resistance flatness ($r_{ON(flat)}$)	0.3 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	199 ns/182 ns
Break-before-make time (t_{BBM})	7.1 ns
Charge injection (Q_C)	120 pC
Bandwidth (BW)	32 MHz
OFF isolation (O_{ISO})	–70 dB at 100 kHz
Crosstalk (X_{TALK})	–70 dB at 100 kHz
Total harmonic distortion (THD)	0.01%
Package option	12-pin WCSP (YFC)

Table 2. FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

APPLICATION BLOCK DIAGRAM

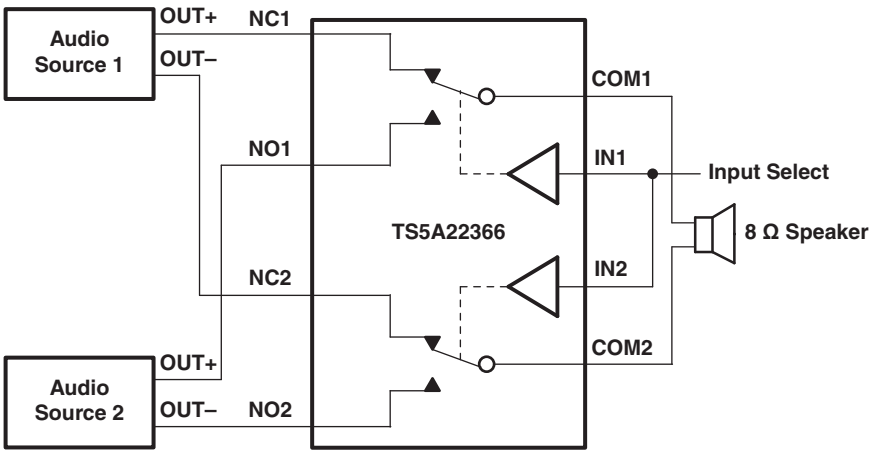


Figure 1. TS5A22366 Application Block Diagram

Negative Signaling Capacity

The TS5A22366 dual SPDT switch features negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single +2.3-V to +5.5-V supply. The input/output signal swing of the device is dependant of the supply voltage V_+: the devices pass signals as high as V_+ and as low as V_+ – 5.5 V, including signals below ground with minimal distortion.

Table 3 shows the input/output signal swing the user can get with different supply voltages.

Table 3. Input/Output Signal Swing

SUPPLY VOLTAGE, V+	MINIMUM (V_{NC}, V_{NO}, V_{COM}) = V_+ – 5.5	MAXIMUM (V_{NC}, V_{NO}, V_{COM}) = V_+
5.5 V	0 V	5.5 V
4.2 V	–1.3 V	4.2 V
3.3 V	–2.2 V	3.3 V
3 V	–2.5 V	3 V
2.5 V	–3 V	2.5 V

ABSOLUTE MINIMUM AND MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(3) (4) (5)		V_+ – 6	V_+ + 0.5	V
I_K	Analog port diode current(6)	$V_+ < V_{NC}, V_{NO}, V_{COM} < 0$	–50	50	V
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–150	150	mA
	ON-state peak switch current(7)		–300	300	
V_I	Digital input voltage range		–0.5	6.5	V
I_{IK}	Digital input clamp current(3) (4)	$V_{IO} < V_I < 0$	–50		mA
I_{GND} I_+	Continuous current through V_+or GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Requires clamp diodes on analog port to V_+.
(7) Pulse at 1-ms duration <10% duty cycle

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance(1)	YFC package	106.2	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1)

V_+ = 2.25 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					V_+ – 5.5		V_+	Ω
ON-state resistance	r_{on}	V_{NC} or V_{NO} = V_+, 1.5 V, V_+ – 5.5 V I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	2.25 V		1	1.8	Ω
				Full				2	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	2.25 V		0.05	1	Ω
				Full				1	
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} or V_{NO} = V_+, 1.5 V, V_+ – 5.5 V I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	2.25 V		0.53	1.5	Ω
				Full				1.6	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} = 2.25, V_+ – 5.5 V V_{COM} = V_+ – 5.5 V, 2.25, V_{NO} = Open, or V_{NO} = 2.25, V_+ – 5.5 V V_{COM} = V_+ – 5.5 V, 2.25, V_{NC} = Open,	Switch OFF, See Figure 16	25°C	2.7 V	–50		50	nA
				Full		–375		375	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = Open, V_{COM} = V_+,V_+ – 5.5 V,	See Figure 17	25°C	2.7 V	–50		50	nA
				Full		–375		375	
Digital Control Inputs (IN, EN)(2)									
Input logic high	V_{IH}			Full		1.05		5.5	V
Input logic low	V_{IL}			Full				0.65	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 1.8 V or GND		25°C	2.7 V	–700		700	nA
				Full		–700		700	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1) (continued)

V_+ = 2.25 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V		193	297	ns
				Full	2.25 V to 2.7 V			350	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V			266	ns
				Full	2.25 V to 2.7 V			320	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2 R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	2.5 V	1	15.6		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 24	25°C	2.5 V		91		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	2.5 V		51		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	2.5 V		181		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	2.5 V		181		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 18	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 20	25°C	2.5 V		32		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, Switch OFF, See Figure 22	f = 100 kHz,	25°C	2.5 V		–70		dB
			f = 1 MHz,				–50		
			f = 5 MHz,				–35		
Crosstalk	X_{TALK}	R_L = 50 Ω, Switch ON, See Figure 23	f = 100 kHz,	25°C	2.5 V		–70		dB
			f = 1 MHz,				–50		
			f = 5 MHz,				–35		
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	2.5 V		0.02		%
Supply									
Positive supply current	I_+	V_I = 1.8 V or GND,		Full	2.7 V		6	12	µA

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}, V_{NC}				V_+ – 5.5		V_+	Ω
ON-state resistance	r_{on}	V_{NC} or V_{NO} ≤ V_+, 1.5 V, V_+ – 5.5 V, I_{COM} = –100 mA, Switch ON, See Figure 15	25°C	3 V		0.8	1.3	Ω
			Full				1.53	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA, Switch ON, See Figure 15	25°C	3 V		0.08	0.17	Ω
			Full				0.3	
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} or V_{NO} ≤ V_+, 1.5 V, V_+ – 5.5 V, I_{COM} = –100 mA, Switch ON, See Figure 16	25°C	3 V		0.3	0.65	Ω
			Full				0.75	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} = 3, V_+ – 5.5 V, V_{COM} = V_+ – 5.5 V, 3, V_{NO} = Open, or V_{NO} = 3 , V_+ – 5.5 V, V_{COM} = V_+ – 5.5 V, 3, V_{NC} = Open, Switch OFF, See Figure 16	25°C	3.6 V	–50		50	nA
			Full		–375		375	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = Open, V_{COM} = V_+,V_+ – 5.5 V, Switch ON, See Figure 17	25°C	3.6 V	–50		50	nA
			Full		–375		375	
Digital Control Inputs (IN, EN)(2)								
Input logic high	V_{IH}		Full		1.05		5.5	V
Input logic low	V_{IL}		Full				0.65	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 1.8 V or GND	25°C	3.6 V	–920		920	nA
			Full		–920		920	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1) (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V		199	313	ns
				Full	3 V to 3.6 V			370	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V		182	289.9	ns
				Full	3 V to 3.6 V			350	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2 R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	3.3 V	1	7.1		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 24	25°C	3.3 V		120		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or V_+ – 5.5 V, Switch OFF,	See Figure 18	25°C	3.3 V		50		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 18	25°C	3.3 V		180		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	3.3 V		180		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 18	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 20	25°C	3.3 V		32		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, Switch OFF, See Figure 22	f = 100 kHz,	25°C	3.3 V		–70		dB
			f = 1 MHz,				–50		
			f = 5 MHz,				–35		
Crosstalk	X_{TALK}	R_L = 50 Ω, Switch ON, See Figure 23	f = 100 kHz,	25°C	3.3 V		–70		dB
			f = 1 MHz,				–50		
			f = 5 MHz,				–35		
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	3.3 V		0.01		%
Supply									
Positive supply current	I_+	V_I = 1.8 V or GND		Full	3.6 V		6	13	µA

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					V_+ – 5.5		V_+	Ω
ON-state resistance	r_{on}	VNC or VNO = V+, 1.5V, V+ -5.5V I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	4.5 V		0.7	1	Ω
				Full				1.36	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	4.5 V		0.1	0.2	Ω
				Full				0.3	
ON-state resistance flatness	$r_{on(flat)}$	VNC or VNO = V+, 1.5V, V+ -5.5V I_{COM} = –100 mA,	Switch ON, See Figure 16	25°C	4.5 V		0.135	0.37	Ω
				Full				0.51	
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} = 4.5, V_+ – 5.5 V V_{COM} = V_+ – 5.5 V, 4.5, V_{NO} = Open, or V_{NO} = 4.5, V_+ – 5.5 V V_{COM} = V_+ – 5.5 V, 4.5, V_{NC} = Open,	Switch OFF, See Figure 16	25°C	5.5 V	–50		50	nA
				Full		–375		375	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = Open, V_{COM} = V_+,V_+ – 5.5 V,	Switch ON, See Figure 17	25°C	5.5 V	–50		50	nA
				Full		–375		375	
Digital Control Inputs (IN, EN)(2)									
Input logic high	V_{IH}			Full		1.05		5.5	V
Input logic low	V_{IL}			Full				0.65	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = 1.8 V or 0		25°C	5.5 V	–1.5		1.5	µA
				Full		–1.5		1.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY(1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 19	25°C	5 V		230	374	ns
				Full	4.5 V to 5.5 V			470	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 19	25°C	5 V		206	325	ns
				Full	4.5 V to 5.5 V			380	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2 R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	3.3 V	1	3		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 24	25°C	5 V		168		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or V_+ – 5.5 V, Switch OFF,	See Figure 18	25°C	5 V		48		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or V_+ – 5.5 V, Switch ON,	See Figure 18	25°C	5 V		176		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 18	25°C	5 V		176		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 18	25°C	5 V		3		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 20	25°C	5 V		32		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, Switch OFF, See Figure 22	f = 100 kHz	25°C	5 V		–70		dB
			f = 1 MHz				–50		
			f = 5 MHz				–35		
Crosstalk	X_{TALK}	R_L = 50 Ω, Switch ON, See Figure 23	f = 100 kHz	25°C	5 V		–70		dB
			f = 1 MHz				–50		
			f = 5 MHz				–35		
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 25	25°C	5 V		0.01		%
Supply									
Positive supply current	I_+	V_I = 1.8 V or GND		Full	5.5 V		7	14	µA

TYPICAL PERFORMANCE

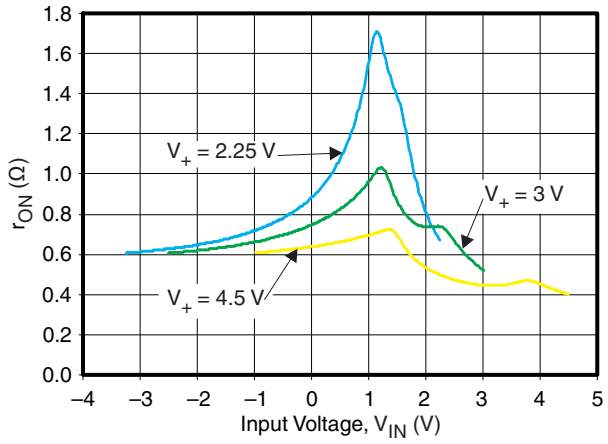


Figure 2. r_{on} vs V_{IN}

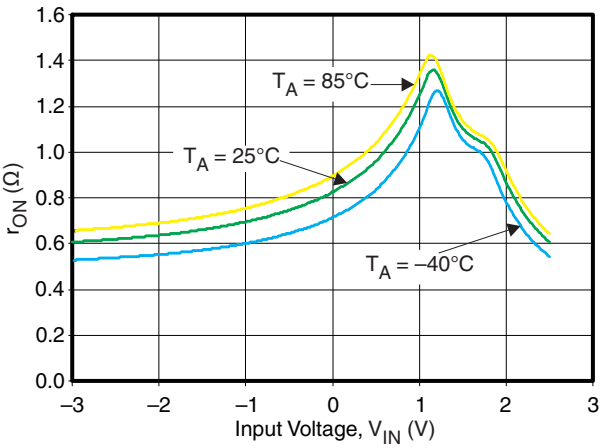


Figure 3. r_{on} vs V_{IN} (V_+ = 2.5 V)

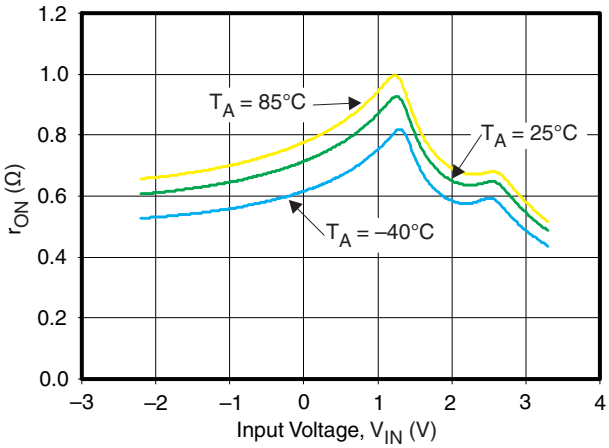


Figure 4. r_{on} vs V_{IN} (V_+ = 3.3 V)

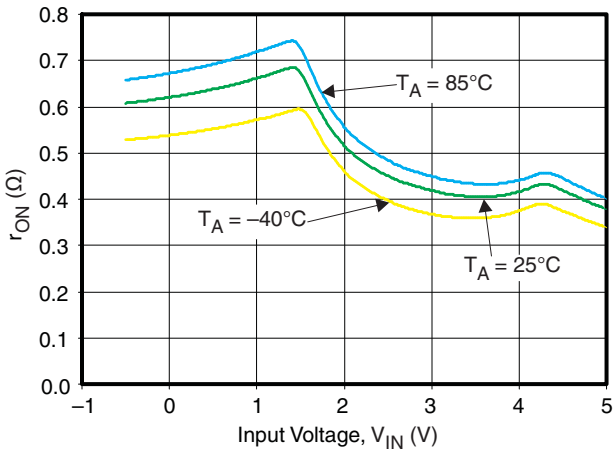


Figure 5. r_{on} vs V_{IN} (V_+ = 5 V)

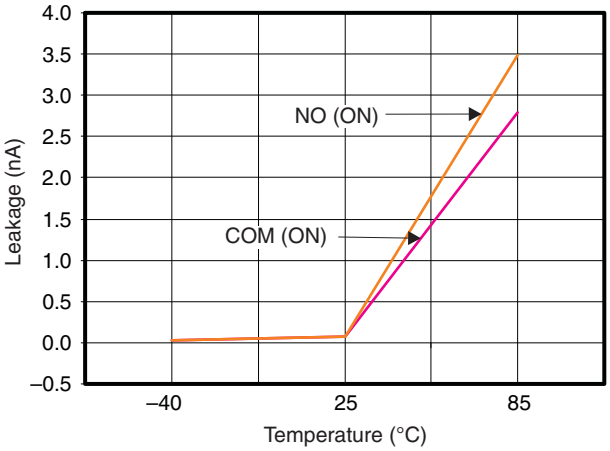


Figure 6. Leakage Current vs Temperature

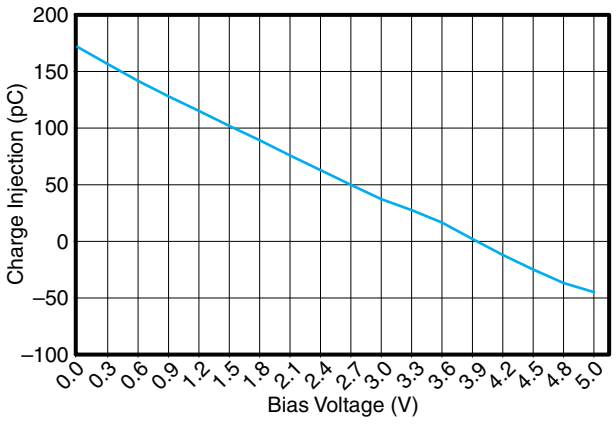


Figure 7. Charge Injection (Q_C) vs V_{COM}(V_+ = 5 V)

TYPICAL PERFORMANCE (continued)

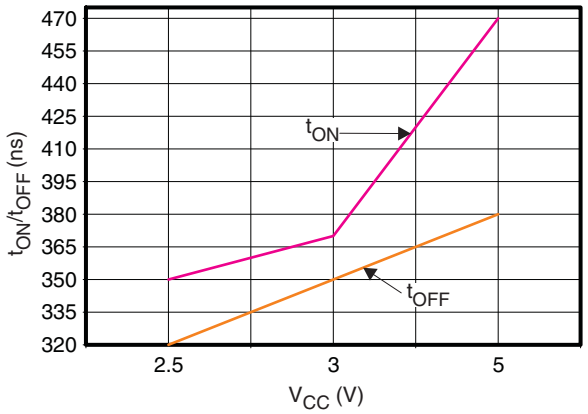


Figure 8. t_{ON} and t_{OFF} vs Supply Voltage

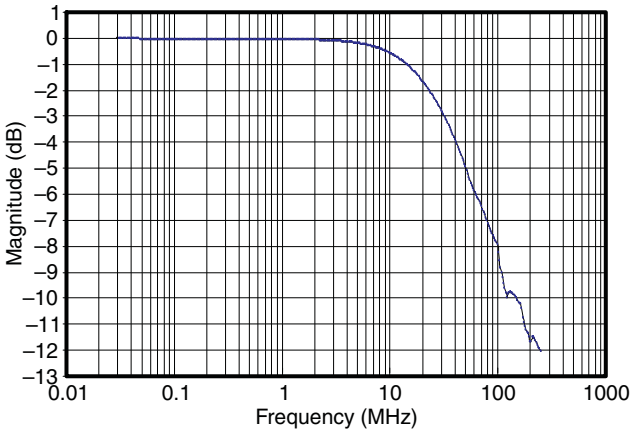


Figure 9. Bandwidth (V_+ = 2.5 V)

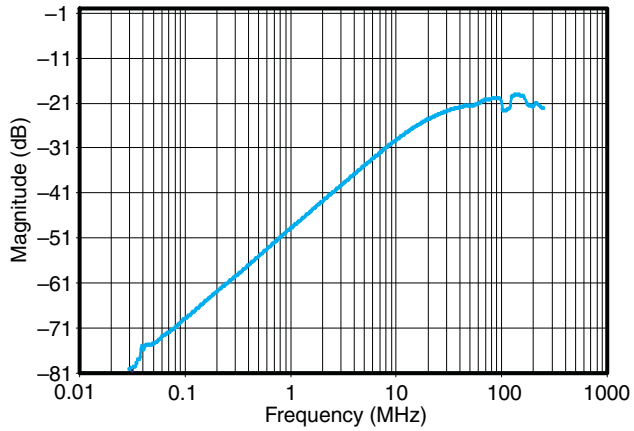


Figure 10. OFF Isolation vs Frequency

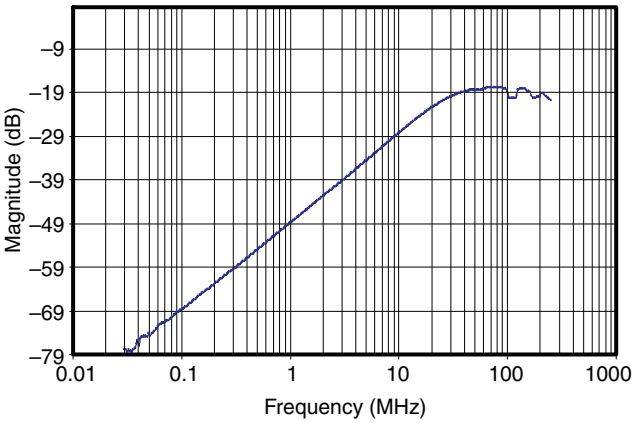


Figure 11. Crosstalk (V_+ = 3.3 V)

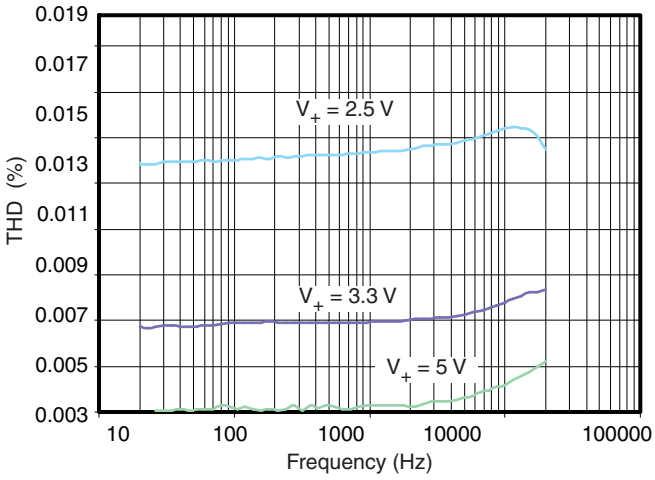


Figure 12. Total Harmonic Distortion vs Frequency

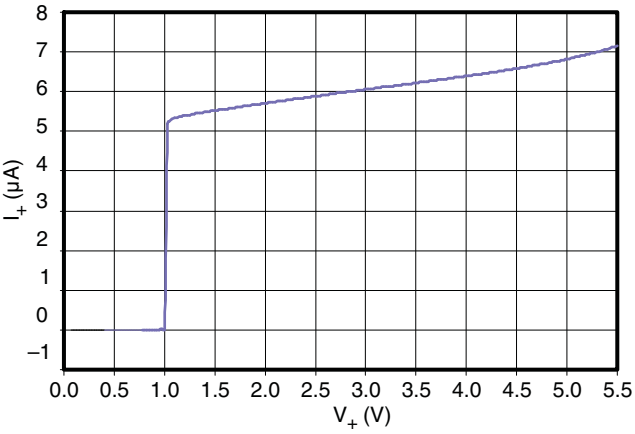


Figure 13. Power-Supply Current vs V_+

TYPICAL PERFORMANCE (continued)

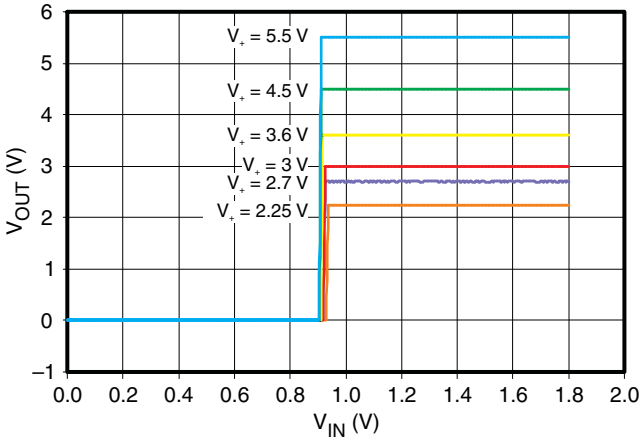


Figure 14. Control Input Thresholds

PARAMETER MEASUREMENT INFORMATION

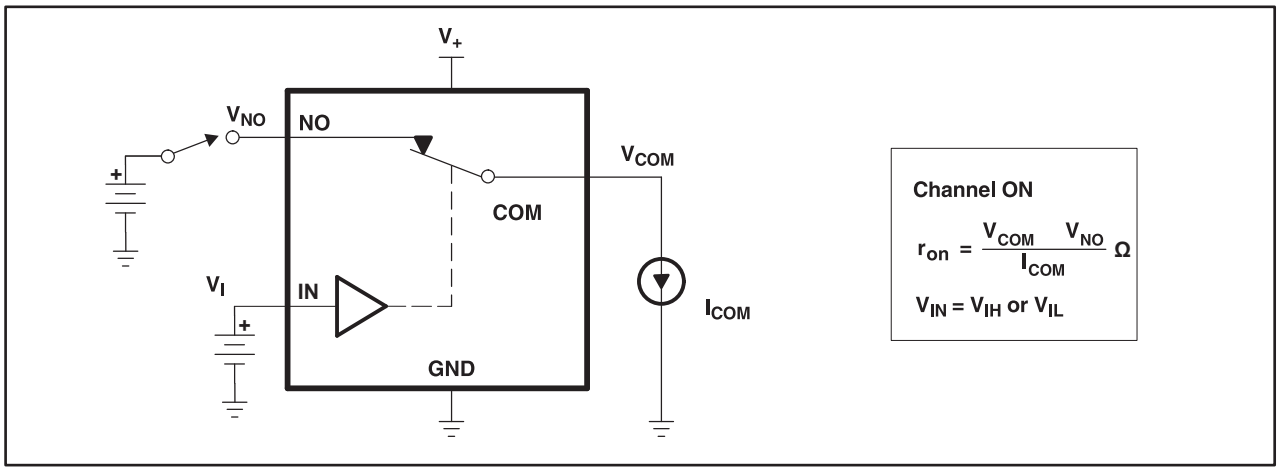


Figure 15. ON-state Resistance (r_{ON})

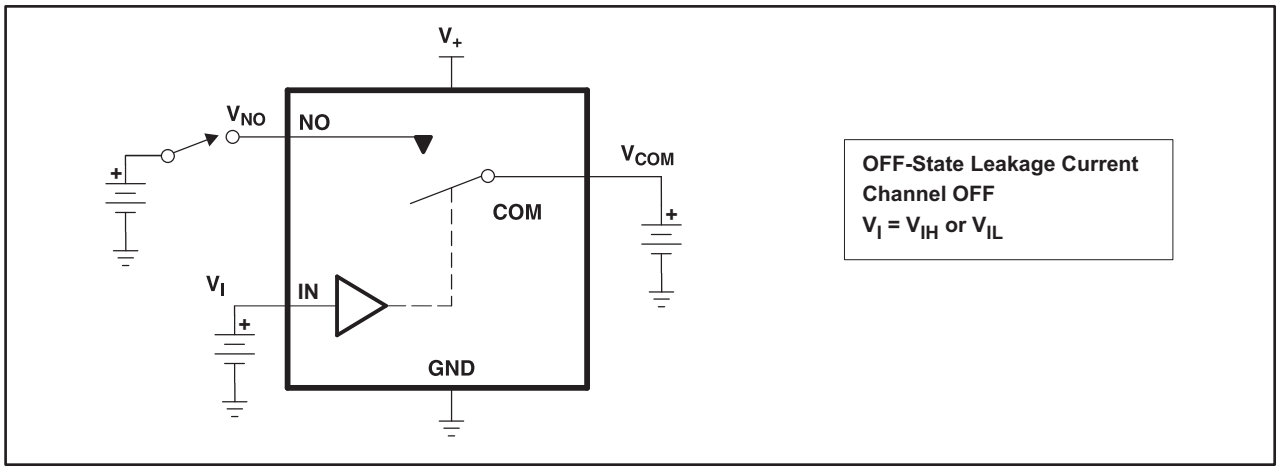


Figure 16. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

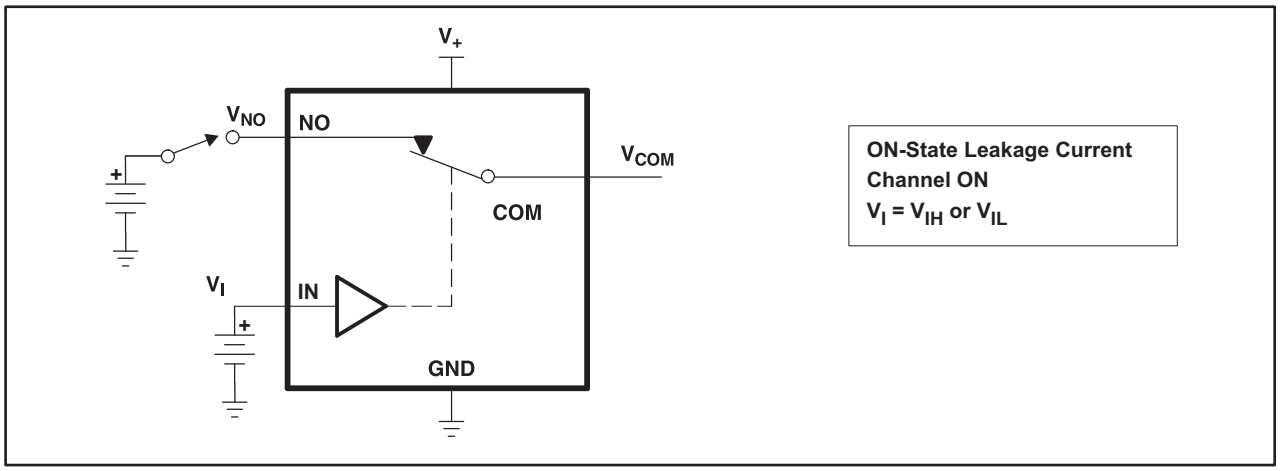


Figure 17. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

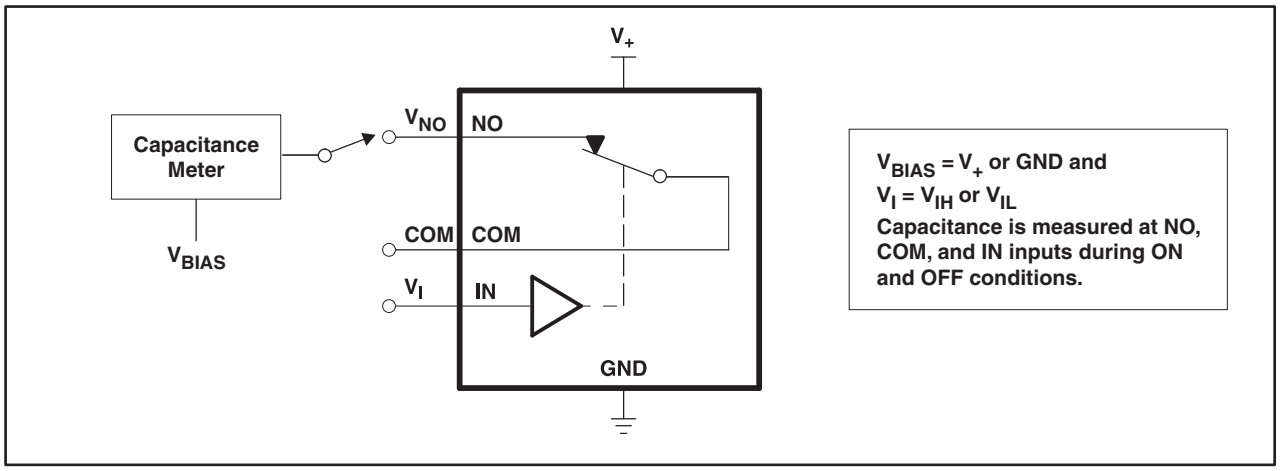
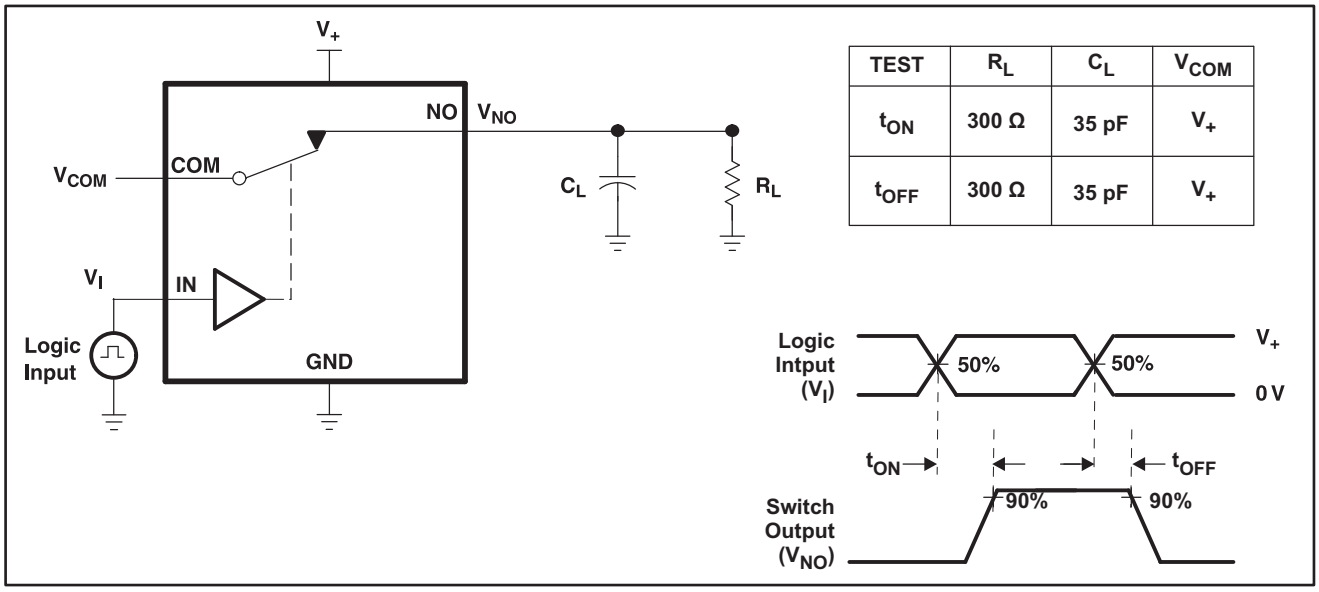


Figure 18. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)



TEST	R_L	C_L	V_{COM}
t_{ON}	300 Ω	35 pF	V_+
t_{OFF}	300 Ω	35 pF	V_+

Figure 19. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

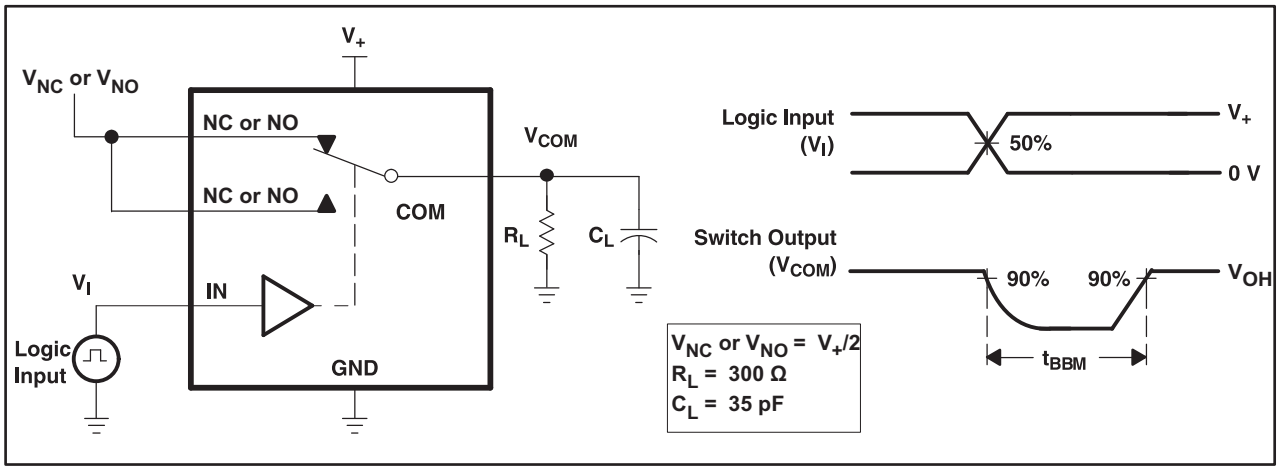


Figure 20. Break-Before-Make Time (t_{BBM})

PARAMETER MEASUREMENT INFORMATION (continued)

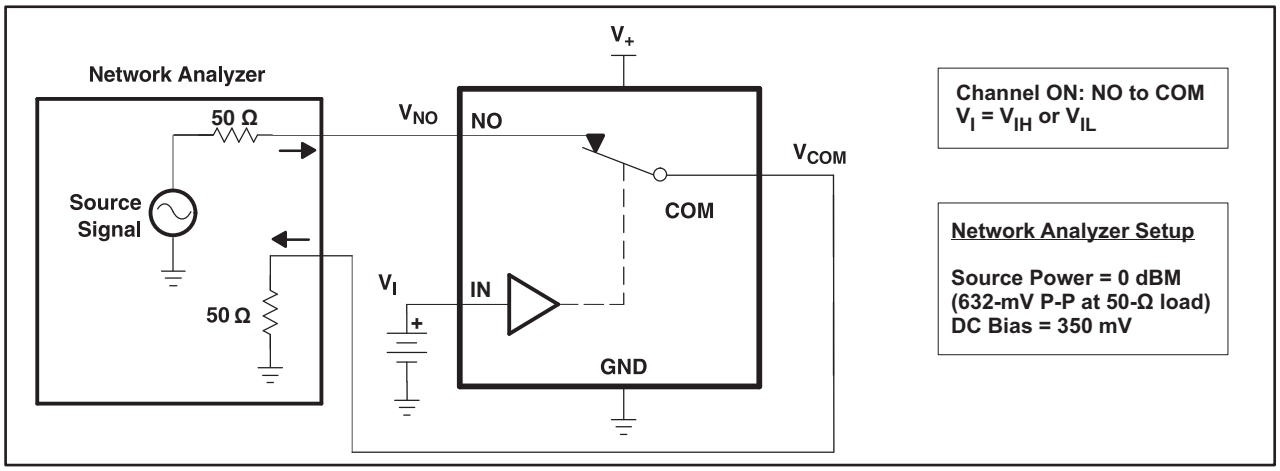


Figure 21. Bandwidth (BW)

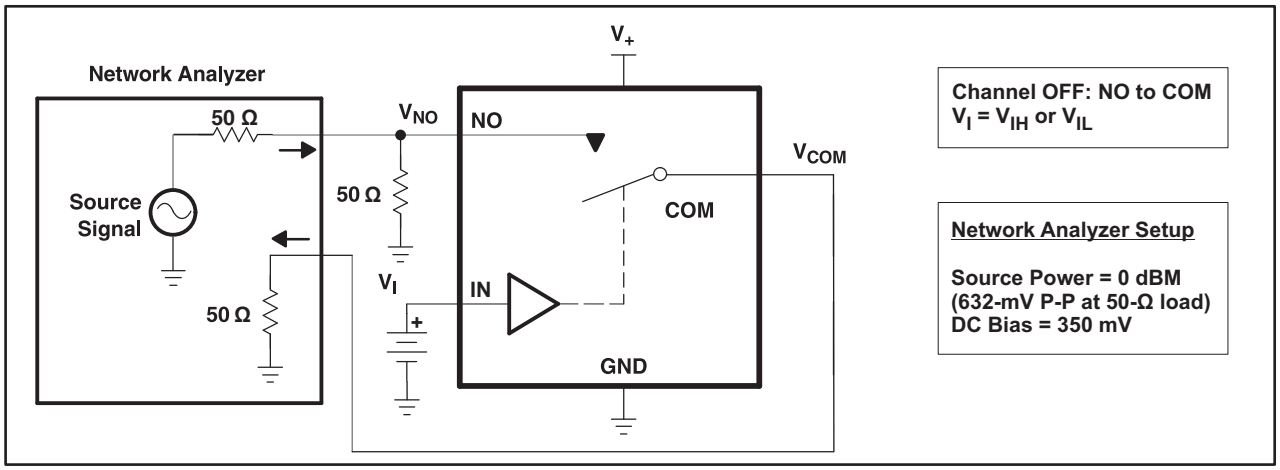


Figure 22. OFF Isolation (O_{ISO})

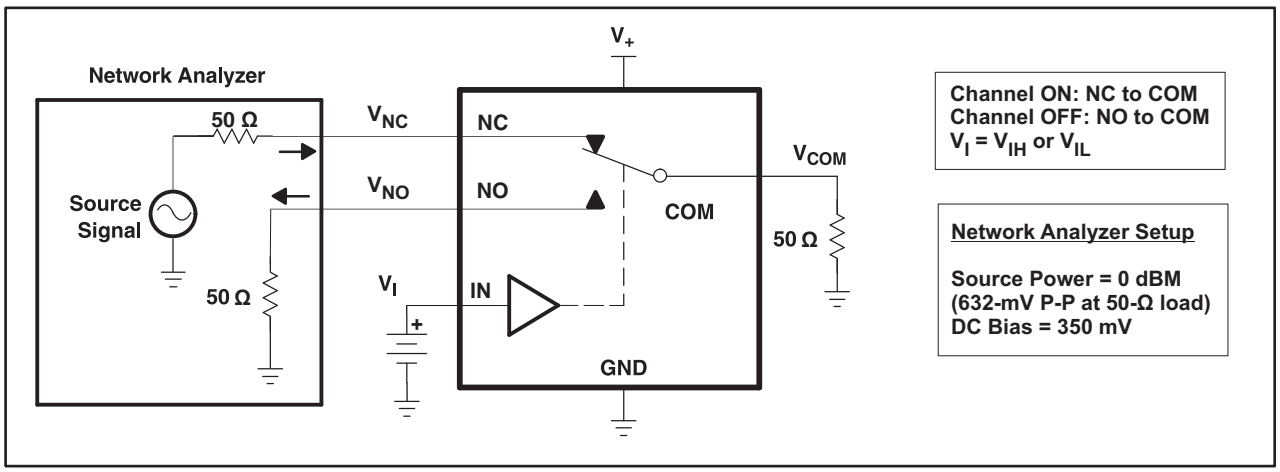


Figure 23. Crosstalk (X_{TALK})

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)

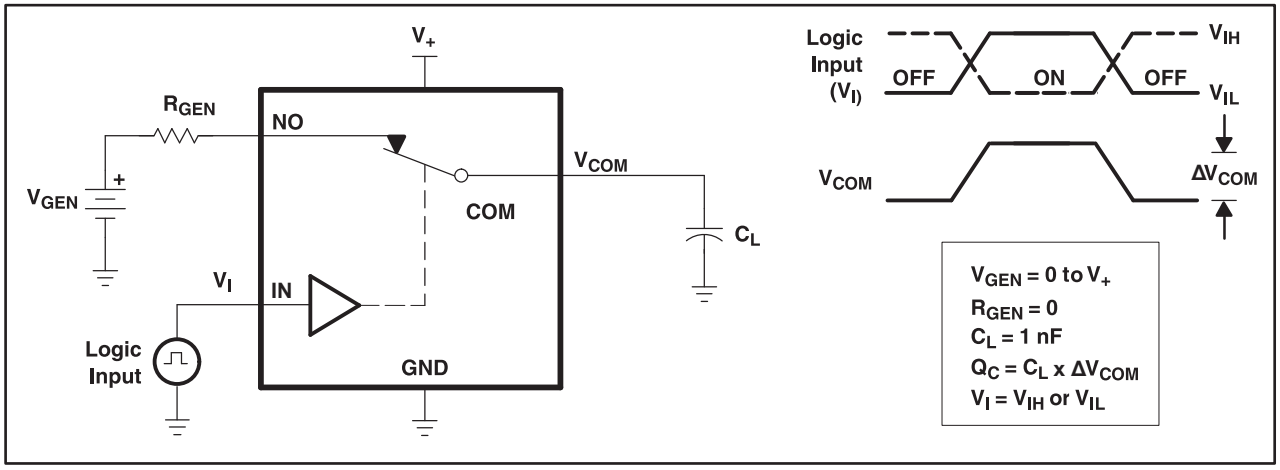


Figure 24. Charge Injection (Q_C)

A. C_L includes probe and jig capacitance.

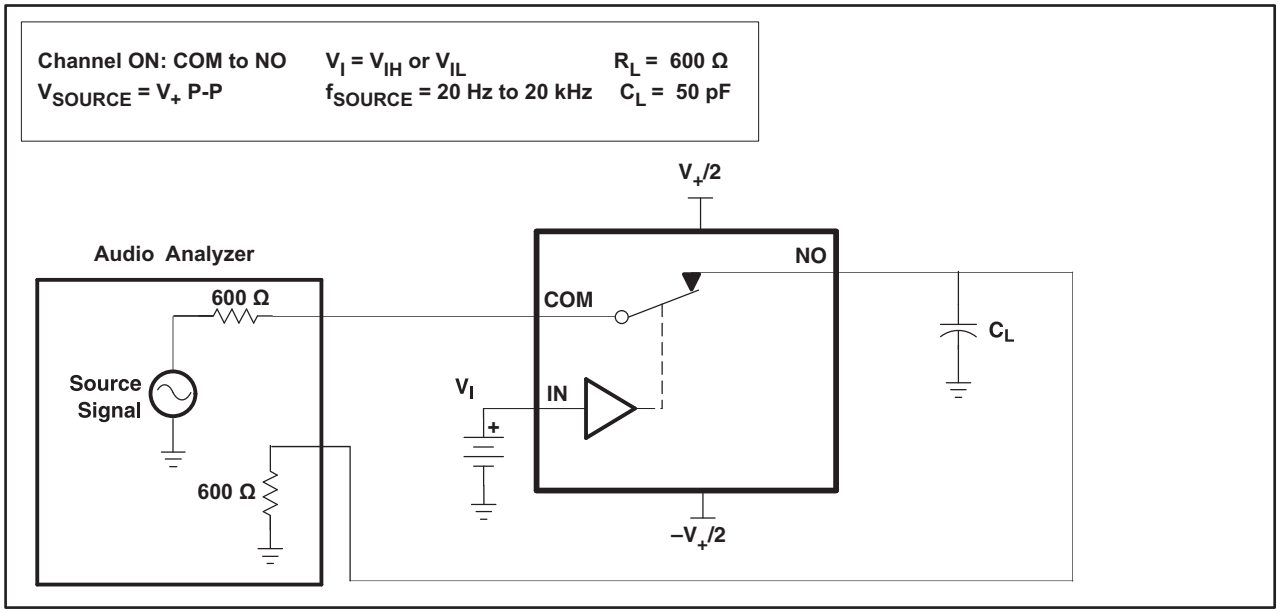


Figure 25. Total Harmonic Distortion (THD)

REVISION HISTORY

Changes from Revision A (August 2009) to Revision B	Page
• Removed QFN reference from product description.	1
• Changed Analog signal range MIN value from V_+ – 0.5 to V_+ – 5.5	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A22366YFCR	ACTIVE	DSBGA	YFC	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(3A2 ~ 3AN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

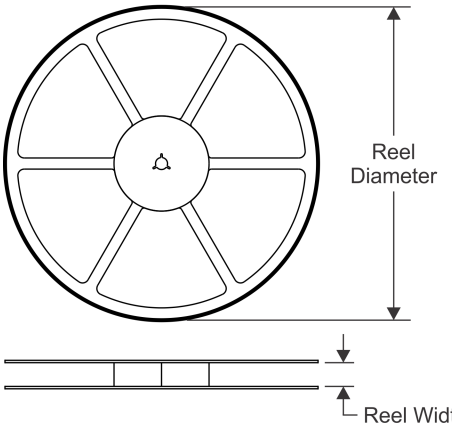
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

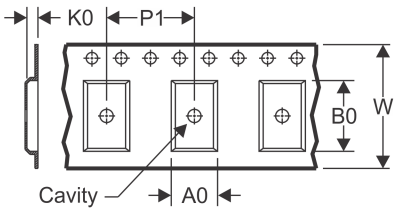
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

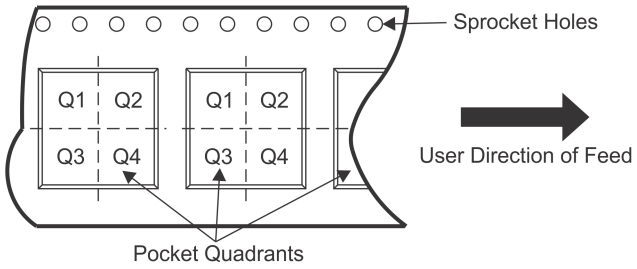


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

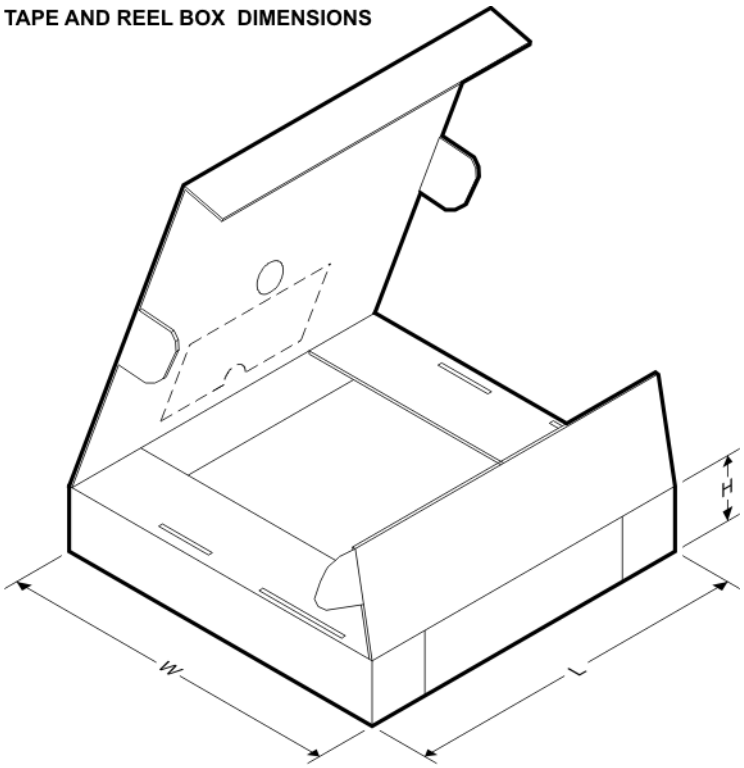
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A22366YFCR	DSBGA	YFC	12	3000	178.0	9.2	1.29	1.69	0.73	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

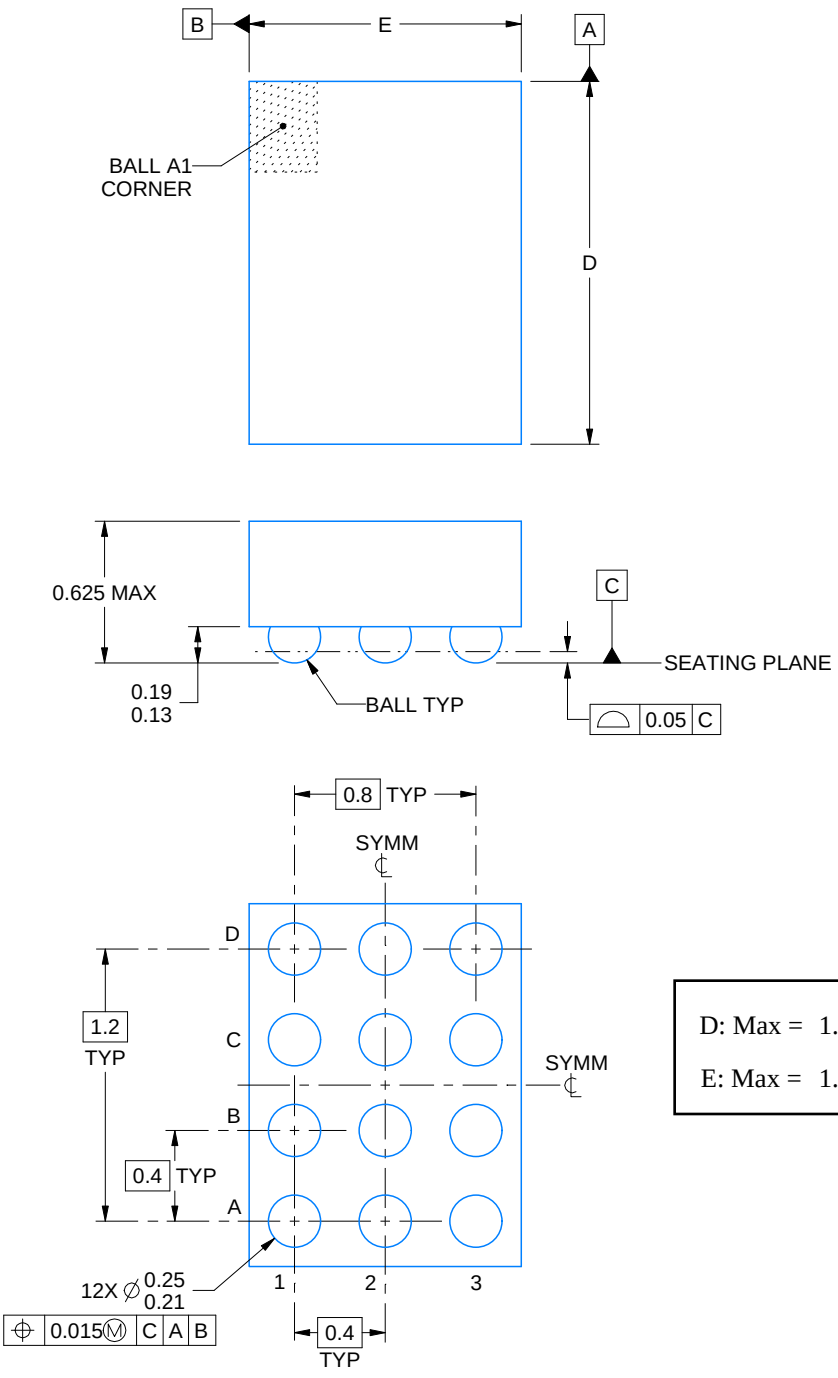
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A22366YFCR	DSBGA	YFC	12	3000	220.0	220.0	35.0

PACKAGE OUTLINE

YFC0012

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.59 mm, Min = 1.53 mm

E: Max = 1.19 mm, Min = 1.13 mm

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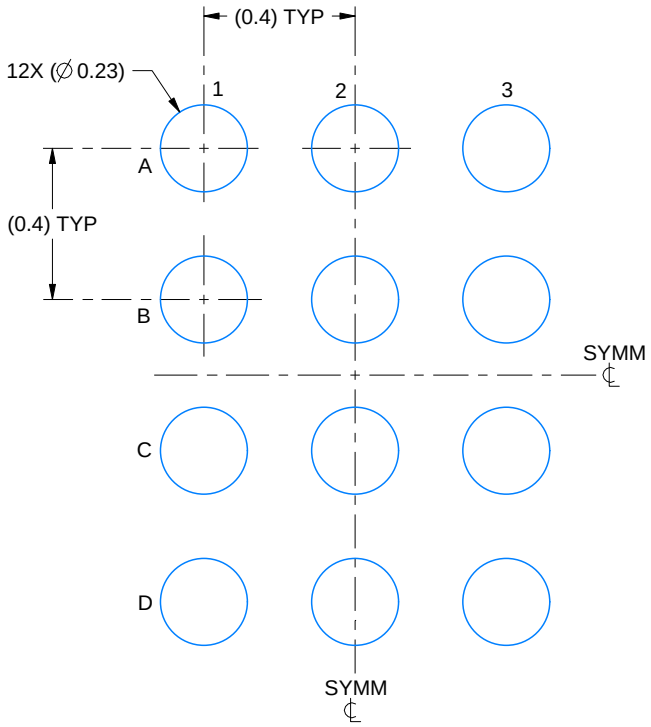
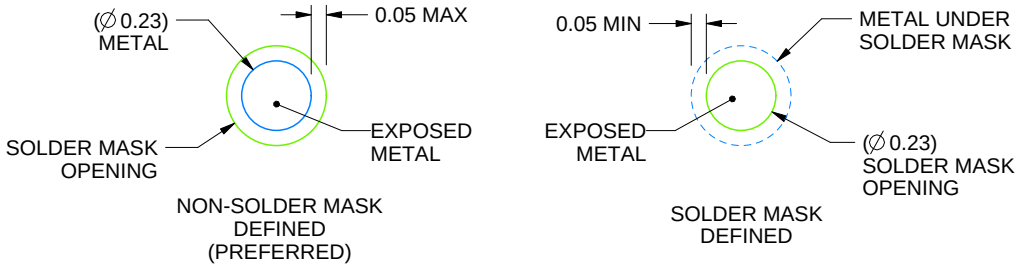
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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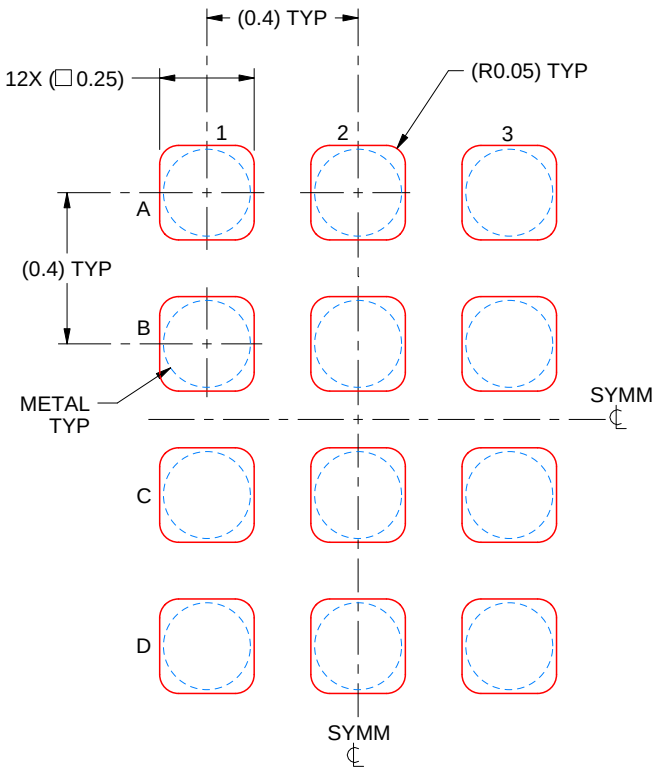
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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