TS61005
Wireless Charging PWM Controller

POWER MANAGEMENT

Features

- Dual N-Channel MOSFET Driver with Programmable Dead Time Control
- Wide Power Stage Input Voltage: Up to 36V
- Integrated Low Input Voltage 3.3V LDO
- Smart Gate Drive to Reduce EMI
- Integrated Bootstrap Switch
- Diode Emulation for High Light Load Ef ciency
- Tri-State PWM Input for Drive Stage Shutdown
- UVLO, Over Temperature Shutdown
- 10 Lead MLPD-UT 2.3mm x 2.3mm Package
- Full Industrial Temperature Range
- Fully WEEE and RoHS Compliant

Applications

- Smart Watches
- Wearables
- Consumer
- Toys
- Portable Lighting
- Medical Devices
- Low power Industrial applications

Description

The TS61005 is a high-side and low-side N-channel MOSFET driver with integrated bootstrap switch optimized for wireless charging applications. This driver can be used as a synchronous buck converter MOSFET driver. The SmartDrive™ function at the turn-on of the high-side MOSFET is a standout feature of this part to reduce the EMI. The diode emulation mode operation offers the opportunity to achieve high ef ciency at light load. The integrated LDO reduces the cost and the footprint of the system.

An Under-Voltage-Lock-Out (UVLO) function is included to ensure the driver outputs are of when the bias voltage falls below 4.02V. An over temperature shutdown feature is also included to prevent the driver from overheating.

The TS61005 is available in a space-saving 10 lead 2.3mm x 2.3mm MLPD-UT package and operates over the industrial temperature range.

Typical Application Circuit

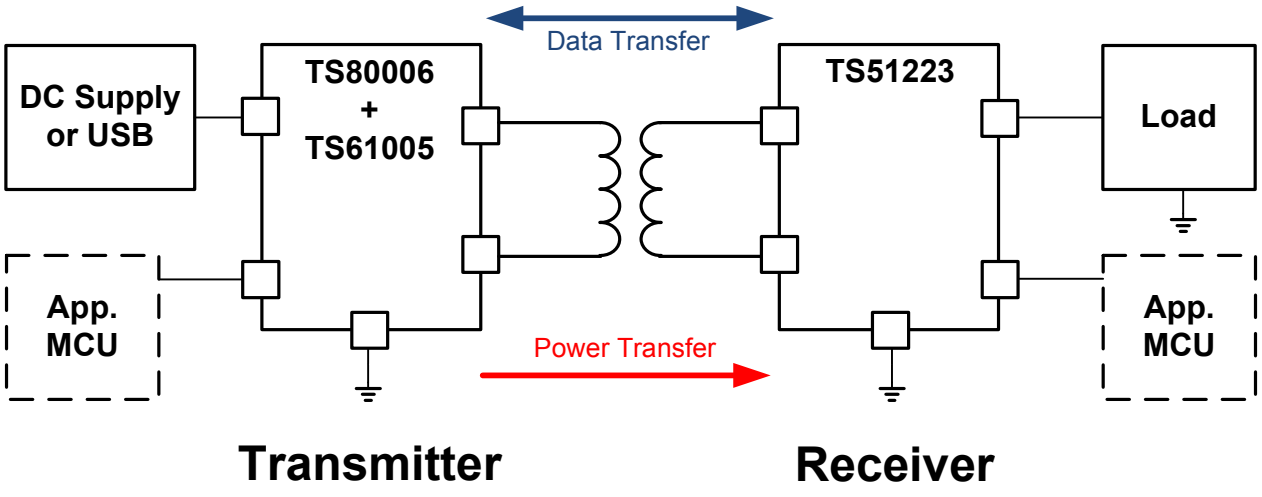
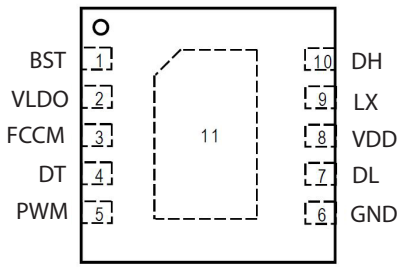


Figure 1. Typical Application for Wireless Power

Pin Configuration

Top View



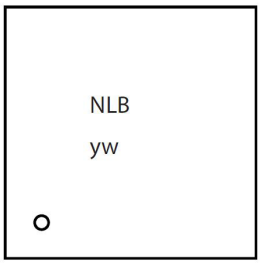
θ_{JA} = 42°C/W
10-Lead (2.3mm x 2.3mm) MLPD-UT

Ordering Information

Device Part #	Description	MLPD-UT-10 (2.3mm x 2.3mm)
TS61005-QFNR	Wireless Charging PWM Controller	Tape & Reel (3000 parts/reel)

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Available in lead-free package only. Device is WEEE and RoHS compliant and halogen free.

Marking Information



NLB - Part Number
yw - Datecode

Absolute Maximum Ratings

VDD to GND (V) ..... -0.3 to +6.0
DH, BST to GND (V) ..... -0.3 to +44
DH, BST to LX (V) ..... -0.3 to +6.0
LX to GND (V)(1) ..... -2.0 to +38
PWM, FCCM, DT, DL to GND (V) ..... -0.3 to VDD+0.3
VLDO to GND (V) ..... -0.3 to +6.0
ESD Protection Level(2) (kV) 3

Recommended Operating Conditions

VDD (V) ..... $4.5 \leq V_{DD} \leq 5.5$

Thermal Information

Thermal Resistance, Junction to Ambient(3) (°C/W) 42
Maximum Junction Temperature (°C) .....+150
Storage Temperature Range (°C)..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) The transient negative voltage specification for the LX pin is -6V for 100ns.
(2) Tested according to JEDEC standard JS-001-2012. BST-VDD passed 1.5kV.
(3) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless noted otherwise T_J = 25° C for typical, -40° C $\leq T_J \leq$ 125° C for min and max, VDD = 5.25V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VDD						
Operating range			4.5		5.5	V
UVLO threshold		rising edge	3.92	4.14	4.34	V
		falling edge	3.88	4.02	4.13	
Quiescent current		PWM = high	249	374	463	µA
		PWM = low	392	531	665	µA
		PWM pin floating	440	570	709	µA
Internal LDO						
LDO output accuracy		LDO load = 10mA	3.16	3.26	3.38	V
Current limit			127		372	mA
Over Temperature Shutdown						
Over temperature shutdown		temperature rising threshold		150		°C
Hysteresis				20		°C

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High-Side Driver						
Peak source current		BST-LX=5.25V		2		A
Source resistance				1.2	1.7	Ω
Rise time (1)	t_{DH_R}	C_L = 3.3nF, BST-LX = 5.25V, LX = 5V		12		ns
Peak sink current		BST-LX = 5.25V		2		A
Sink resistance				0.8	1.4	Ω
Fall time (1)	t_{DH_F}	C_L = 3.3nF, BST-LX = 5.25V		8		ns
Propagation delay time (1)	t_{DH_PD}	From PWM input falling to DH output falling		16		ns
Low-Side Driver						
Peak source current		VDD = 5.25V		2		A
Source resistance				1.1	1.7	Ω
Rise time (1)	t_{DL_R}	C_L = 3.3nF, VDD = 5.25V		12		ns
Peak sink current		VDD = 5.25V		4		A
Sink resistance				0.4	0.8	Ω
Fall time (1)	t_{DL_F}	C_L = 3.3nF, VDD = 5.25V		6		ns
Propagation delay time (1)	t_{DL_PD}	From PWM input rising to DL output falling		16		ns
PWM Input						
Tri-state rising threshold		V_{PWM_PEAK} = 3.3V and 5V, VDD = 5.25V	0.75	1.0	1.3	V
Tri-state falling threshold		V_{PWM_PEAK} = 3.3V and 5V, VDD = 5.25V	1.7	2.1	2.5	V
Tri-state voltage		PWM float		1.45		V
Tri-state shutdown entry delay (1)	t_{TR_END}	VDD = 5.25V		303		ns
Tri-state shutdown exit delay (1)	t_{TR_EXD}	VDD = 5.25V		62		ns
PWM sink impedance			7.5	10	14	kΩ
PWM source impedance			19	26	34	kΩ
Operating frequency range			4		7000	kHz
Minimum pulse width at high				30		ns
FCCM						
Input logic high		Rising threshold	2.0			V

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input logic low		Falling threshold			0.8	V
Zero cross detector threshold		VDD = 5V	-1		+1	mV
Zero cross blanking time		FCCM enabled, VDD = 5V		325		ns
FCCM pin leakage current		FCCM = VDD		3.5	5.6	µA
		FCCM = GND	-1.5		1.5	µA
Intenal Bootstrap Switch						
On resistance				10		Ω
Leakage current				5	15	µA
Dead Time						
Minimum dead time		DT pin is floated		20		ns
Dead Time (2)	t_{DT}	A capacitor C_{DT} = 100pF connected from DT pin to GND		100		ns
Internal series resistor			15	24.5	38	kΩ

NOTES:
(1) Refer to Figure 2 and Figure 3 for the timing definition.
(2) The dead time is C_{DT} x 1ns/pF, where C_{DT} is in pF.

Electrical Characteristics (continued)

Timing Diagram

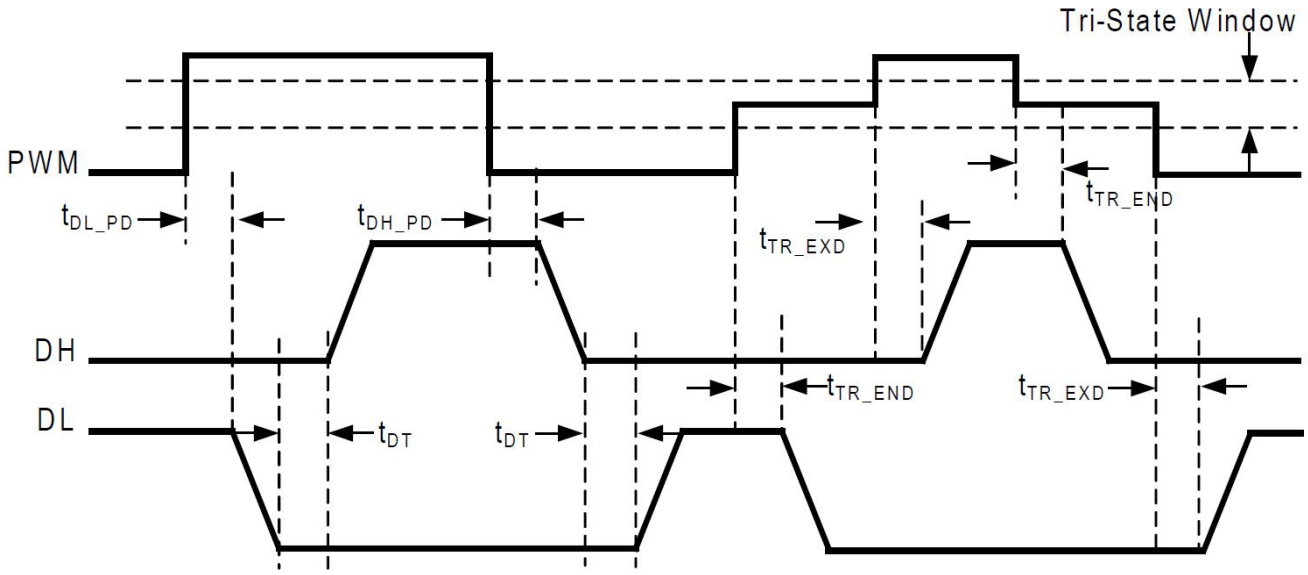


Figure 2. Timing Diagram 1

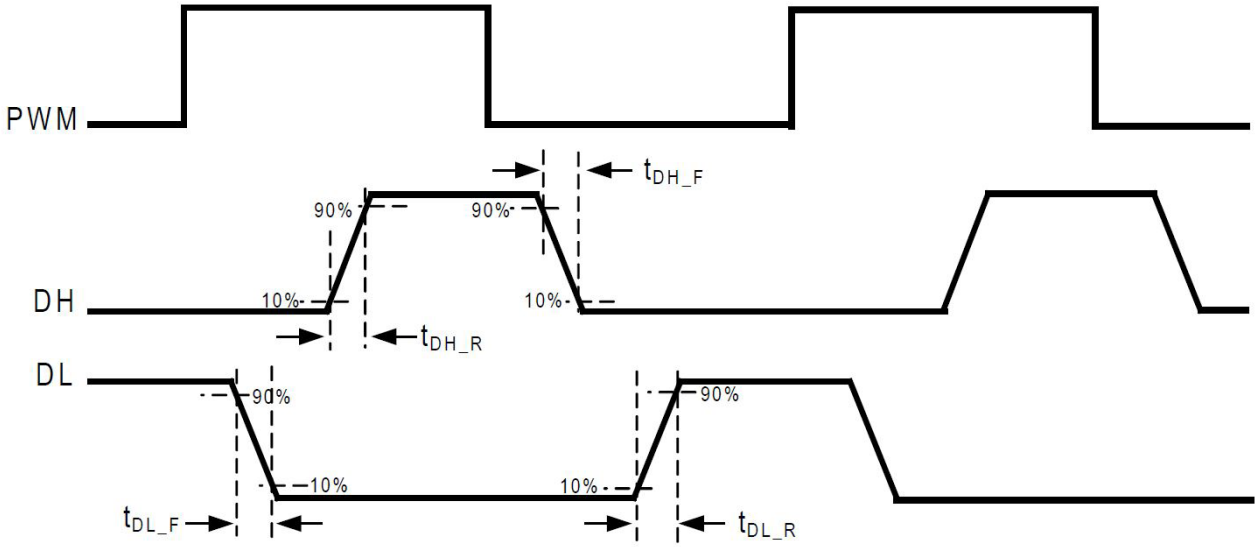


Figure 3. Timing Diagram 2

Pin Descriptions

Pin #	Pin Name	Pin Function
1	BST	Bootstrap pin, supply for the high-side driver.
2	VLDO	3.3V LDO output pin.
3	FCCM	If FCCM pin is low, the low-side MOSFET is turned off when the inductor current reaches zero (diode emulation mode); if FCCM pin is pulled high or floated, the device operates in forced continuous conduction mode (FCCM).
4	DT	Dead time programming pin. Connect a ceramic capacitor from this pin to GND to set the dead time (1ns/pF) between DH and DL.
5	PWM	PWM input pin.
6	GND	Ground pin.
7	DL	Low-side drive output pin.
8	VDD	Power supply pin for the device.
9	LX	Phase node.
10	DH	High-side drive output pin.
	THERMAL PAD	The exposed pad enhances thermal performance and is not electrically connected inside the package. It is recommended to connect the exposed pad to the ground plane.

Block Diagram

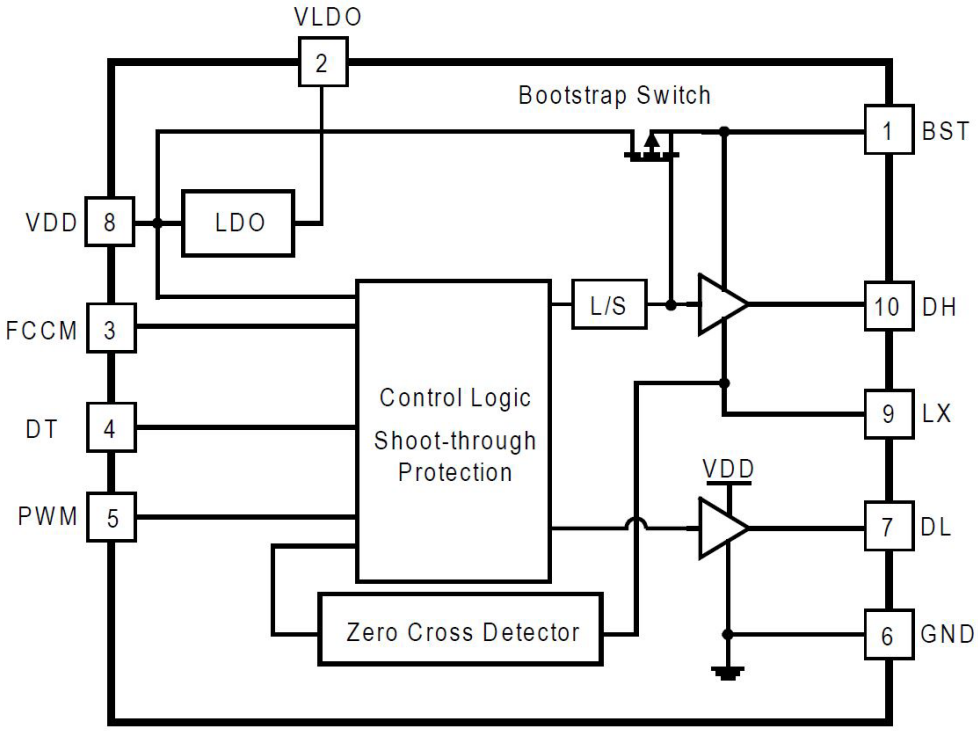
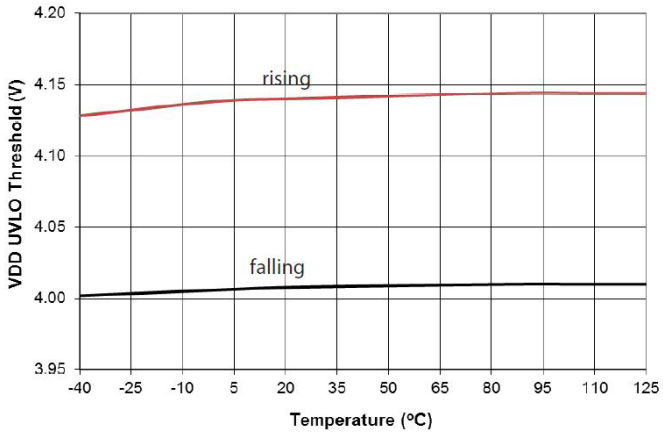


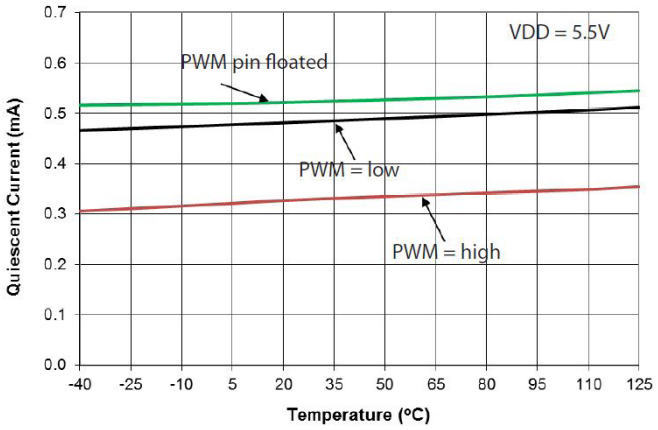
Figure 4. TS61005 Block Diagram

Typical Characteristics

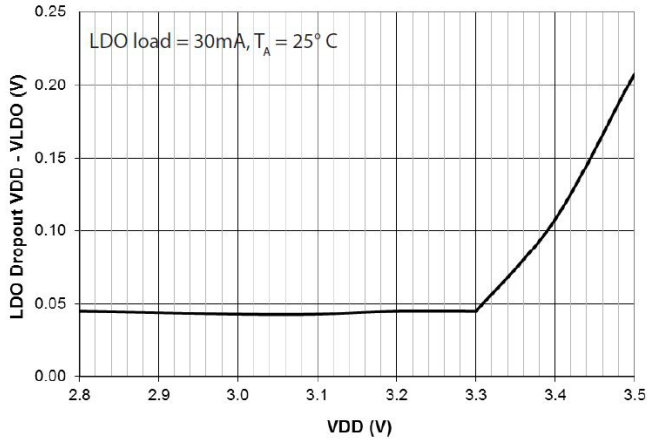
Under Voltage Lockout Threshold



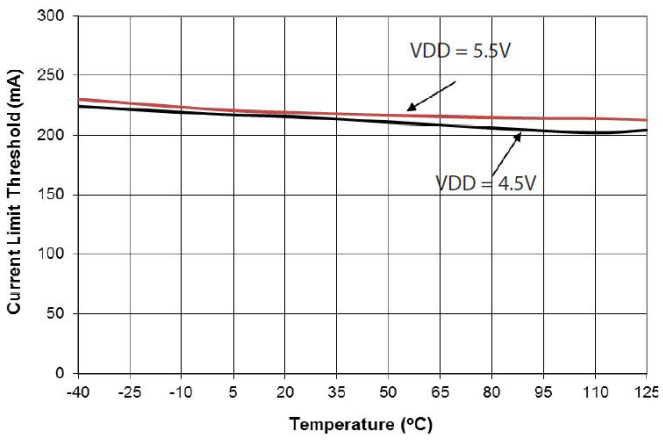
VDD Quiescent Current



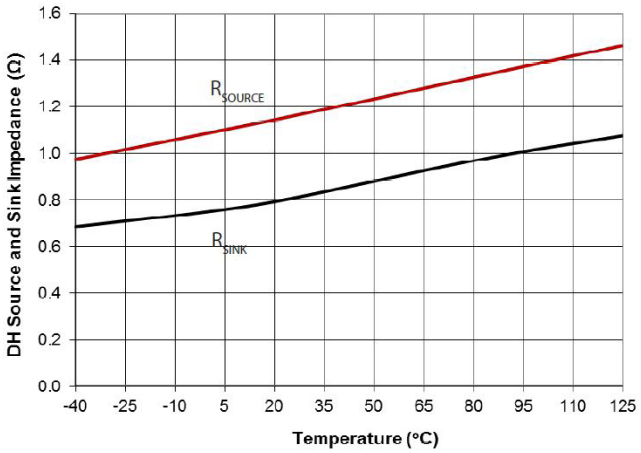
3.3V LDO Dropout Voltage



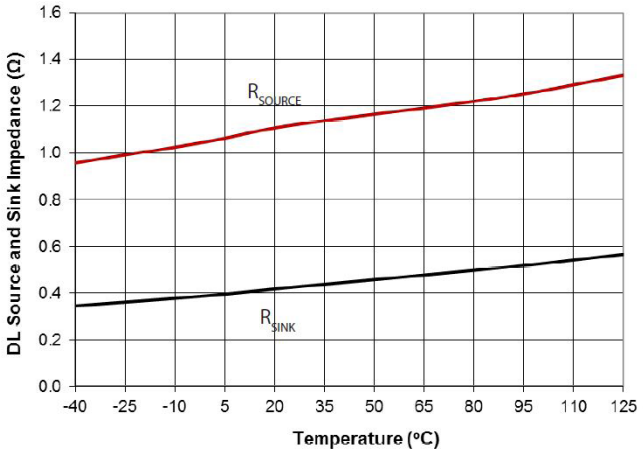
3.3V LDO Current Limit



High-Side Driver Source and Sink Impedance

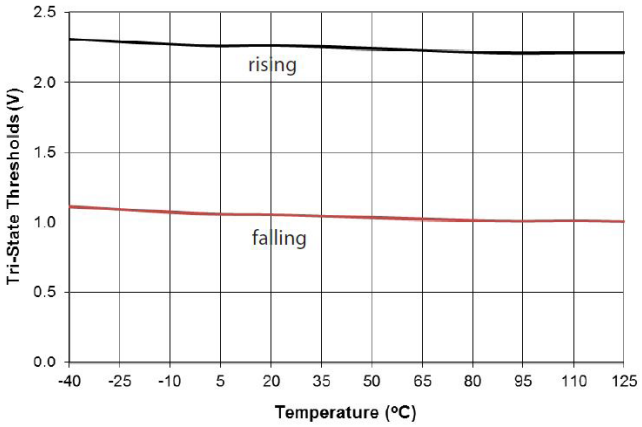


Low-Side Driver Source and Sink Impedance

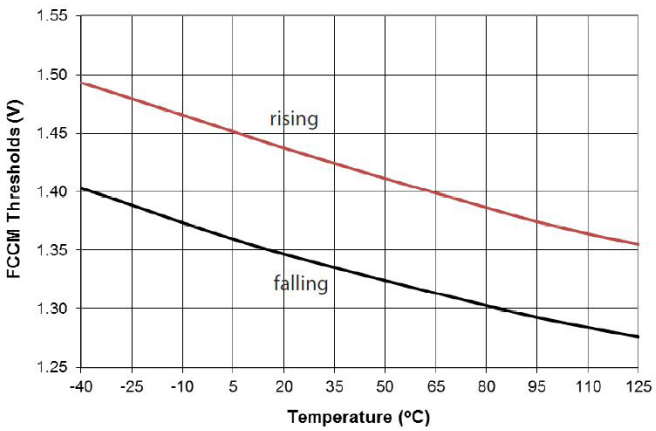


Typical Characteristics (Continued)

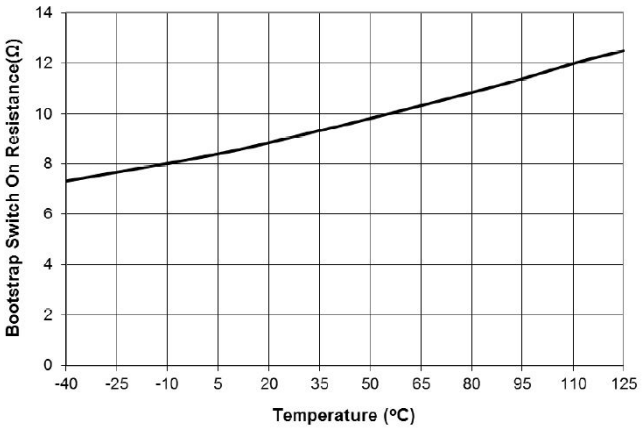
PWM Tri-State Thresholds



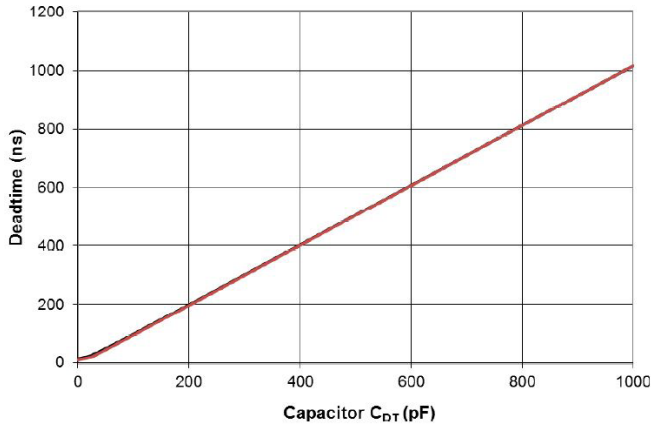
FCCM Logic Thresholds



Bootstrap Switch On Resistance



Dead Time vs C_{DT}



Application Information

Overview

The TS61005 is a high-side and low-side N-channel MOSFET driver. The driver receives a ground-referenced PWM signal with fast slew rate to drive two N-channel MOSFETs in a synchronous buck converter or any other application with two MOSFETs in a half-bridge configuration. The SmartDrive™ function at the turn-on of the high-side MOSFET reduces the voltage ringing on the low-side switch and also reduces the EMI. Tying the FCCM pin to ground offers diode emulation mode operation to achieve high efficiency at light load. The Under-Voltage-Lock-Out (UVLO) threshold ensures a reliable drive voltage for the external MOSFETs. The over temperature shutdown feature is also included to prevent the driver from overheating.

Under Voltage Lockout

The TS61005 has an under voltage lockout (UVLO) circuit which keeps the driver off when the input voltage is not high enough to drive the external MOSFETs reliably. During power on, the driver outputs (DH and DL) are low until the input voltage reaches the UVLO rising threshold. Once the UVLO threshold is reached, the driver outputs are determined by the signals on the PWM pin and FCCM pin. The UVLO falling threshold is about 0.2V lower which prevents the driver from turning on and off due to a slow input slew rate.

Tri-State PWM Input

The TS61005 features a tri-state PWM input pin. When the PWM signal is less than 1V (typical), it is considered as a logic low while the signal is taken as a logic high when it is higher than 2.1V (typical). 1V to 2.1V is the tri-state window for the PWM signal. These thresholds make it work well for both 3.3V logic and 5V logic PWM signals. If the PWM pin is left floating, the internal resistor divider sets the voltage on the PWM pin to 1.45V which is within the tri-state window. For a synchronous buck converter application, pre-biased output startup is supported if the buck controller features a tri-state PWM output pin.

Programmable Dead Time Control

The dead time control is to prevent shoot-through of the high-side MOSFET and the low-side MOSFET. Shoot-through can cause poor efficiency and even cause the MOSFET to blow up. The dead time control circuitry of a MOSFET driver is thus very important in real applications. An adaptive dead time control function is implemented in the TS61005 by sensing the DH and DL signals. The TS61005 has a DT pin which offers an option to program the dead time with a ceramic capacitor from this pin to the GND pin. A ceramic capacitor with tight tolerance such as Murata C0G material capacitor should be used for this purpose. The dead time is 20ns typical with the DT pin floated.

Application Information (Continued)

FCCM/Diode Emulation Mode Operation

There are two operating modes which can be configured with the FCCM pin of the TS61005. When the FCCM pin is floated or tied to a logic high signal (e.g. VDD), the drive signal DL is always complementary to DH. This is called forced continuous conduction mode (FCCM) operation. If the FCCM pin is grounded, a zero-crossing circuit is activated in the TS61005. The DL output is turned to low when the current in the external low-side MOSFET reaches zero. In other words, the external low-side MOSFET acts like a diode. This operation mode is thus called diode emulation mode. The benefit of this diode emulation mode is to reduce conduction losses at light load for high efficiency.

SmartdriveTM

For each DH drive pulse, the TS61005 initially turns on the high-side MOSFET with a weak driver, allowing a softer, smooth turnoff of the low-side MOSFET. Once the low-side MOSFET is turned off and the LX pin voltage has risen about 2.5V above ground, the TS61005 switches to a much stronger driver to complete the turn-on of the high-side MOSFET at a more rapid rate. This technique reduces the voltage ringing for the switching node, which relieves the need for a snubber or a gate resistor.

Bootstrap Capacitor

The TS61005 integrates the bootstrap switch. Only an external bootstrap capacitor connected between the BST pin and the LX pin is needed for a complete bootstrap circuit. The bootstrap capacitor, which is charged from VDD during the on time of the low-side MOSFET, provides the energy to turn on the high-side MOSFET. The capacitance for the bootstrap capacitor is mainly determined by the gate charge Q_g of the high-side MOSFET. The equation below gives a first order estimate:

$C_b = Q_g / \Delta V_b$

Where ΔV_b is the allowable voltage drop of the drive voltage for the high-side MOSFET. In a real application, considering the capacitance tolerance, Q_g variation, leakage current of the BST pin etc., a capacitor with two times the calculated value is a good starting point. A ceramic capacitor of X5R or X7R, or equivalent material, should be used.

VLDO Decoupling Capacitor

The VLDO pin is the 3.3V LDO output pin. This 3.3V LDO can be used as the bias for a microcontroller or any other digital controller which requires quite, accurate 3.3V bias on the system board. A high frequency decoupling capacitor with low ESR and low ESL should be put from the VLDO pin to the GND pin with minimum trace length. A typical value of 2.2µF, 6.3V rating, X5R or X7R ceramic capacitor is recommended.

VDD Decoupling Capacitor

The VDD is the input bias for the low-side driver and the internal control circuitry. This pin is also used for the VDD UVLO check. A high frequency decoupling capacitor with low ESR and low ESL should be put from the VDD pin to the GND pin with minimum trace length. A typical value of 2.2µF, 10V rating, X5R or X7R ceramic capacitor is recommended.

Power Dissipation

wer dissipation in this driver consists of two main components: the power loss for turning on and off the external MOSFETs, and the power loss in the internal LDO (if used). The below equation can be used to estimate the total power dissipation in the driver:

$P_d = VDD\ f_s\ (Q_{gh} + Q_{gl}) + (VDD - 3.3)\ I_L$

Where:

f_s is the switching frequency

Q_{gh} is the total gate charge of the high-side MOSFET

Q_{gl} is the total gate charge of the low-side MOSFET

I_L is the external load connected to the VLDO pin

Application Information (Continued)

To ensure proper operation and long-term reliability, the power dissipation should be examined in the real application to make sure the junction temperature will not go beyond 125°C. Multiple vias should be used to connect the thermal pad underneath the driver package to the ground plane on the system board for good thermal management.

$T_J = T_A + P_d \theta_{JA}$
Where:
T_J is the junction temperature
T_A is the ambient temperature
θ_{JA} is the thermal resistance, 42°C/W

There is a temperature monitor in the driver which will shut down the driver outputs and the LDO when the junction temperature reaches 150°C. The driver will automatically recover when the junction temperature cools to less than 132°C.

Layout Recommendations

TS61005 is designed to provide strong source and sink capability for MOSFET drive at high frequency. In order to achieve this objective, the PCB layout is critical. Some guidelines are highlighted below to achieve good performance with TS61005.

A. Locate the driver as close as possible to the MOSFETs.

B. Mount the decoupling capacitors as close as possible between the VIN pin and the GND pin, the VDD pin and the GND pin, the BST pin and the LX pin.

C. Minimize the PCB trace length between the DL pin to the low-side MOSFET gate, the GND pin and the source of the low-side MOSFET. Avoid mixing the ground trace of the drive loop with the power stage current path.

D. Apply a similar rule for the high-side drive loop.

E. Use wide PCB trace > 20 mils for the drive loops.

F. Use two or more vias if the PCB trace for the drive loops needs to be routed from one layer to another.

G. The ground of the input signals (PWM, FCCM and DT) should be separated from the power ground plane and directly connected to the GND pin of the driver.

H. Use multiple vias to connect the thermal pad to the ground plane.

Typical Application Circuits

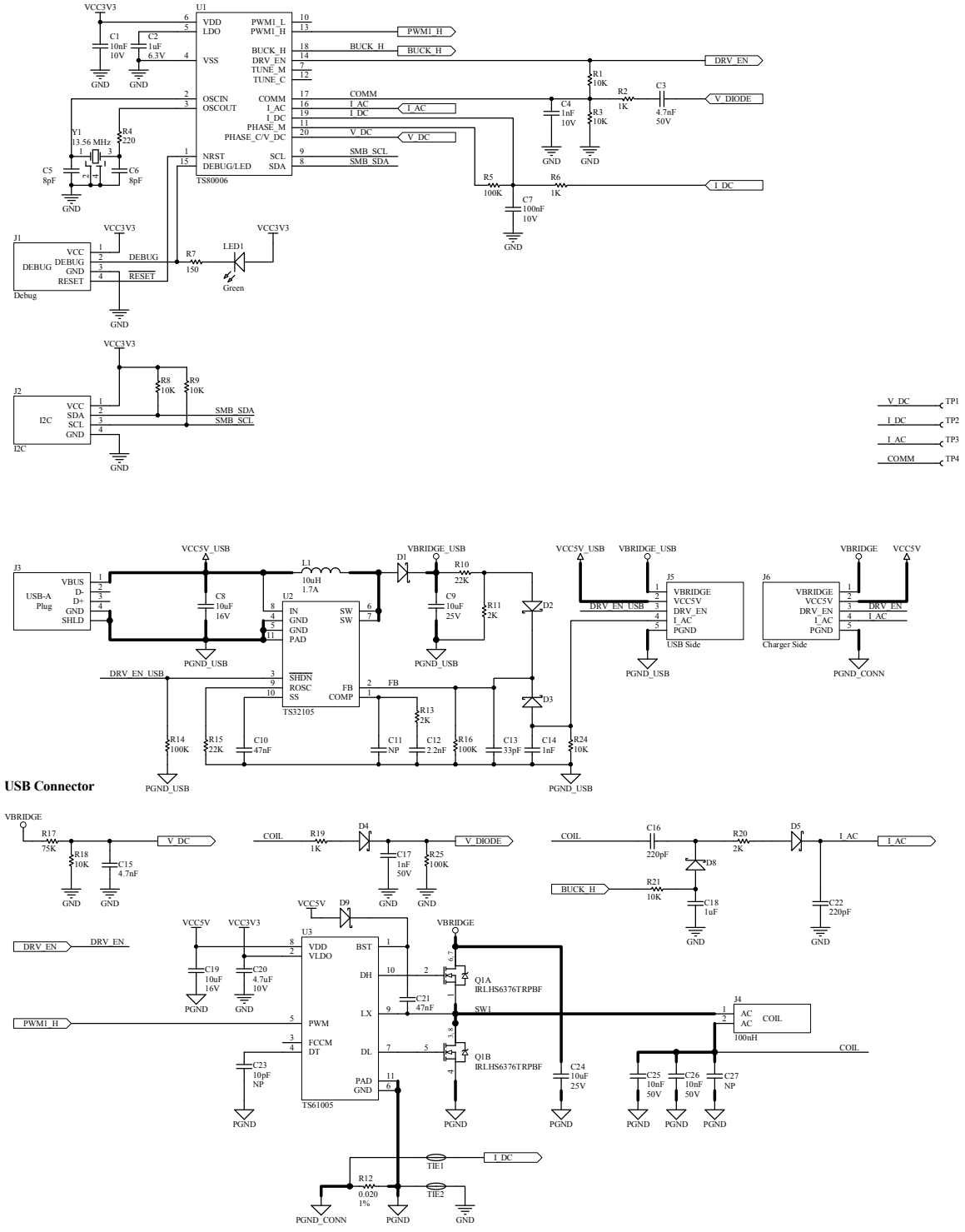
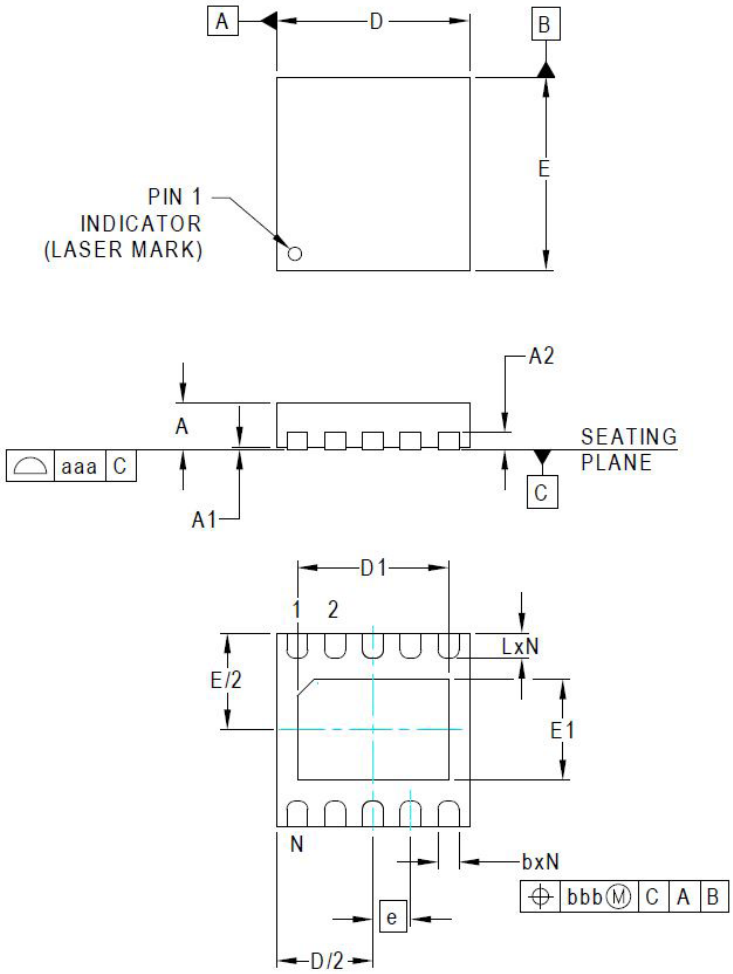


Figure 5. Wearable Wireless Power Transmitter

Outline Drawing — 2.3mm x 2.3mm MLPD-UT-10

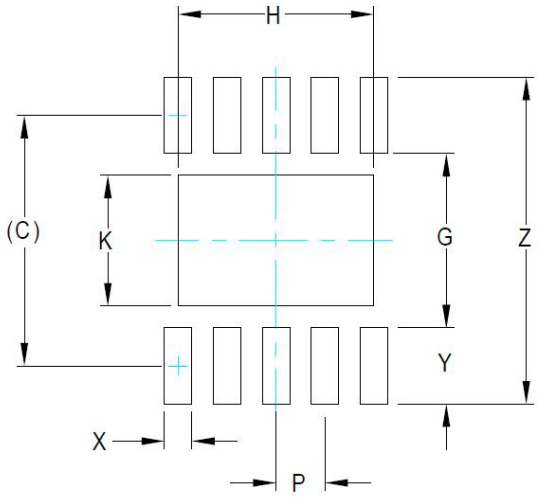


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	-	0.60
A1	0.00	0.02	0.05
A2		(0.152)	
b	0.18	0.25	0.30
D	2.20	2.30	2.40
D1	1.65	1.80	1.90
E	2.20	2.30	2.40
E1	1.05	1.20	1.30
e		0.45 BSC	
L	0.20	0.30	0.40
N		10	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern — 2.3mm x 2.3mm MLPD-UT-10



DIMENSIONS	
DIM	MILLIMETERS
C	(2.30)
G	1.60
H	1.80
K	1.20
P	0.45
X	0.25
Y	0.70
Z	3.00

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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