

TS7021N - 100W CW GaN Broadband RF Switch SPDT

1.0 Features

- Low insertion loss: 0.65dB @ 1.9GHz
- High isolation: 37dB @ 1.9GHz
- High linear power handling capability
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6-5.5V power supply
- Operating frequency: 500MHz to 2.7GHz

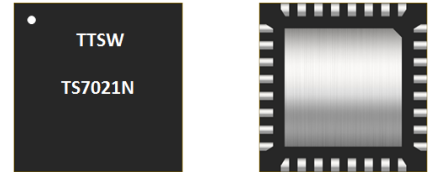


Figure 1 Device Image
(32 Pin 5x5x1.25mm QFN Package)

2.0 Applications

- Private mobile and military radios
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals



**RoHS/REACH/Halogen Free
Compliance**

3.0 Description

The TS7021N is a symmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high power switching applications. With a simple broadband match, the TS7021N can cover 500M to 2.7GHz bandwidth and provide low insertion loss, high isolation and high linearity within a small package size. TS7021N is an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7021N is packaged into a compact Quad Flat No lead (QFN) 5x5mm 32 leads plastic package.

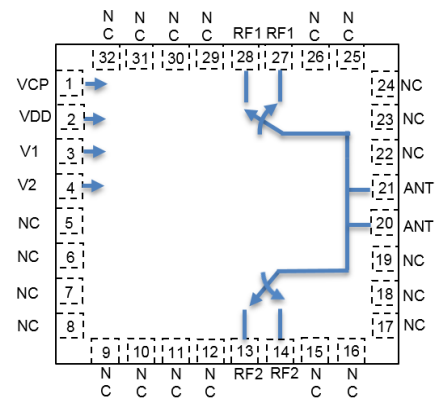


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS7021N	32 Pin 5x5x1.25mm QFN	Tape and Reel	1000	13" (330mm)	18mm	TS7021NMTRPBF
Evaluation Board						TS7021N-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
2	VDD	DC power supply
3	V1	Switch control input 1
4	V2	Switch control input 2
5,6,7,8,9,10,11,16,17, 18,23,24,25,30,31,32	NC	No internal connection, can be grounded
12,15,19,22,26,29	NC	No internal connection. Do not connect to ground
13,14	RF2	RF port 2
20,21	ANT	Antenna port
27,28	RF1	RF port 1

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias and adequate heat sinking must be used to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T _{st}	-55 to +125	°C
Operating Temperature Range	T _{op}	-40 to +85	°C
Maximum Junction Temperature	T _J	+140	°C
RF Input Power CW, T _{case} =+85°C, 800MHz	RFx	47	dBm
RF Input Power CW, T _{case} =+85°C, 2600MHz	RFx	46.5	dBm
RF Input Power (VSWR 20:1), 2 minutes, 800MHz	RFx	45	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	R _{θJC}	4.0	°C/W
Soldering Temperature	T _{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+2.7V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		500		2700	MHz
Insertion loss, RFx	800MHz		0.50	0.60	dB
	1.95GHz		0.65	0.75	
	2.6GHz		0.70	0.85	
Isolation ANT-RFx	800MHz	41	45		dB
	1.95GHz	33	37		
	2.6GHz	30	34		
Return loss ANT, RFx	800MHz		19		dB
	1.95GHz		20		
	2.6GHz		25		
Harmonic distortion					
H2	800MHz, Pin=45dBm		-74		dBc
H3	800MHz, Pin=45dBm		-70		dBc
IIP3	800MHz		71		dBm
P0.1dB ^[1]	0.1dB compression point, 500MHz ~ 1.5GHz		50		dBm
P0.1dB ^[1]	0.1dB compression point, 1.5GHz ~ 2.7GHz		49.0		dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. CP=1nF to ground on VCP pin.		1.5		μs
Control voltage	Power Supply VDD	2.6	3.3	5.5	V
	All control pins high, V _{ih}	1.0	3.3	5.25	V
	All control pins low, V _{il}	-0.3		0.5	V
Control current	All control pins low, I _{il}		0		μA
	All control pins high, I _{ih}			7.5	μA
Current consumption, I _{DD}	Active mode (VDD on)		160	200	μA

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	1	All OFF
0	0	ANT-RF1 ON
1	0	ANT-RF2 ON

Attention:

- [1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
- [2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-RF1 ON.
- [3] If all OFF state is not used, the switch can be operated with single control pin V1.

9.0 Evaluation Board

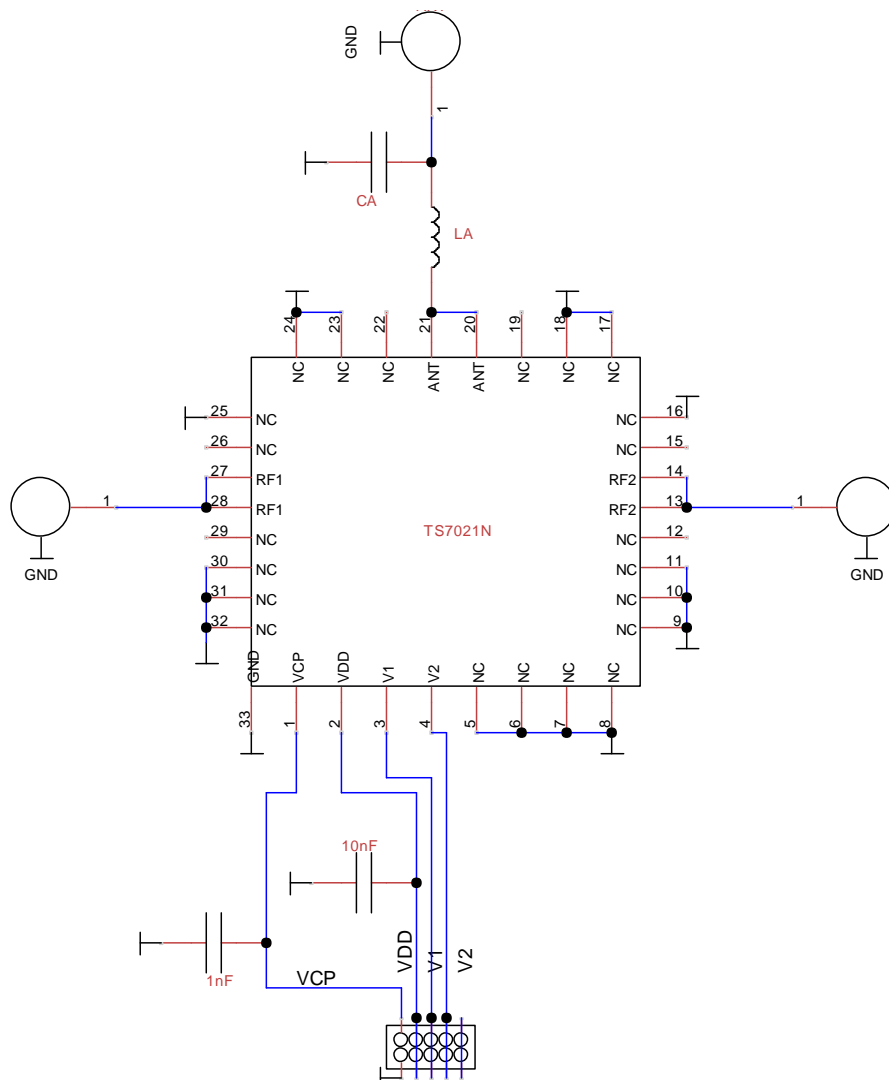


Figure 3 Evaluation Board Schematic

Attention:

[1] **33 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this Ground Pad and adequate heat sinking should be used.**

[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

[3] Place matching components close to pin of the part.

Table 6 Recommended Evaluation Board Component Values

Reference Designator	Value	Part #	Manufacturer
LA	1.6nH	0603HC-1N6XJLU	Coilcraft
CA	0.9pF	0603N0R9BW251	Passive Plus Inc

10.0 Typical Characteristics

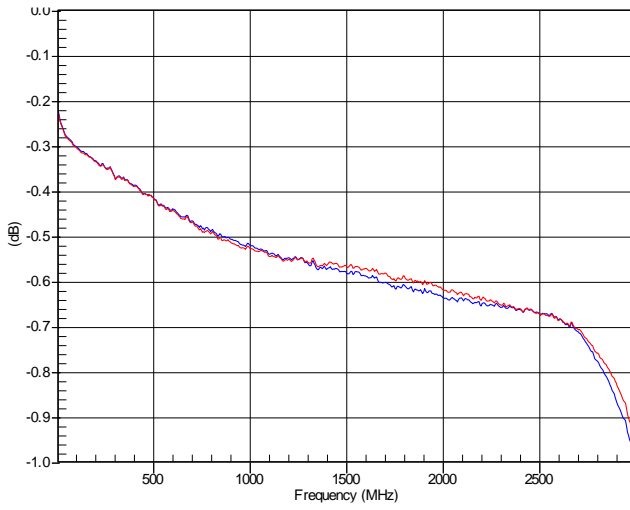


Figure 4 RF1, RF2 Insertion Loss

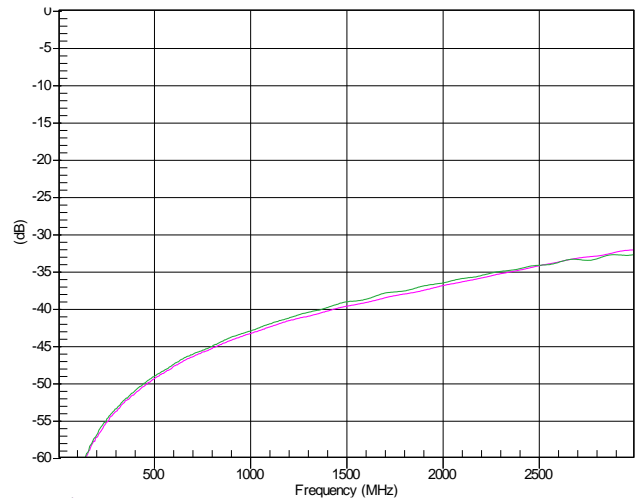


Figure 5 RF1, RF2 Isolation

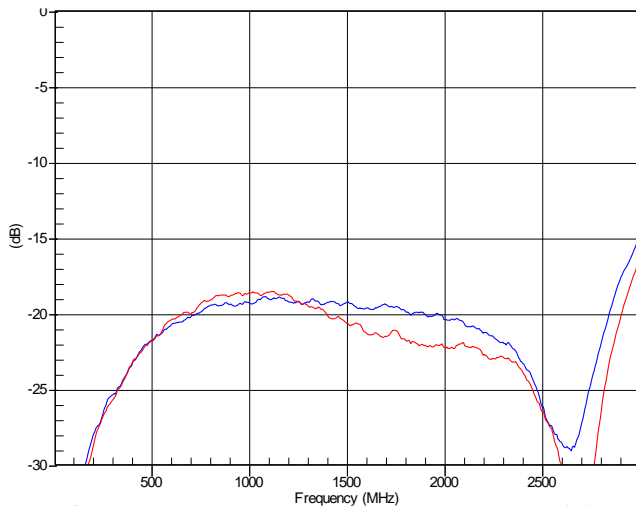


Figure 6 RF1, RF2 Return Loss

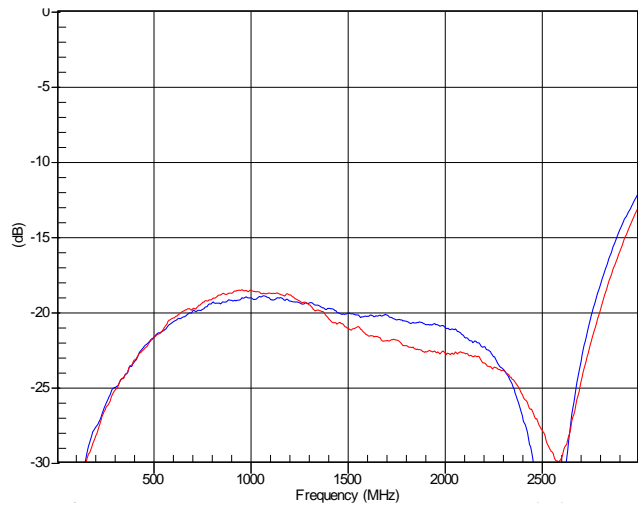


Figure 7 ANT Return Loss

11.0 Device Package Information

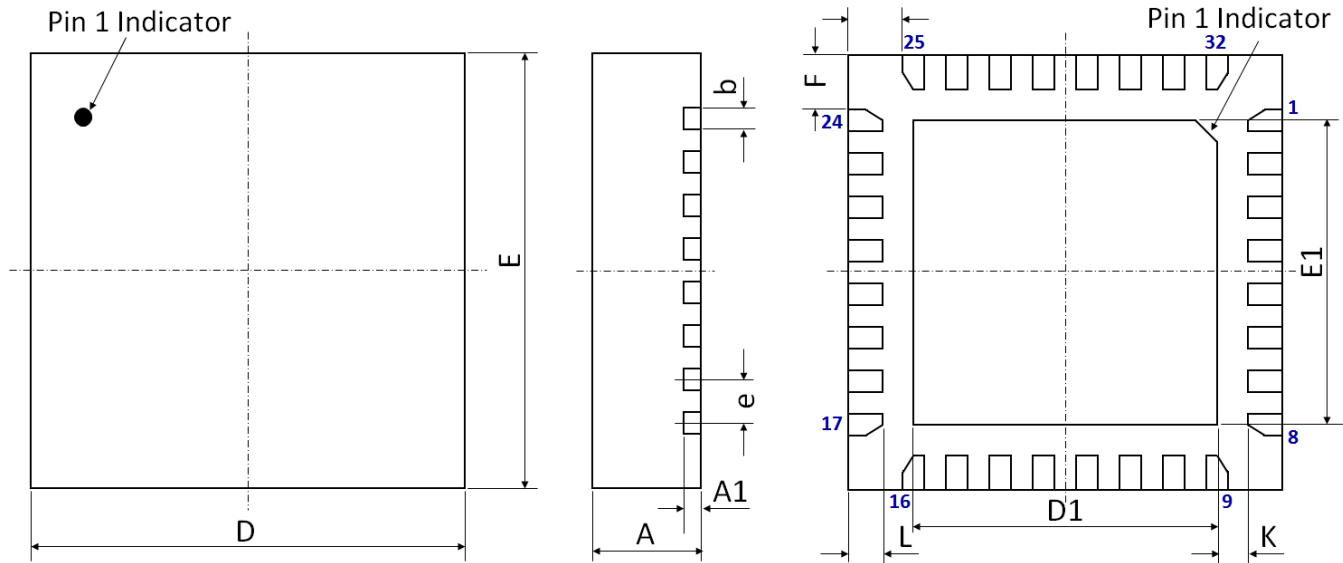


Figure 12 Device Package Drawing
(All dimensions are in mm)

Table 7 Device Package Dimensions

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A	1.25	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.10	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.10	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.50	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:

Please refer to application notes [TN-001](#) and [TN-003](#) at <http://www.tagoretech.com> for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:

- [1] 4 layer PCB is recommended.
- [2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- [3] Thermal vias shall only be placed on the center pad.
- [4] The maximum via number for the center pad is $5(X) \times 5(Y) = 25$.

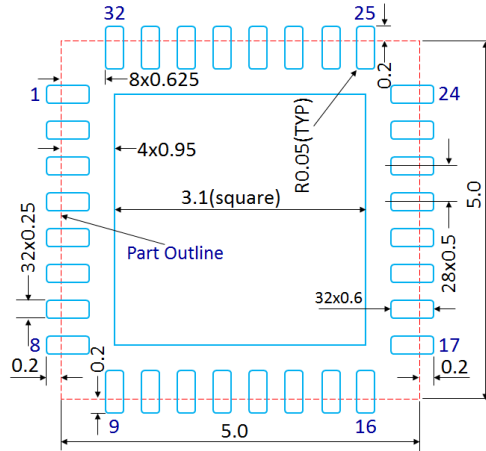


Figure 8 PCB Land Pattern
(Dimensions are in mm)

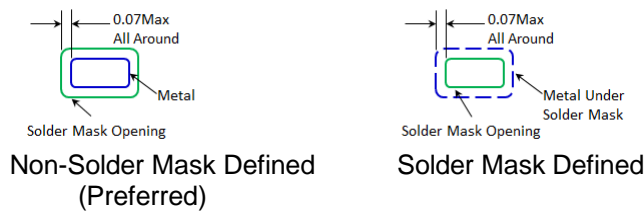


Figure 9 Solder Mask Pattern
(Dimensions are in mm)

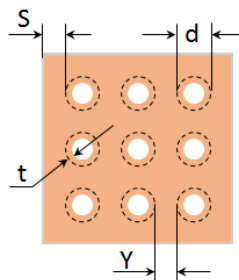


Figure 10 Thermal Via Pattern
(Recommended Values: $S \geq 0.15\text{mm}$; $Y \geq 0.20\text{mm}$; $d = 0.2\text{mm}$; Plating Thickness $t = 25\mu\text{m}$ or $50\mu\text{m}$)

13.0 PCB Stencil Design

Guidelines:

- [1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- [2] Stencil thickness is recommended to be 125µm.

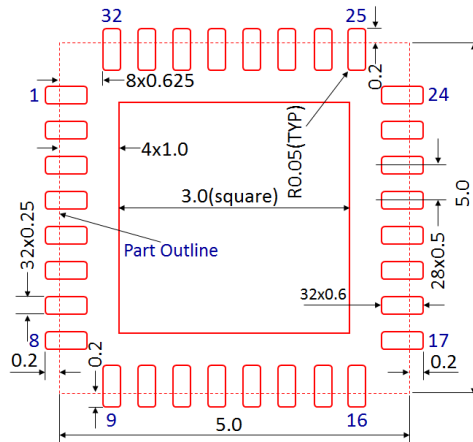


Figure 11 Stencil Openings
(Dimensions are in mm)

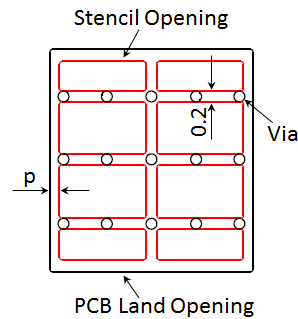


Figure 12 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

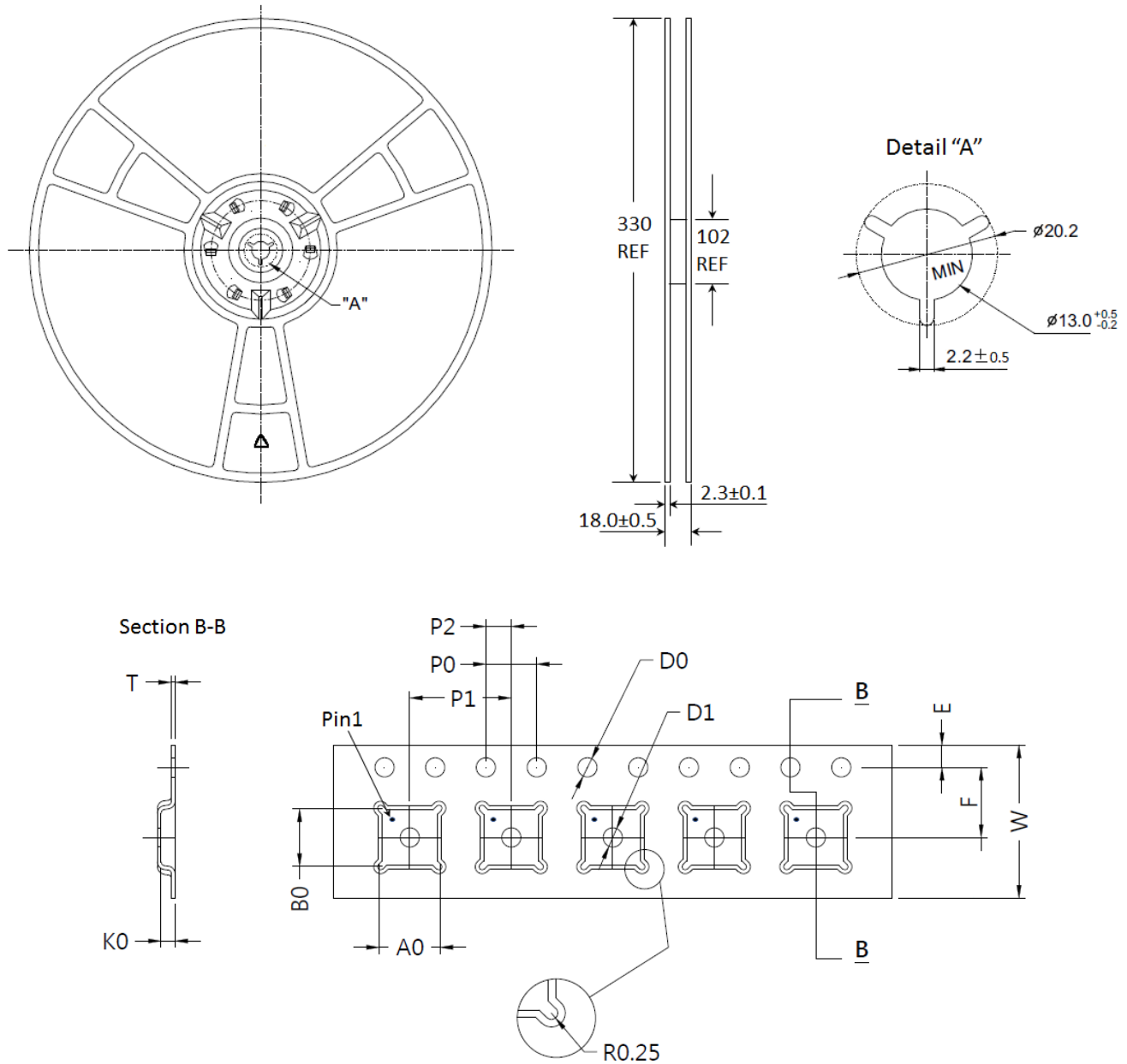


Figure 13 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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