TS7232FK - 10W CW GaN Broadband RF Switch SP3T

1.0 Features

- Low insertion loss: 0.40dB @ 800MHz
- High isolation: 45dB @ 800MHz
- High peak power handling capability
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6-5.5V power supply
- Operating frequency: 30MHz to 4.0GHz

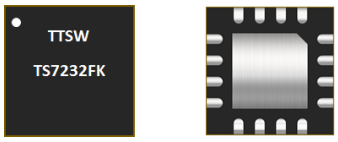


Figure 1 Device Image
(16 Pin 3×3×0.8mm QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS7232FK is a symmetrical reflective Single Pole Three Throw (SP3T) switch designed for broadband, high peak power switching applications. Its broadband behavior from 30MHz to 4GHz frequencies makes the TS7232FK an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7232FK is packaged into a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.

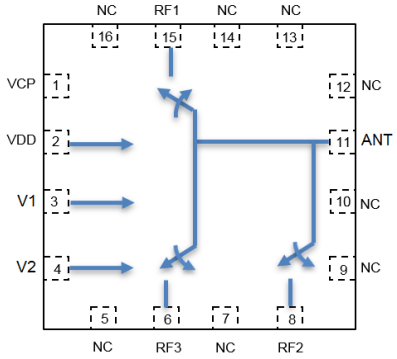


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS7232FK	16 Pin 3×3×0.8mm QFN	Tape and Reel	3000	13” (330mm)	18mm	TS7232FKMTRPBF
Evaluation Board						TS7232FK-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
2	VDD	DC power supply
3	V1	Switch control input 1
4	V2	Switch control input 2
6	RF3	RF port 3
5,7,9,10,12,13,14,16	NC	No internal connection, Can be grounded
8	RF2	RF port 2
11	ANT	Antenna port
15	RF1	RF port 1

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, 800MHz	RFx	40	dBm
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	25	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	39	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+2.7V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Frequency		30		4000	MHz
Insertion Loss, RFx	400MHz		0.35		dB
	800MHz		0.40	0.50	
	1.95GHz		0.50	0.60	
	2.6GHz		0.55	0.65	
	4.0GHz		0.85		
Isolation ANT-RFx	400MHz		50		dB
	800MHz	36	45		
	1.95GHz	28	34		
	2.6GHz	25	30		
	4.0GHz		25		
Return Loss ANT-RFx	400MHz		25		dB
	800MHz		23		
	1.95GHz		22		
	2.6GHz		20		
	4.0GHz		13		
H2	800MHz, Pin=35dBm		-43		dBm
H3	800MHz, Pin=35dBm		-46		dBm
IIP3	800MHz		70		dBm
P0.1dB[1]	0.1dB compression point, 800MHz	40	42		dBm
Switching Time	50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3)		0.7		μs
Control Voltage	Power supply VDD	2.6	3.3	5.5	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control Current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current Consumption, IDD	Active mode		160	200	μA

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	0	ANT-RF1
1	0	ANT-RF2
0	1	ANT-RF3
1	1	All OFF

Attention:

[1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.

[2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-RF1 ON.

9.0 Evaluation Board

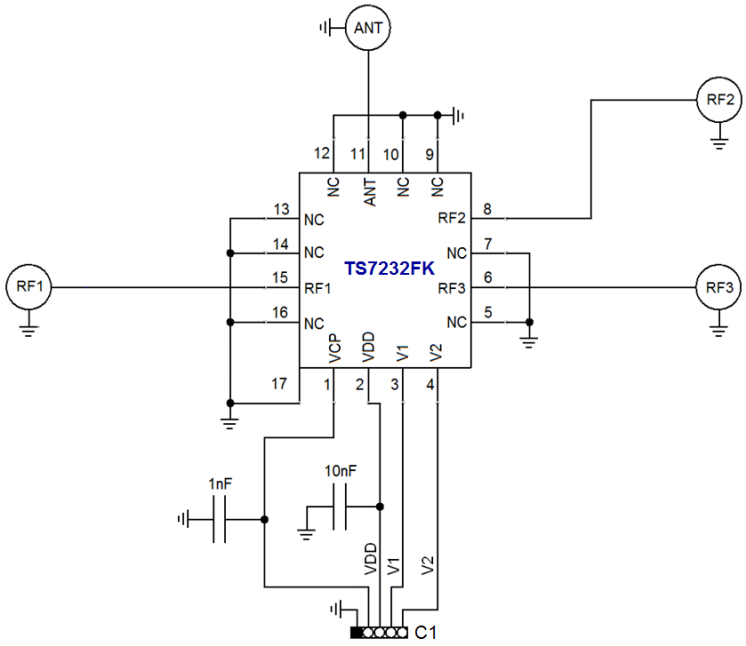


Figure 3 Evaluation Board Schematic

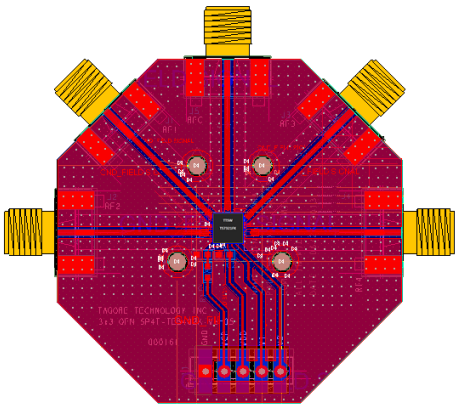


Figure 4 Evaluation Board Image

Attention:

[1] 17 refers to the center pad of the device.

[2] The purpose of connection between VCP and connector C1 is to monitor VCP, do not apply external voltage to VCP.

10.0 Typical Characteristics

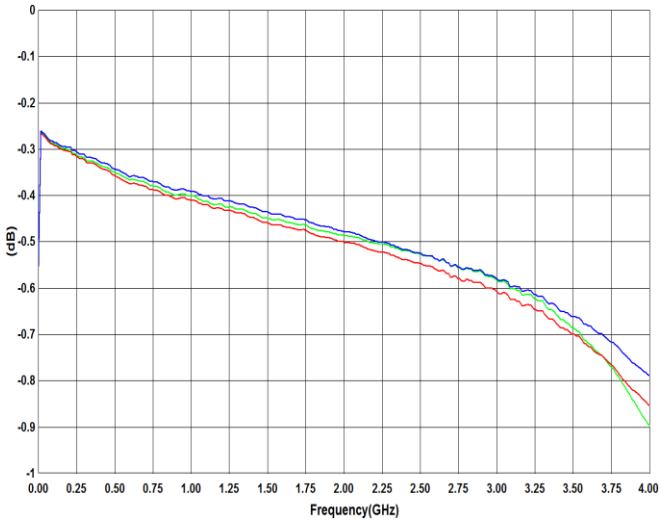


Figure 5 RF1 to RF3 Insertion Loss

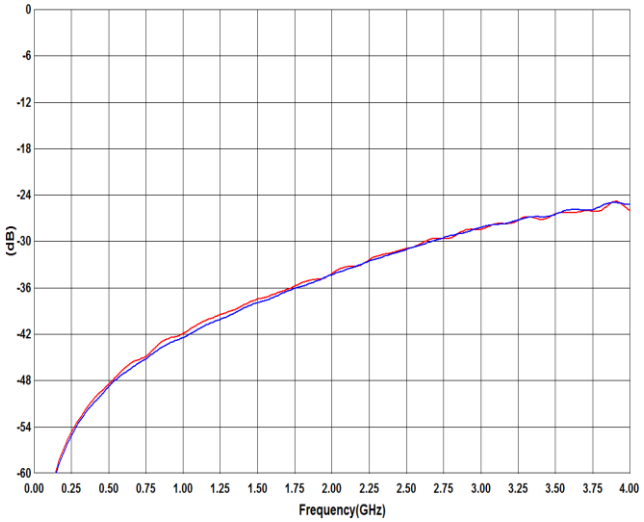


Figure 6 RF1 ON, RF1 Isolation to RF2 to RF3

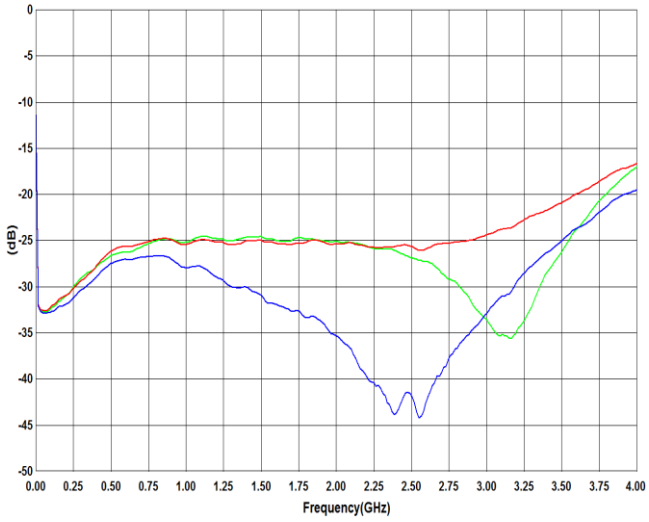


Figure 7 RF1 to RF3 Return Loss

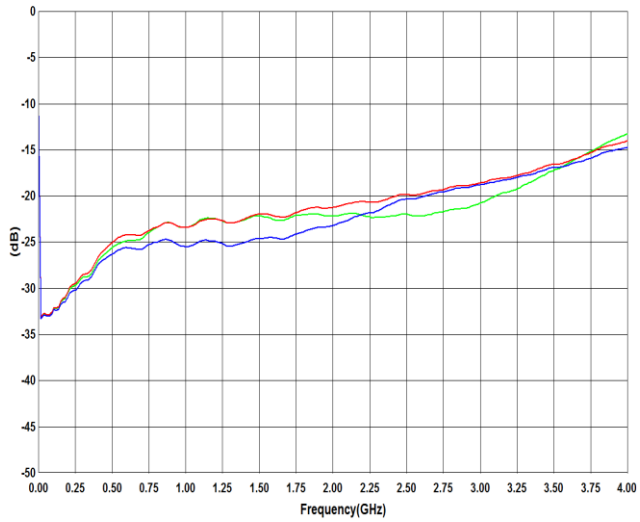


Figure 8 ANT Return Loss

11.0 Device Package Information

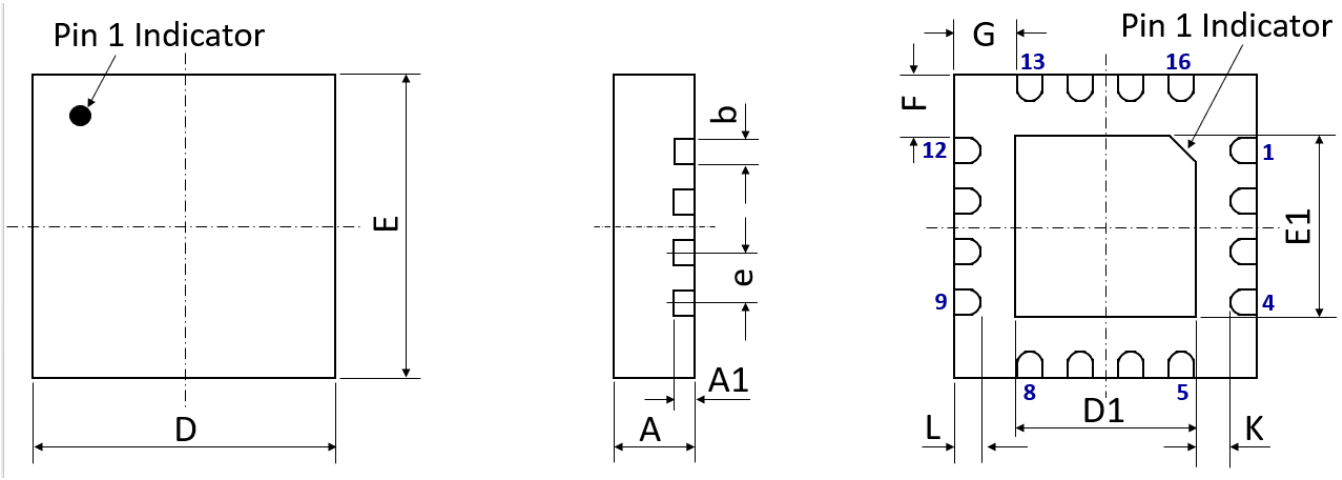


Figure 9 Device Package Drawing
(All dimensions are in mm)

Table 6 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 3(X)×3(Y)=9.

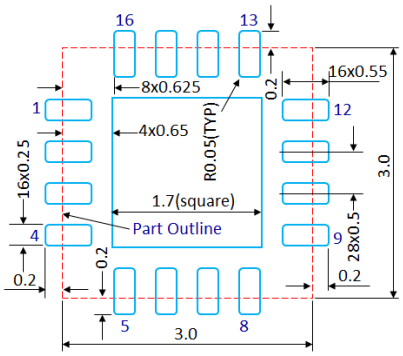
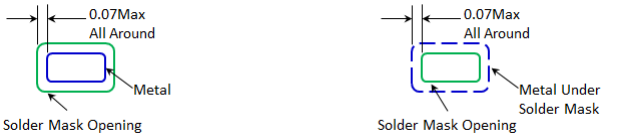


Figure 10 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 11 Solder Mask Pattern
(Dimensions are in mm)

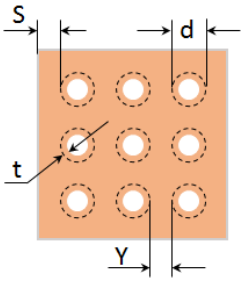


Figure 12 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

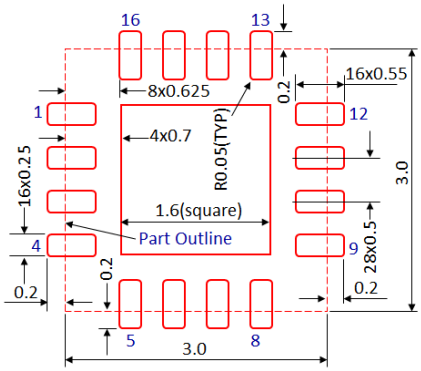


Figure 13 Stencil Openings
(Dimensions are in mm)

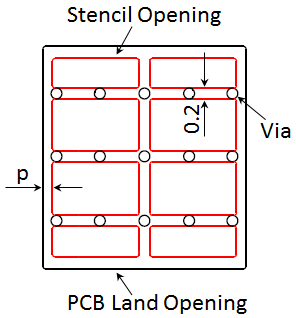


Figure 14 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

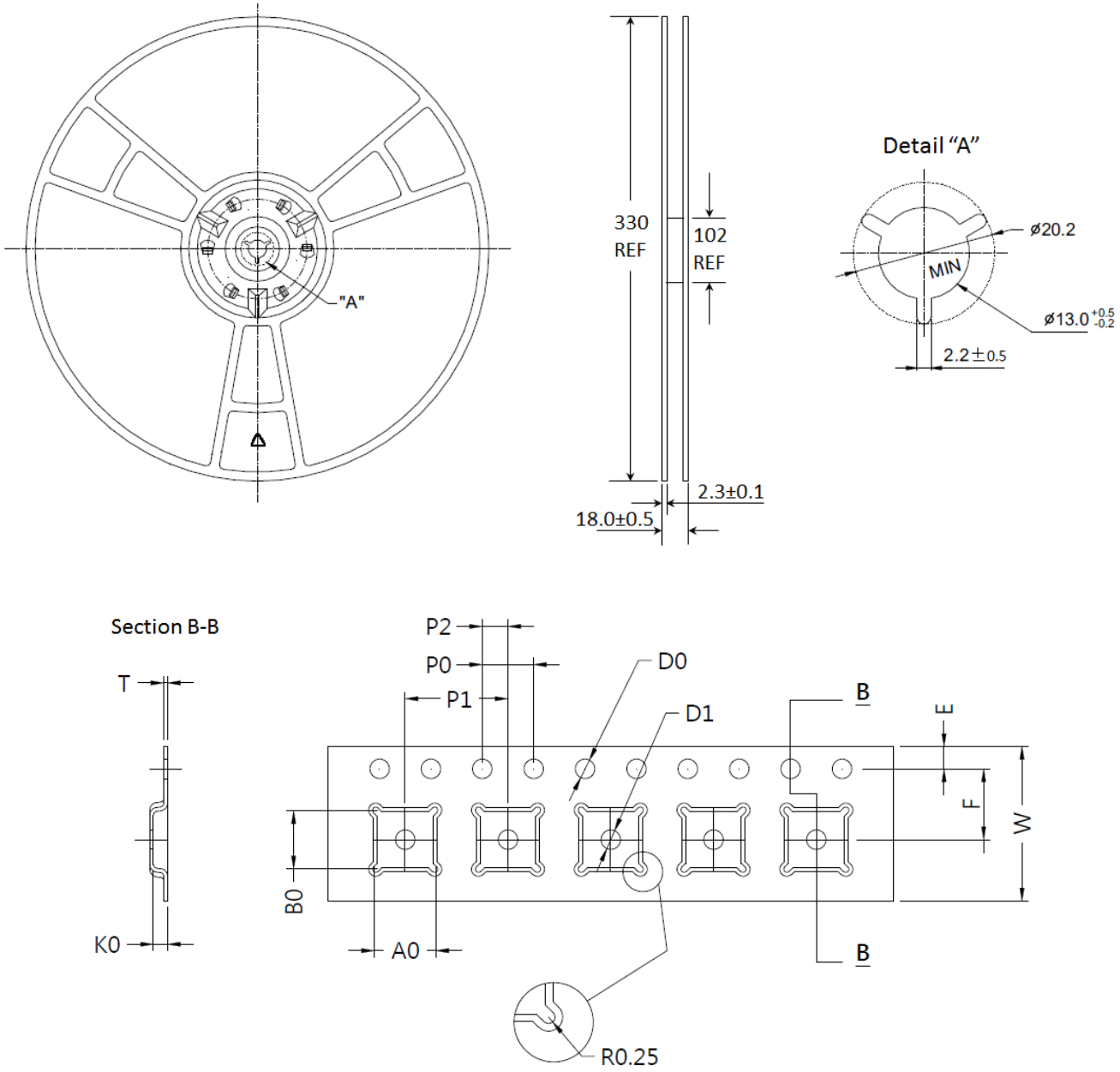


Figure 15 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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