Datasheet

Main Features

- **10-bit Resolution**
- **1.2 Gsps Guaranteed Conversion Rate, 1.4 Gsps Typical**
- **4:1 Integrated Parallel MUX**
- **PECL/LVDS Differential Data and Clock Inputs**
- **2 Vpp Differential Analog Output Swing**
- **Output Impedance: 50Ω Single-ended, 100Ω Differential**
- **Programmable DSP Clock**
- **Power Up Reset for Easy Synchronization of Several DACs**
- **Dual Power Supply: ±5V**
- **CBGA 255 Package for = *C* and *V* Grades**
- **CI-CGA 255 Package for *M* Grade**
- **Evaluation Board TSEV86101G2BGL**

Performance

- **Broadband**
  - **NPR: 49 dB at Fs = 1.2 Gsps: 9.5 bits equivalent (20 MHz to 580 MHz Broadband Pattern, 25 MHz Notch Centered Around 250 MHz)**
- **Single Tone**
  - **SFDR Baseband (Full First Nyquist Zone):**
    70 dBFS at Fs = 1.0 Gsps
    68 dBFS at Fs = 1.2 Gsps
  - **SFDR in Third Nyquist Zone**
    69 dBFS at Fs = 1.2 Gsps, Fout = 5 × Fs/4
    > 60 dBFS at Fs = 1.2 Gsps, Fout = 5 × Fs/4 ±150 MHz (–12 dBm Constant Output Power over 300 MHz Instantaneous Bandwidth)
- **Multi-tone**
  - **Eight-tone IMD: 70 dBFS at Fs = 1.2 Gsps and 500 MHz Baseband**
    Eight Tones Ranging from 80 MHz to 517.5 MHz, 62.5 MHz Spacing
- **Total Power Dissipation = 3.6W**

Applications

- **Direct Digital Synthesis (DDS) for Broadband Applications**
- **Digital Beam Forming**
- **Automatic Test Equipment (ATE)**
- **Instrumentation: Arbitrary Waveform Generator**

Screening

- **Temperature Range:**
  - **C grade: 0°C < T$_C$; T$_J$ < 90°C**
  - **V grade: –40°C < T$_C$; T$_J$< 110°C**
  - **M grade: –55°C < T$_C$; T$_J$ < 125°C**

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1. Description

The TS86101G2B is a 10-bit 1.2 Gsps DAC with an integrated 4:1 multiplexer, allowing easy interfacing with standard FPGAs. The enhanced linearity and Noise Power Ratio (NPR) performance (9.5 bits equivalent at 1.2 Gsps) over 550 MHz instantaneous bandwidth make this product particularly suitable for high-end applications such as arbitrary waveform generators and broadband DDS systems.

2. Specifications

Table 2-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive digital power supply	V_{CCD}		GND to 6.0	V
Negative digital power supply	V_{EED}		−6.0 to GND	V
Negative analog power supply	V_{EEA}		−6.0 to GND	V
Maximum difference between negative supply voltages	V_{EED} - V_{EEA}		0.7	V
Digital inputs Port Y = A/B/C/D	<Y0_T; Y9_T> or <Y0_F; Y9_F>		$V_{IL} > -0.25$ $V_{IH} < 5.5$	V
Maximum difference digital inputs Port Y = A/B/C/D	<Y0_T; Y9_T> <Y0_F; Y9_F>		V_{IH} - $V_{IL} < 1.4$	Vp
Data ready clock input	D_CK_T, D_CK_F		$V_{IL} > -0.25$ $V_{IH} < 5.5$	V
Maximum difference between D_CK_T and D_CK_F	D_CK_T, D_CK_F		V_{IH} - $V_{IL} < 1.4$	Vp
Master clock input	CW_IN_T, CW_IN_F		$V_{IL} > -3.5$ $V_{IH} < 0.75$	V
Maximum difference between CW_IN_T and CW_IN_F	CW_IN_T, CW_IN_F		V_{IH} - $V_{IL} < 1.2$	Vp
Digital shift select voltage	CS		GND to V_{CCD}	V
Maximum junction temperature	T_J		135	°C
Storage temperature	Tstg		−65 to 150	°C
Lead temperature	T_{balls}		250 (during 10s max.)	°C

Notes: 1. Maximum ratings are limiting values only (referenced to GND = 0V), and are to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability. The use of a thermal heat sink is mandatory (refer to "Thermal and Moisture Characteristics" on page 36.)
2. Maximum ratings enable active inputs with MUXDAC power off.
3. Maximum ratings enable floating inputs with MUXDAC power on.

Table 2-2.   Recommended Conditions of Use

Parameter	Symbol	Comments	Typ	Unit
Positive digital power supply	V_{CCD}		5	V
Negative digital power supply[1]	V_{EED}		−5	V
Negative analog power supply[1]	V_{EEA}		−5	V
Differential digital inputs Port Y = A, B, C, D V_{IH} V_{IL} Swing (on each single-ended input)	<Y0_T; Y9_T> <Y0_F; Y9_F>		1.4 1.0 0.2	V V Vp
Differential data ready clock inputs V_{IH} V_{IL} Swing (on each single-ended input)	D_CK_T D_CK_F		1.4 1.0 0.2	V V Vp
Differential master clock inputs Swing (on CW_IN_T)	CW_IN_T CW_IN_F	Single-ended mode: master clock applied on CW_IN_T through 10 nF AC capacitor. CW_IN_F grounded through 10 nF AC capacitor	0.316	Vp
Master clock input power level	PCW_IN_T PCW_IN_F	Single-ended mode	0	dBm
Operating temperature range	T_C, T_J	Commercial "C" grade Industrial "V" grade Military "M" grade	$0°C < T_C$; $T_J < 90°C$ $−40°C < T_C$; $T_J < 110°C$ $−55°C < T_C$; $T_J < 125°C$	°C

Note: 1. V_{EAA} and V_{EED} are internally short circuited through the chip substrate (4Ω equivalent resistance between V_{EEA} and V_{EED}). Therefore, V_{EEA} and V_{EED} must be externally driven by the same power supply source with V_{EEA} and V_{EED} board planes short circuited, and power supply connected to the V_{EEA} plane.

2.1   Electrical Operating Characteristics

Table 2-3.   Electrical Operating Characteristics: V_{CCD} = 5V, V_{EEA} and V_{EED} = –5V, LVDS Input Level, T_J = 85°C

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Resolution		4		10		bits
ESD protection		4	1600			V
Power Requirements						
Positive supply voltage (digital)	V_{CCD}	1	4.75	5	5.25	V
Positive supply current	I_{VCCD}	1		33	40	mA
Negative supply voltage Analog Digital	V_{EEA} V_{EED}	1	–5.25 –5.25	–5 –5	–4.75 –4.75	V V
Negative supply current Analog Digital	I_{VEEA} I_{VEED}	1		380 300	430 340	mA mA
Power dissipation	P_D	1		3.6	4.0	W
Digital Inputs and Data Ready Clock Input						
Logic compatibility			2.5V PECL/3.3V PECL/LVDS			
Digital input voltages (differential): - Logic *0* voltage - Logic *1* voltage - Swing (on each single-ended input) - Common mode	V_{IL} V_{IH} Vp CM	4	–0.2 0.3 0.1 0.2	1.0 1.4 0.2 1.2	2.7 2.9 0.7 2.8	V V Vp V
Input capacitance (die) from each single-ended input to ground		4		2		pF
Input resistance: - Single-ended - Differential		1		50 100		Ω Ω
Master Clock Input (CW_IN_T, CW_IN_F)						
Logic compatibility			ECL/PECL/LVDS (providing AC coupling capacitors)			
AC coupled digital input voltages (differential): Single-ended operation: - Swing (on single-ended input used) Differential operation: - Swing (on each singled-ended input)	Vp Vp	4	0.2 0.1	0.3 0.15	0.8 0.4	Vp Vp
Power level: - Single-ended operation - Differential operation (power on each single-ended input)		4	–4 –10		8 2	dBm dBm
Input capacitance (die)		4		2		pF
Input resistance: - Single-ended - Differential		4		50 100		Ω Ω

Table 2-3. Electrical Operating Characteristics: $V_{CCD} = 5V$, V_{EEA} and $V_{EED} = -5V$, LVDS Input Level, $T_J = 85°C$ (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
DSP Clock Output (DSP_CK_T, DSP_CK_F)						
Logic compatibility		4	PECL/LVDS (providing AC coupling capacitors and pull-down resistors to change the common mode voltage)			
Digital output voltages (true or false signals): - Logic 0 voltage - Logic 1 voltage (only depends on V_{CCD}) - Swing (on each single-ended output) - Common mode voltage	V_{OL} V_{OH} Vpp CM	1	V_{CCD} −0.38 V_{CCD} −0.22 0.15	V_{CCD} −0.35 V_{CCD} −0.16 0.19 4.75	V_{CCD} −0.30 V_{CCD} −0.13 0.22	V V Vpp V
Analog Outputs						
Differential full-scale output voltage (100Ω differentially terminated) Full-scale output power (differential output) Full-scale power at $1/\sqrt{2}$ balun output 50Ω terminated)	(OUT_T, OUT_F) $P_{OUT}D$ $P_{OUT}B$	4		2 7 7		Vpp dBm dBm
Single-ended full-scale output voltage (50Ω terminated) Full-scale output power (single-ended output)	OUT_T or OUT_F $P_{OUT}S$	4		1 4		Vpp dBm
Single ended mid-scale output voltage (50Ω terminated)		5		−600		mV
Output capacitance (from each single-ended output to ground)	C_{OUT}	4		1		pF
Output VSWR (50Ω // 2 pF load on each single-ended output): - From DC to 600 MHz - From 600 MHz to 1.5 GHz	VSWR	4			1.25:1 2.75:1	
Deviation from theoretical Sinx/x (50Ω // 2 pF load on each single ended output at Fs = 1.2 Gsps) Fout up to 600 MHz		4		−1.5	−2.0	dB
AC Performance						
Single tone Spurious free dynamic range[1]: Fs = 600 Msps; Fout = 12.5 MHz (−6 dBFS)	SFDR	4	61 67	65 71		dBc dBFS
Fs = 600 Msps; Fout = 287.5 MHz (−6 dBFS)		1	57 67	62 72		dBc dBFS
Fs = 1.2 Gsps; Fout = 25 MHz (−6 dBFS)		4	58 64	62 68		dBc dBFS
Fs = 1.2 Gsps; Fout = 575 MHz (−6 dBFS)		4	53 63	58 68		dBc dBFS

Table 2-3. Electrical Operating Characteristics: V_{CCD} = 5V, V_{EEA} and V_{EED} = –5V, LVDS Input Level, T_J = 85°C (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Single tone Spurious free dynamic range in third Nyquist zone[2]: assuming an Fs/4 bandwidth centered around 5 Fs/4, with a sin x/x pre-compensation for a constant output power of –12.3 dBm over the band of interest): see Figure 3-6 on page 12. Fs = 1.2 Gsps; Fout = Fs + 150 MHz = 1350 MHz Fs = 1.2 Gsps; Fout = Fs + 450 MHz = 1650 MHz	IF SFDR	4	36 65 39 59	40 69 43 63		dBc dBFS dBc dBFS
SFDR sensitivity over temperature and power supplies range		4			±3	dB
Signal independent spur (clock-related spur) Fs = 1.2 Gsps: Fs/4 power level (first Nyquist zone) Fs/2 Power level (first Nyquist zone)		4		–80 –72		dBm dBm
Signal-to-noise ratio (DC to Nyquist) Fs = 1.2 Gsps; Fout = 375 MHz (–15 dBFS)	SNR	4	58	60		dBFS
Multi-tone inter-modulation: Fs = 1.2 Gsps Four tones at 100 MHz spacing (150 to 450 MHz) (–12 dBFS) Eight tones at 62.5 MHz spacing (80 to 517.5 MHz) (–18 dBFS)	IMD	4	63 65	68 70		dBFS dBFS
Broadband noise power ratio: At –12 dBFS peak to rms optimum loading factor Fs = 1.2 Gsps, 20 to 580 MHz broadband pattern, 25 MHz Notch centered around 250 MHz	NPR	4	47	49		dB
DC Accuracy						
Differential non-linearity	DNL+	4		0.25		LSB
Differential non-linearity	DNL-	4		–0.25		LSB
Integral non-linearity	INL+	4		0.25		LSB
Integral non-linearity	INL-	4		–0.25		LSB
DC gain - Initial gain error[3] - DC gain dispersion[4] - DC gain sensitivity to power supplies - DC gain drift over temperature		1 1 1 4			±3.5% ±2.3% ±1.5% –400	%FS %FS %FS ppm/°C
Mid-scale output voltage[5]		5		–600		mV

Table 2-3. Electrical Operating Characteristics: V_{CCD} = 5V, V_{EEA} and V_{EED} = –5V, LVDS Input Level, T_J = 85°C (Continued)

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Switching Performance						
Maximum operating clock frequency		4	1.2	1.4		Gsps
Minimum operating clock frequency[6]		4			10	Msps

Notes: 1. SFDR is the ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the frequency band DC to Fs/2 (first Nyquist zone).
2. SFDR is the ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the frequency band Fs to 3 × Fs/2 (third Nyquist zone).
3. Initial gain error corresponds to the deviation of the DC gain center value from the unity gain.
4. DC gain dispersion excludes initial gain error.
5. Mid-scale output voltage is measured with a 100Ω differential load on DAC output.
6. Minimum operating clock frequency can be DC. Actually linked to clock input AC coupling external capacitor.

2.2 Timing Characteristics

Table 2-4. Timing Characteristics: 50Ω // 2pF Loading Conditions on Each Single-ended Output. Absolute Timing Values are Given at Package Input/Output Balls

Parameter	Test Level	Min	Typ	Max
Data and data ready maximum allowable input jitter	4			300 ps peak- to-peak
Input data rise/fall time[1] Data ready rise/fall time[1]	4			500 ps 500 ps
Tsetup[2] see Figure 5-2 on page 21 Thold[2] see Figure 5-2 on page 21	4 4	−1.3 ns 2.5 ns		
Input data rate (ports A, B, C and D)	4			350 MWords/s
Input data pulse width (ports A, B, C and D)	4	5.7 ns (at 350 MWord/s)		
CW_IN clock input frequency	4			1400 MHz
CW_IN master clock input jitter[3]	4			1 ps rms
CW_IN to DSP clock output delay with clock shift 0000 CW_IN to DSP clock output delay with clock shift 1111 DSP clock output phase tuning range DSP clock output phase tuning steps	4 4 1 1		2.1 ns + 1 clock cycle 5.2 ns + 1 clock cycle 0 to 3.1 ns 200 ps	
Data ready to CW_IN clock timing: (Figure 5-4 on page 22) Forbidden area	4			600 ps
Pipeline delay[4] TOD[5] TPD[5][6] (propagation delay) Analog output rise/fall time[7]	4		1 clock cycle 3.7 ns Pipeline delay + TOD 180 ps	

Notes: 1. Digital input data rise/fall time: defined between 20% to 80%.
2. Exclusive of period (pp) jitter on both Data and on Data Ready.
3. CW_IN clock input jitter over 5 GHz bandwidth. MUXDAC also operates with CW_IN clock showing more jitter but this may degrade performance (SNR and NPR).
4. Guaranteed by design.
5. See "Definitions of Terms" on page 35.
6. TPD can be directly measured at package input/output, between CW_IN clock and analog output.
7. Full-scale analog output (10% to 90%).

2.3   Explanation of Test Levels

Table 2-5.   Explanation of Test Levels

Num	Characteristics
1	100% production tested at +25°C[1]
2	100% production tested at +25°C, and sample tested at specified temperatures[1]
3	Sample tested only at specified temperatures
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature)
5	Parameter is a typical value only

Notes: 1.   The level 1 and 2 tests are performed at 100 Msps (600 Msps for SFDR performance).
           2.   Only MIN and MAX values are guaranteed (typical values are issued from characterization results).

3.   Typical Characteristics

The device's typical characteristics are the following, unless stated otherwise:

- T_J = 85°C, V_{CCD} = 5V, V_{EEA} = –5V, V_{EED} = –5V
- 100Ω differential output, 0 dBFS = 7 dBm
- Full-scale analog output voltage = 2 Vpp if (50Ω // 2pF) × 2 differentially-terminated
- SFDR up to Nyquist[1]

Figure 3-1.   SFDR at Fs = 1.2 Gsps Against Output Level in Nyquist Conditions (Fout = 575 MHz)
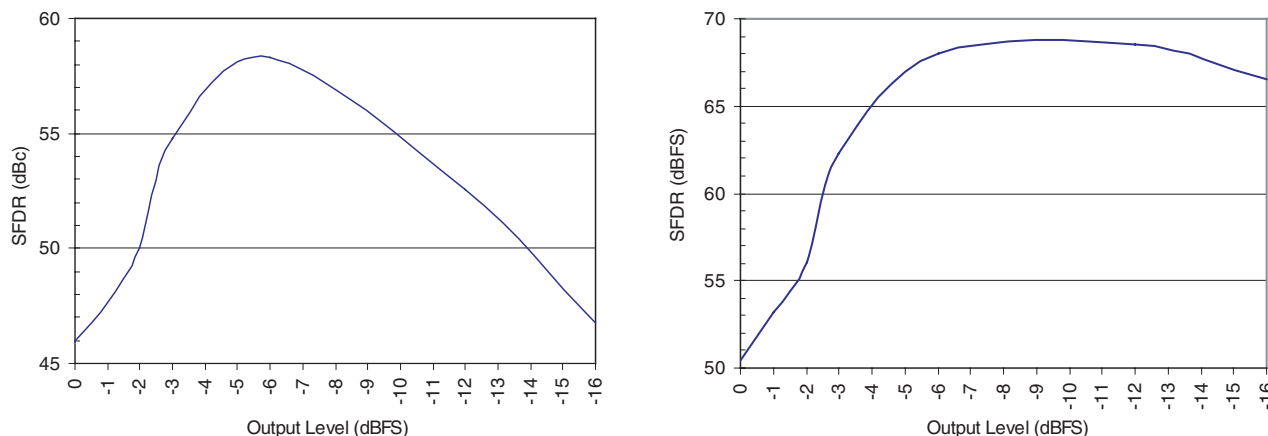
Notes: 1.   SFDR performance (expressed in dBc) is optimum near –6 dBFS.

2. SFDR performance (expressed in dBFS) is quasi-constant for output levels below –6 dBFS. This means that the level of spurs remains quasi-unchanged when lowering the amplitude of the fundamental.

3. SFDR is the ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the frequency band DC to Fs/2.

4. In single-ended operation, 0 dBFS = full-scale = 1 Vpp = 0.5V peak over 50Ω = –6 dBV = 4 dBm. In differential mode, 0 dBFS = full-scale = 2 Vpp = 0.707 V peak over 100Ω = –3 dBV = 7 dBm.

5. The power level at the DAC's output is given by both the digital sinusoidal input level (dBFS) and the theoretical sin X/X deviation, which is Fout-dependent. For example, considering the SFDR with a –10 dBFS digital sinusoidal input and Fout = 499 MHz, Fs = 1 Gsps, the differential output power level of the single tone at Fout = 499 MHz is –6.9 dBm (–10 dBFS = –3 dBm and the theoretical deviation of sin X/X is –3.9 dB in Nyquist).

Figure 3-2. SFDR Against Sampling Rate (Fout/Fs = 0.479) for Three Output Levels (–6 dBFS, –12 dBFS and –16 dBFS)
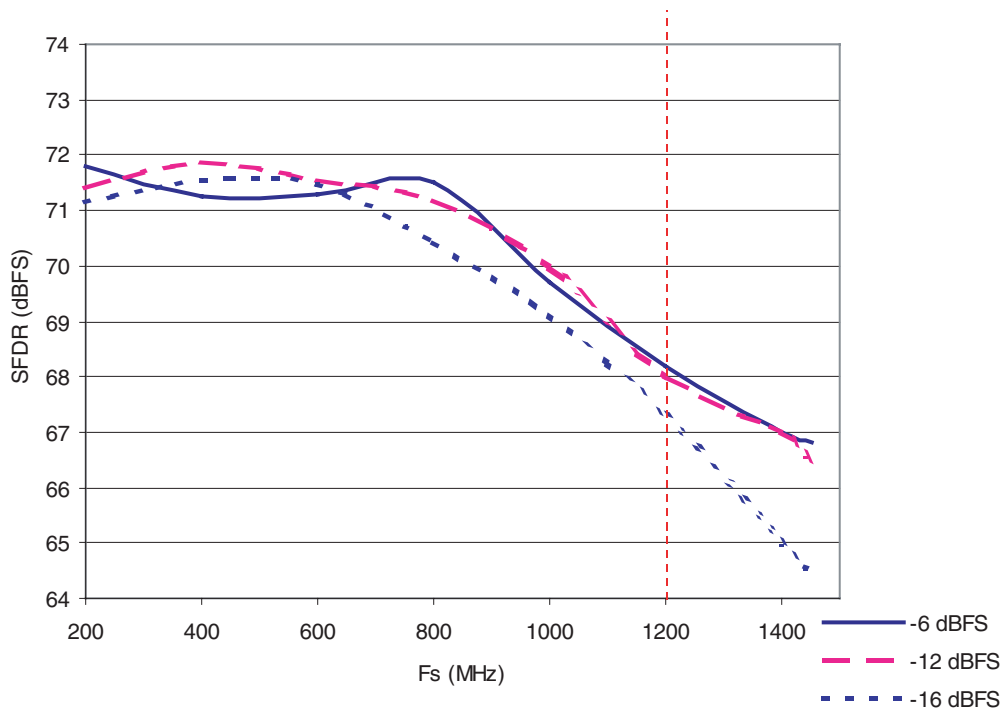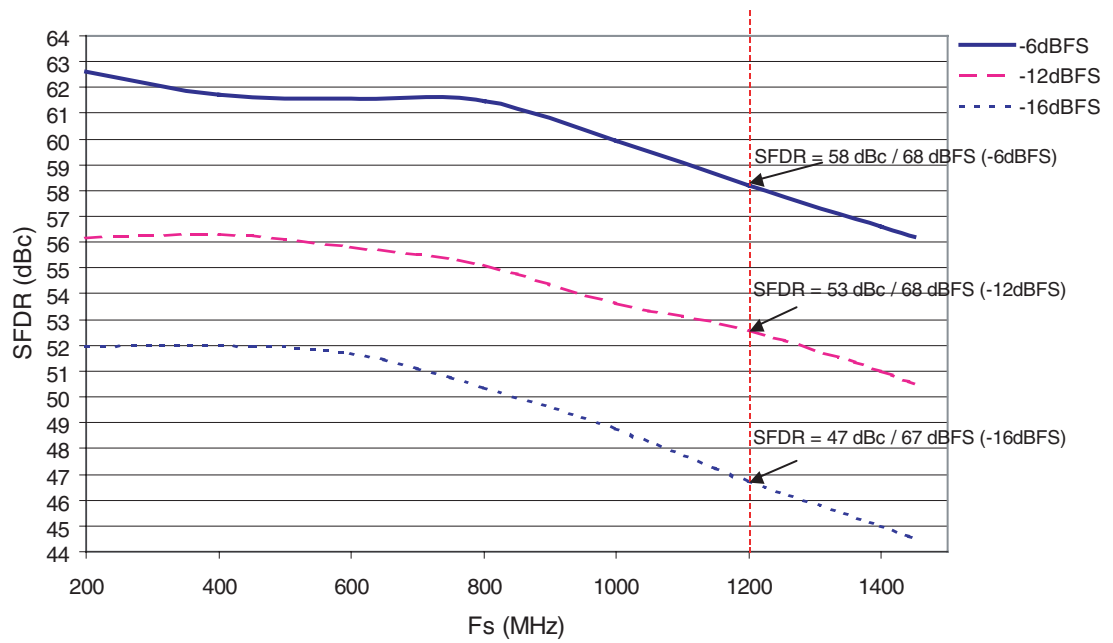
Note: SFDR performances (expressed in dBFS) are quasi-equivalent for output levels below –6 dBFS.

Figure 3-3. Single-tone Spectrum in First Nyquist
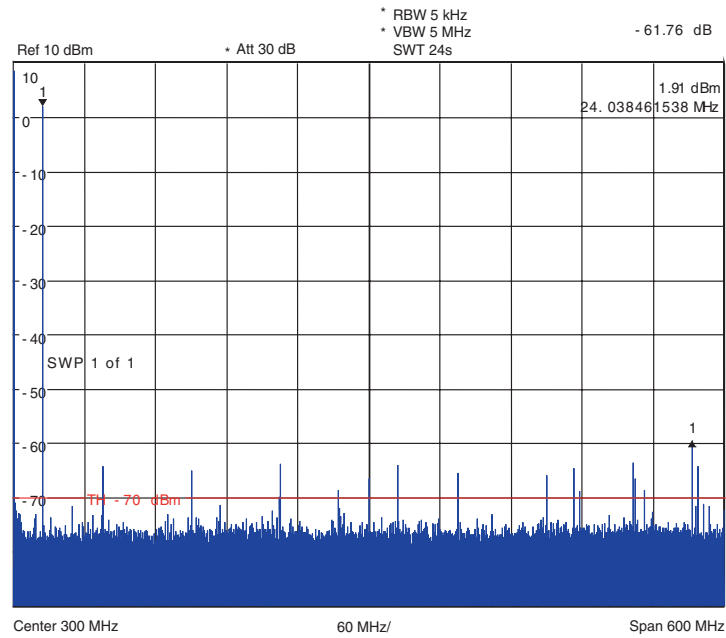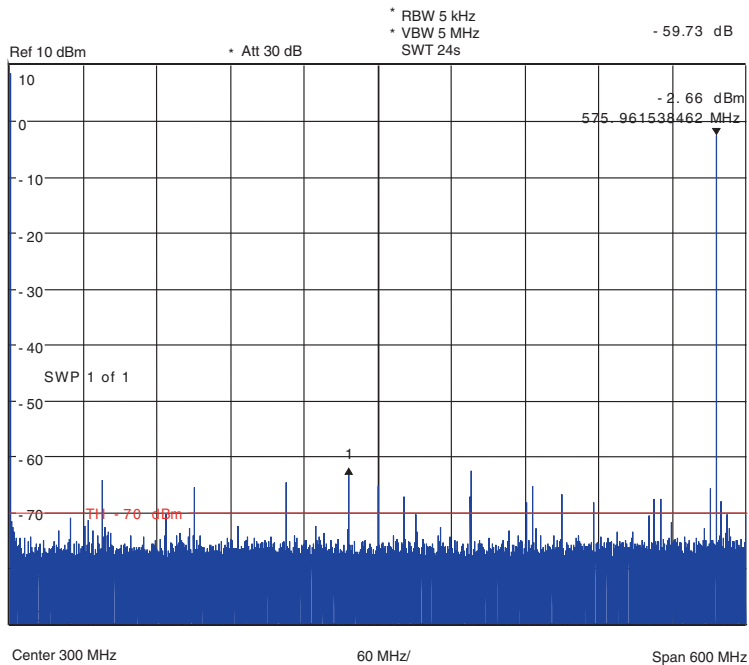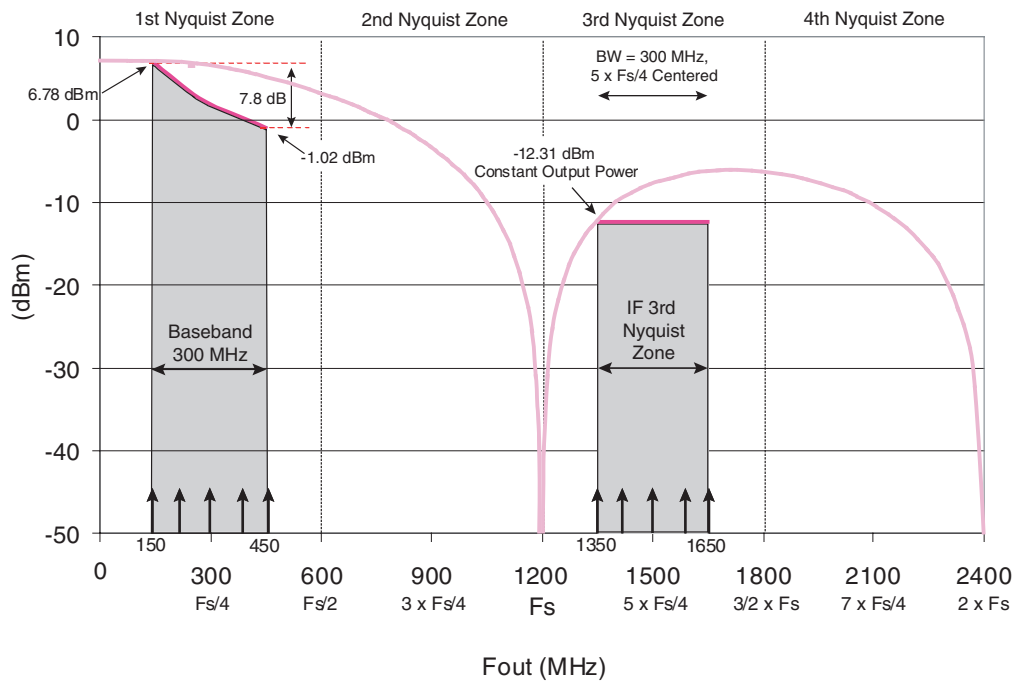Fs = 1.2 Gsps in First Nyquist Zone (Fout = 25 MHz, –6 dBFS) SFDR = 62 dBc (68 dBFS)

Figure 3-4. Single-tone Spectrum in First Nyquist
Fs = 1.2 Gsps in First Nyquist Zone (Fout = 575 MHz, –6 dBFS) SFDR = 59 dBc (69 dBFS)

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Figure 3-5. Signal Dependent Spur SFDR Performance. Sinc Function (from Zero Order Hold Function) DAC Full-scale Differential Output Without Pre-compensation (Fs = 1.2 Gsps)
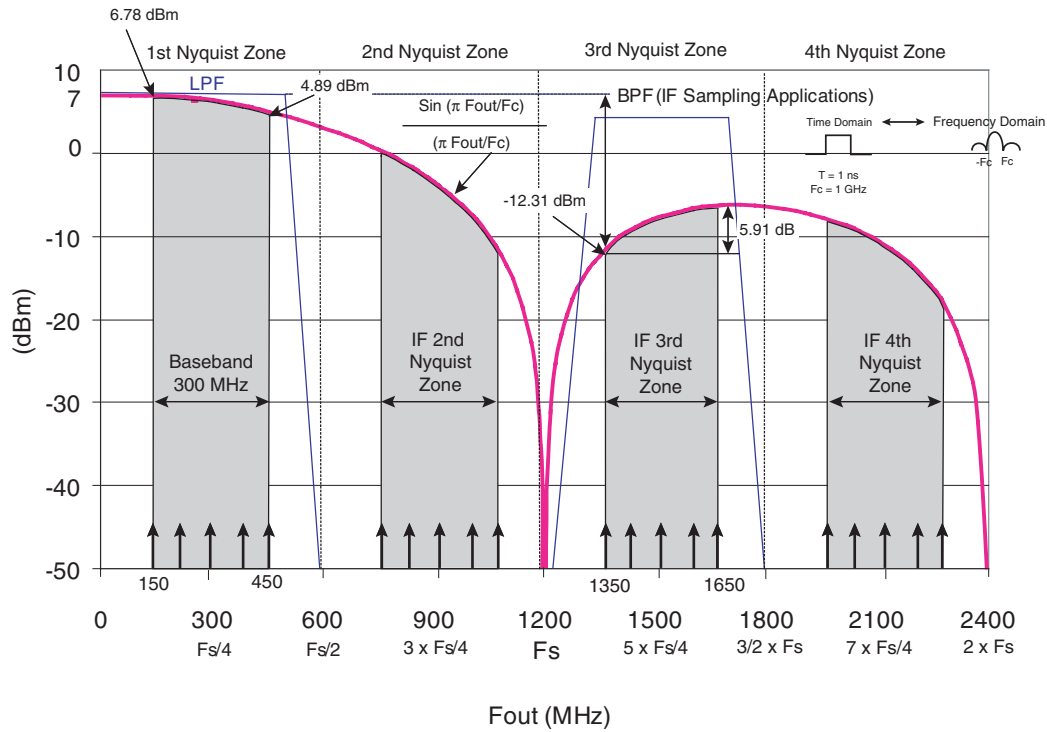
Figure 3-6. Signal Dependent Spur SFDR Performance at 1.2 Gsps, 300 MHz Pattern Width Centered on 5 Fs/4. DAC Full-scale Output with Sinc Pre-compensation for Constant Output Power in Third Nyquist Zone

Figure 3-7.   Single-tone Spectrum in First Nyquist Fs = 1.2 Gsps in First Nyquist Zone
(Fout = 390 MHz, –5.5 dBFS) SFDR = 56 dBc (63 dBFS)
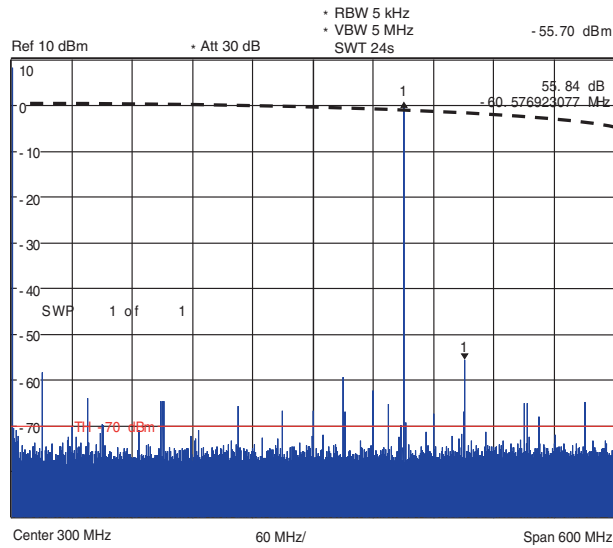
Figure 3-8.   Single-tone Spectrum in Third Nyquist
Fs = 1.2 Gsps in Third Nyquist Zone (Fout = Fs + 390 MHz = 1590 MHz) with Sinc Pre-compensation for
Constant Output Power (–12.31 dBm) in Third Nyquist Zone. SFDR = 44 dBc (64 dBFS)
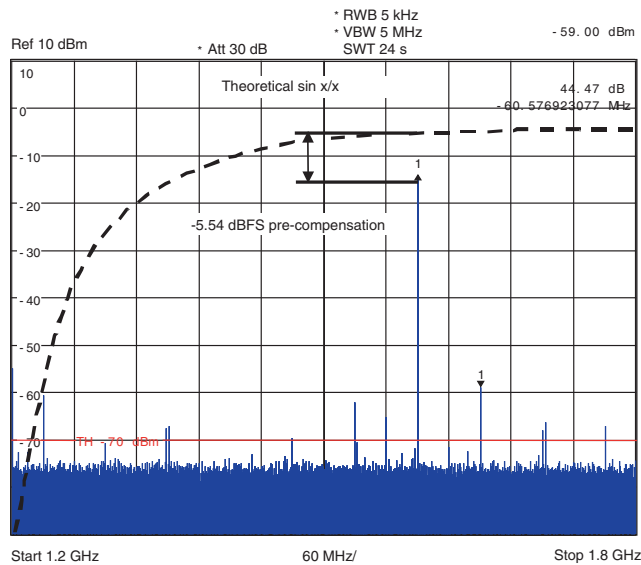
The absolute level of harmonics is equivalent in both the first and third Nyquist zones. The SFDR figures
(in dBFS) are therefore similar in these two Nyquist zones. This shows that the MUXDAC can be used
equivalently in the first and third Nyquist zones with equivalent performances (see Figure 3-9 on page
14).

Figure 3-9. Single-tone SFDR Performance in First and Third Nyquist Zones
Fs = 1.2 Gsps
Fout Ranging from 150 MHz to 450 MHz, with Sinc Pre-compensation for Constant Output Power
(–12.31 dBm) in Third Nyquist Zone
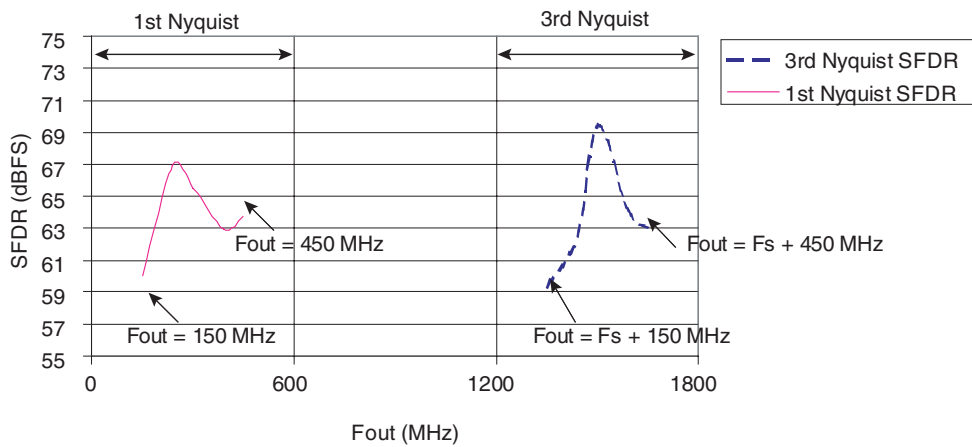
Figure 3-10. Four-tone Spectrum in First Nyquist Zone
Fs = 1.2 Gsps
100 MHz spacing (–12 dBFS): Fout1 = 150 MHz, Fout2 = 250 MHz, Fout3 = 350 MHz,
Fout4 = 450 MHz
Four-tone IMD = 68 dBFS
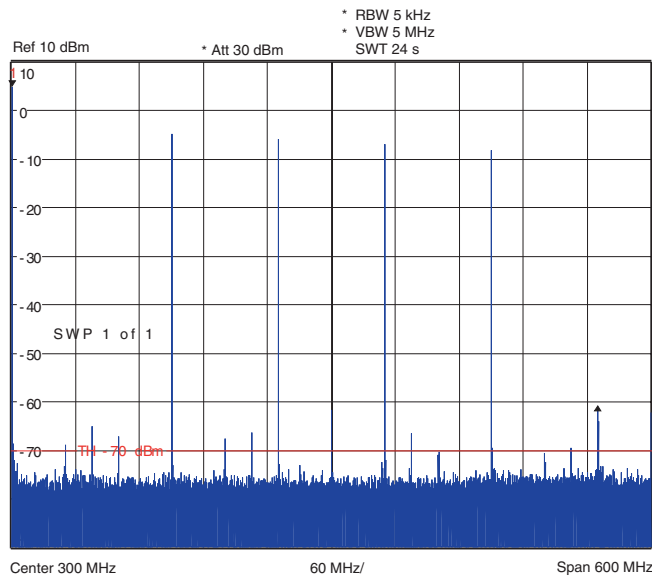
Figure 3-11. Eight-tone Spectrum in First Nyquist Zone
Fs = 1.2 Gsps
62.5 MHz Spacing (–18 dBFS): Fout1 = 80 MHz, Fout2 = 142.5 MHz, Fout3 = 205 MHz, Fout4 = 267.5 MHz, Fout5 = 330 MHz, Fout6 = 392.5 MHz, Fout7 = 455 MHz, Fout8 = 517.5 MHz
Eight-tone IMD = 70 dBFS
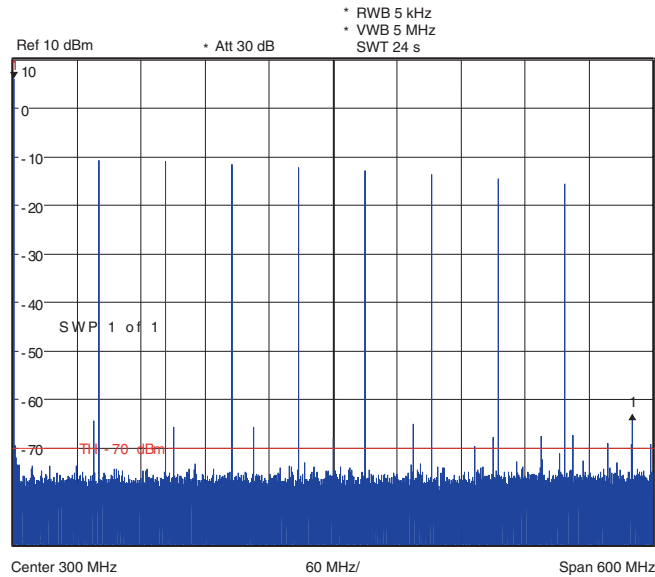
Figure 3-12. Noise Power Ratio (NPR)
Fs = 1.2 Gsps, 20 to 580 MHz Broadband Pattern, 25 MHz Notch Centered Around 250 MHz at –12 dBFS Loading Factor, NPR = 49 dB
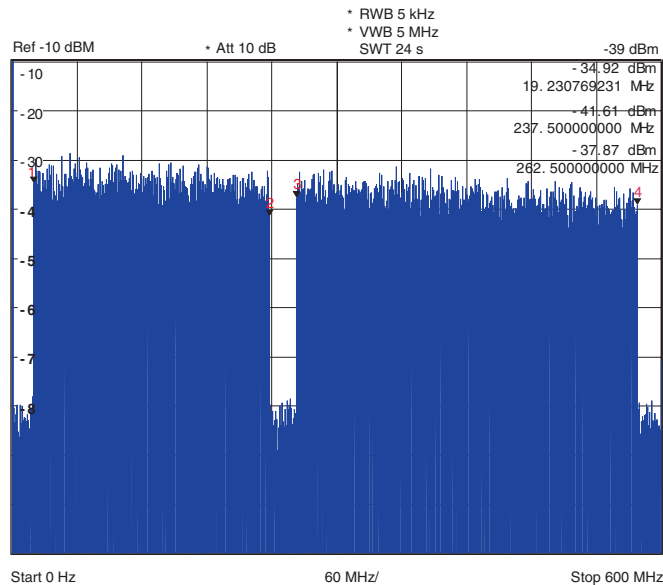
The TS86101G2B DAC can directly synthesize a 550 MHz broadband analog output signal, featuring an equivalent ENOB of 9.5 bits at 1.2 Gsps, for an optimum peak to RMS loading factor of −12 dBFS.

Figure 3-13. Noise Power Ratio (NPR) Against Peak to RMS Loading Factor
Fs = 1.2 Gsps, 20 to 580 MHz Broadband Pattern, 25 MHz Notch Centered Around 250 MHz
Fs = 1.4 Gsps, 20 to 680 MHz Broadband Pattern, 25 MHz Notch Centered Around 250 MHz
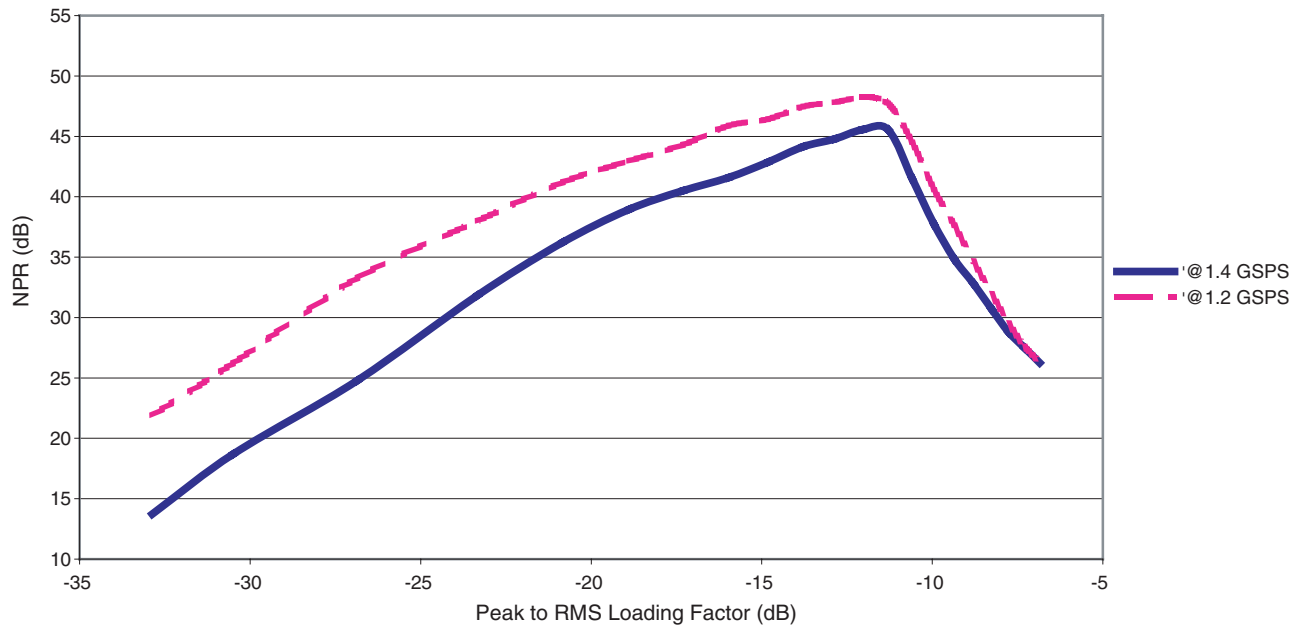
4. Pin Description

Figure 4-1. TS86101G2B Pin Configuration (Top View)

No ball/column on A1 Index Corner

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		AGND	B0T	B1T	B2T	B3T	B4T	DCKT	DCKF	C4T	C3T	C2T	C1T	C0T	AGND	TP	**A**
B	VCCo	VCCo	B0F	B1F	B2F	B3F	B4F	VCCo	VCCo	C4F	C3F	C2F	C1F	C0F	VCCo	VCCo	**B**
C	DGND	DGND	B5T	B6T	B7T	B8T	B9T	VEEo	VEEo	C9T	C8T	C7T	C6T	C5T	DGND	DGND	**C**
D	VEEo	VEEo	DGND	B5F	B6F	B7F	B8F	B9F	C9F	C8F	C7F	C6F	C5F	DGND	VEEo	VEEo	**D**
E	A2F	A0F	A0T	A1F	A1T	VCCo	VCCo	VEEo	VEEo	VCCo	VCCo	D1T	D1F	D0T	D0F	D2F	**E**
F	A2T	A3F	A3T	A4F	A4T	VCCo	DGND	VEEo	VEEo	DGND	VCCo	D4T	D4F	D3T	D3F	D2T	**F**
G	A7F	A5F	A5T	A6F	A6T	VCCo	AGND	AGND	AGND	AGND	VCCo	D6T	D6F	D5T	D5F	D7F	**G**
H	A7T	A8F	A8T	A9F	A9T	DGND	AGND	AGND	AGND	AGND	DGND	D9T	D9F	D8T	D8F	D7T	**H**
J	DGND	DGND	DGND	DGND	DGND	VEEA	AGND	AGND	AGND	AGND	VEEA	DGND	DGND	DGND	DGND	DGND	**J**
K	DGND	DGND	DGND	DGND	DGND	VEEA	AGND	AGND	AGND	AGND	VEEA	DGND	DGND	DGND	DGND	DGND	**K**
L	DGND	DGND	DGND	DGND	DGND	VEEA	VEEA	AGND	AGND	VEEA	VEEA	DGND	DGND	DGND	DGND	DGND	**L**
M	DGND	DGND	DGND	DGND	DGND	VEEA	VEEA	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	DGND	**M**
N	DGND	DGND	DGND	DGND	DGND	VEEA	VEEA	AGND	AGND	AGND	AGND	AGND	VEEA	DGND	DGND	DGND	**N**
P	DSPF	DGND	DGND	DGND	DGND	AGND	AGND	AGND	AGND	AGND	AGND	VEEA	VEEA	VEEA	VEEA	GA	**P**
R	DSPT	DGND	DGND	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	CS0	CS2	VEEA	VEEA	Ref	**R**
T	DGND	DGND	DGND	DGND	AGND	CW_T	CW_F	AGND	OUTF	OUTT	AGND	CS1	CS3	VEEA	TempD	VEEA	**T**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Table 4-1. TS86101G2B Pin Description

Symbol	Pin number	Function
Power Supplies		
DGND	C1, C2, C15, C16, D3, D14, F7, F10, H6, H11, J1, J2, J3, J4, J5, J12, J13, J14, J15, J16, K1, K2, K3, K4, K5, K12, K13, K14, K15, K16, L1, L2, L3, L4, L5, L12, L13, L14, L15, L16, M1, M2, M3, M4, M5, M12, M13, M14, M15, M16, N1, N2, N3, N4, N5, N14, N15, N16, P2, P3, P4, P5, R2, R3, R4, T1, T2, T3, T4	Ground pins
AGND	A2, A15, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, L8, L9, M8, M9, M10, M11, N8, N9, N10, N11, N12, P6, P7, P8, P9, P10, P11, R5, R6, R7, R8, R9, R10, R11, T5, T8, T11	Ground pins
V_{EEA}	J6, J11, K6, K11, L6, L7, L10, L11, M6, M7, N6, N7, N13, P12, P13, P14, P15, R14, R15, T14, T16	Analog negative supply
V_{EED}	C8, C9, D1, D2, D15, D16, E8, E9, F8, F9	Digital negative supply
V_{CCD}	B1, B2, B8, B9, B15, B16, E6, E7, E10, E11, F6, F11, G6, G11	Digital positive power supply
Digital Inputs		
A0_T, A1_T, A2_T, A3_T, A4_T, A5_T, A6_T, A7_T, A8_T, A9_T	E3, E5, F1, F3, F5, G3, G5, H1, H3, H5	In-phase (+) digital input Port A A0_T is the LSB A9_T is the MSB
A0_F, A1_F, A2_F, A3_F, A4_F, A5_F, A6_F, A7_F, A8_F, A9_F	E2, E4, E1, F2, F4, G2, G4, G1, H2, H4	Inverted phase (-) Digital inputs B0_F is the inverted LSB B9_F is the inverted MSB
B0_T, B1_T, B2_T, B3_T, B4_T, B5_T, B6_T, B7_T, B8_T, B9_T	A3, A4, A5, A6, A7, C3, C4, C5, C6, C7	In-phase (+) digital input Port B B0_T is the LSB B9_T is the MSB
B0_F, B1_F, B2_F, B3_F, B4_F, B5_F, B6_F, B7_F, B8_F, B9_F	B3, B4, B5, B6, B7, D4, D5, D6, D7, D8	Inverted phase (-) digital inputs B0_F is the inverted LSB B9_F is the inverted MSB
C0_T, C1_T, C2_T, C3_T, C4_T, C5_T, C6_T, C7_T, C8_T, C9_T	A14, A13, A12, A11, A10, C14, C13, C12, C11, C10	In-phase (+) digital input Port C C0_T is the LSB C9_T is the MSB
C0_F, C1_F, C2_F, C3_F, C4_F, C5_F, C6_F, C7_F, C8_F, C9_F	B14, B13, B12, B11, B10, D13, D12, D11, D10, D9	Inverted phase (-) digital inputs C0_F is the inverted LSB C9_F is the inverted MSB
D0_T, D1_T, D2_T, D3_T, D4_T, D5_T, D6_T, D7_T, D8_T, D9_T	E14, E12, F16, F14, F12, G14, G12, H16, H14, H12	In-phase (+) digital input Port D D0_T is the LSB D9_T is the MSB
D0_F, D1_F, D2_F, D3_F, D4_F, D5_F, D6_F, D7_F, D8_F, D9_F	E15, E13, E16, F15, F13, G15, G13, G16, H15, H13	Inverted phase (-) digital inputs D0_F is the inverted LSB D9_F is the inverted MSB

Table 4-1. TS86101G2B Pin Description (Continued)

Symbol	Pin number	Function
Analog Outputs		
OUT_T	T10	In-phase (+) analog output signal
OUT_F	T9	Inverted phase (-) of analog output signal (Vout)
Clock Inputs		
D_CK_T	A8	In phase (+) PECL/LVDS Data Ready clock input signal. The digital data is loaded on the rising edge of the Data Ready clock signal
D_CK_F	A9	Inverted phase (-) of PECL/LVDS Data Ready clock input signal
CW_IN_T	T6	In-phase (+) of ECL/PECL/LVDS master clock input signal. The analog output is sampled and held on the rising edge of the CW_IN_T signal
CW_IN_F	T7	Inverted phase (-) of ECL/PECL/LVDS master clock input signal
DSP Clock Outputs		
DSP_CK_T	R1	In-phase (+) PECL/LVDS DSP clock output signal. The digital DSP clock
DSP_CK_F	P1	Inverted phase (-) of PECL/LVDS DSP clock output signal
Additional Functions		
CS_0, CS_1, CS_2, CS_3	R12, T12, R13, T13	Selectable shift for DSP output clock (adjust TDSP) *0* = TTL low or GND *1* = TTL high or left open
DIODE	T15	Die junction temperature monitoring
GA	P16	Gain adjust (to be connected to the REF pin)
Ref	R16	Reference for gain
TP	A16	Non-connected pin

5. Functional Description

5.1 Device Overview

The TS86101G2B is a 10-bit 1.2 Gsps DAC with an integrated 4:1 input MUX, designed for synthesization of broadband signals, with enhanced linearity and band flatness performances.

The TS86101G2B is manufactured using full Si bipolar technology. Due to its integrated input 4:1 MUX, this digital-to-analog converter enables the user to address data rates of only ¼ of the effective sampling frequency (up to 350 Msps input rate), facilitating its interface with state-of-the art FPGAs, ASICs and DSPs.

The device requires an input Data Ready clock for the data acquisition as well as an output DSP clock, used for synchronization with the DSP/FPGA/ASIC. This DSP clock is phase programmable thanks to the <CS_0;CS_3> 4-bit clock phase shift select function of the device.

The analog output is 2 Vpp in differential mode or 1 Vpp in single-ended mode and a diode pin is provided for die junction temperature monitoring.

Table 5-1. Description of Functions

Name	Function
V_{EEA}	Analog power supply
V_{EED}	Digital power supply
V_{CCD}	Digital power supply
AGND	Analog ground
DGND	Digital ground
<A0_T:A9_T> <A0_F:A9_F>	Differential input data port A
<B0_T:B9_T> <B0_F:B9_F>	Differential input data port B
<C0_T:C9_T> <C0_F:C9_F>	Differential input data port C
<D0_T:D9_T> <D0_F:D9_F>	Differential input data port D
OUT_T,OUT_F	Differential analog output
D_CK_T, D_CK_F	Differential Data Ready clock inputs
DSP_CK_T DSP_CK_F	Differential DSP clock output
CW_IN_T CW_IN_F	Differential independent master clock input
<CS_0:CS_3>	Shift select for DSP clock (TTL)
DIODE	Die junction temperature monitoring
GA	Gain adjust (to be connected to the REF pin)

Figure 5-1. Device Pinout
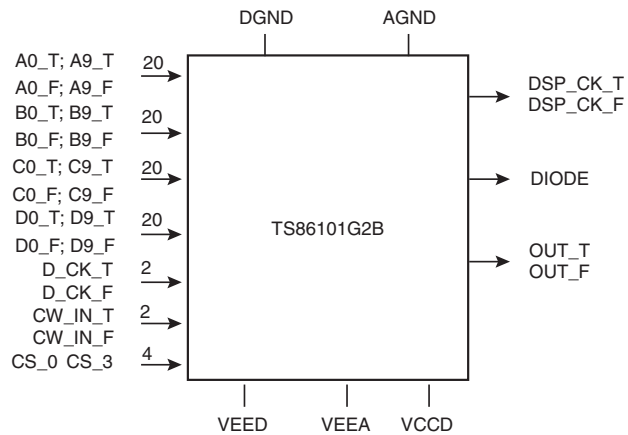
5.2 Registering the Input Data

The 4 × 10-bit differential digital input data patterns (port A: [Ai_T, Ai_F], port B: [Bi_T, Bi_F], port C: [Ci_T, Ci_F] and port D: [Di_T, Di_F]) are loaded in parallel into the first bank of master latches by the rising edge (hold mode) of the differential Data Ready input (D_CK_T,D_CK_F).

Note: The Data Ready duty cycle may vary in accordance with the setup and hold times. The digital data and Data Ready input rates are equivalent to one fourth of the CW_IN master clock frequency. The Data Ready rising edge must be (approximately) centered within the digital data input pulse – a minimum setup and hold time between the data and Data Ready must be observed to ensure enough margin for the input data time jitter and the different systematic skews amongst the data (trace lengths, package skew, etc.).

The registered input data is latched in the second bank of master/slave latches by the rising edge of the CW_IN master clock *divided by 4*. For correct operation, a phase relation between Data Ready and the CW_IN master clock input must be respected (see Figure 5-2).

Figure 5-2. Data or Data Ready (D-CK) Timing

e2v semiconductors SAS 2009
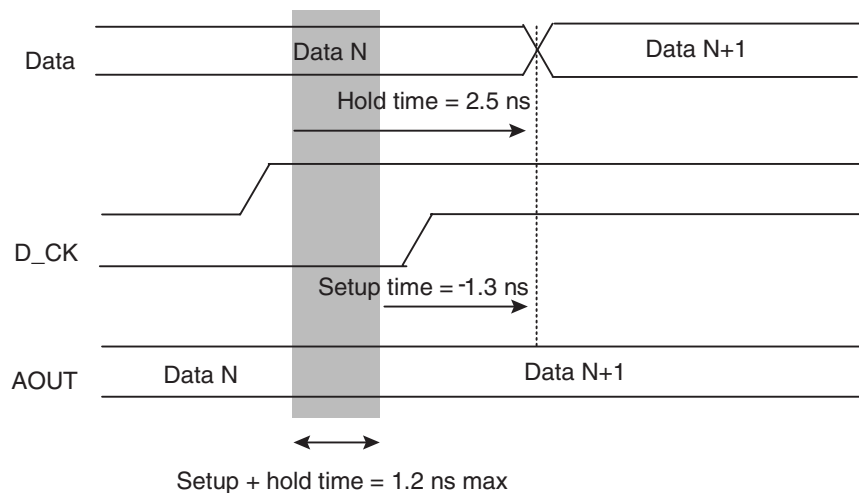
Figure 5-3. Data to Data Clock Forbidden Area
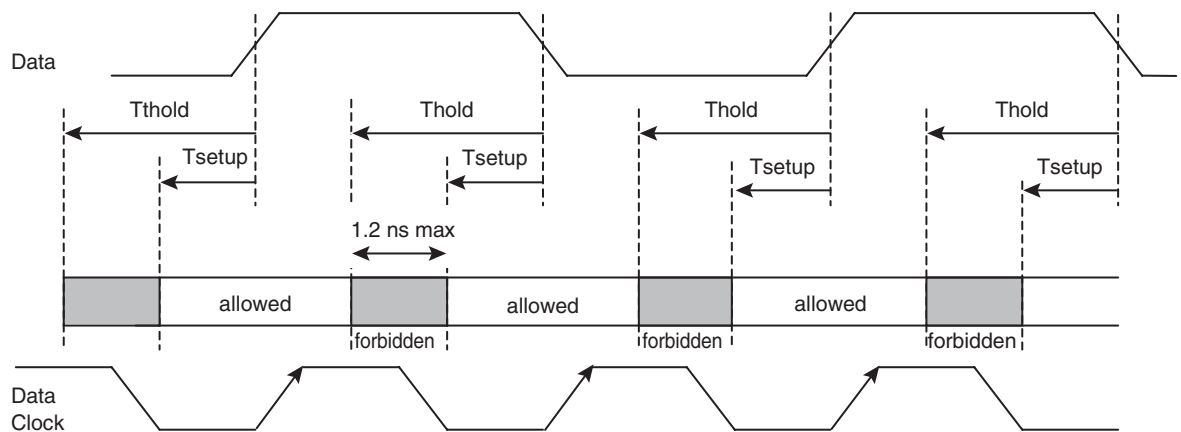
5.3 Phase Relationship Between Data Ready and CW_IN Clock Input

There is a forbidden time range in the phase relation between Data Ready and the CW_IN master clock. This forbidden zone occurs when active rising edges of CW_IN and Data Ready do not comply with the setup and hold times (see Figure 5-4 on page 22). Within this forbidden zone, the data is stored in the second bank of master latches at the time when the first outputs of slave latches switch (acquisition of next incoming data). Within this critical time range of 600 ps, data pattern throughput transmission errors may occur.

To satisfy setup and hold times, the phase of the Data Ready input (D_CK_T to D_CK_F) can be adjusted by choosing one of the 16 DSP clock shift positions (assuming that the DSP providing the data and Data Ready signals to the MUXDAC is clocked by the MUXDAC DSP clock's output signal).

Figure 5-4. Data Ready (D_CK) to CW_IN Master Clock Timing
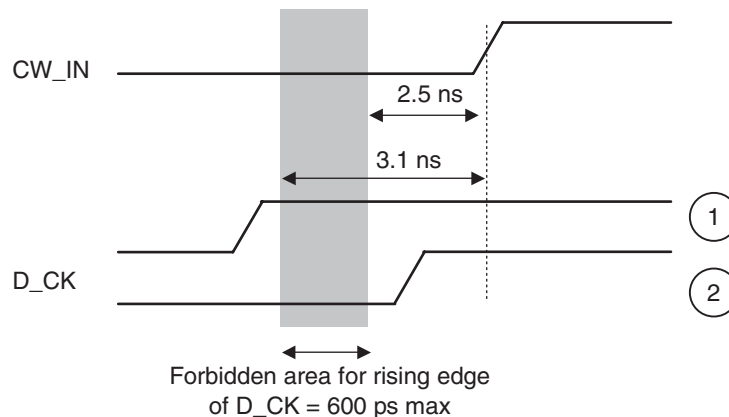
If the D_CK clock edge occurs within the forbidden zone, there is an ambiguity on the data to be transferred from the first to the second bank of latch (data N or data N + 1).

Case 1:

If the D_CK clock edge occurs before the forbidden zone, data N will be transferred internally from the first to the second bank of latch (see).

Case 2:

If the D_CK clock edge occurs after the forbidden zone, data N +1 will be transferred internally from the first to the second bank of latch (see).

5.3.1   Tuning the DSP Clock Output Phase

The DSP clock output phase may be tuned over a range of 3.1 ns in 15 discrete steps of 200 ps each, plus a propagation delay of 2.1 ns (the 2.10 ns value is an absolute timing value measured from CW_IN input ball to DSP Clock output ball), by correctly setting the 4-bit address input CS_0, CS_1, CS_2 and CS_3 from 0000 to 1111:

- 0000: 2.1 ns + 0
- 0001: 2.1 ns + 200 ps
- …
- 1111: 2.1 ns + 3.1 ns

5.3.2   Analog Output Data Switching Information

The analog output data changes on the CW_IN master clock's rising edge, after one clock cycle pipeline delay, plus TOD (output propagation delay). TOD includes the following:

- Propagation time delays of the packaging accesses
- The DAC's core internal conversion time and other internal propagation delays

The typical value of TOD is 3.7 ns, assuming a 50Ω // 2 pF load.

6. Main Features of the TS86101G2B

6.1   Input MUX

The 4:1 integrated input MUX of the TS86101G2B provides the user with the capacity to apply an input data rate four times lower than the effective sampling frequency used:

Data rate = Fs/4 = F(DSP_CK) = F(D_CK)

Where:

- F(DSP_CK) is the frequency of the DSP output clock
- F(D_CK) is the frequency of the Data Ready input clock

Since this input MUX is not programmable, all four ports must be used for proper operation of the DAC.

6.2   Power-up Asynchronous Reset/Synchronization of Several TS86101G2B Devices

A power-on asynchronous reset is integrated on the MUXDAC. It is active during the V_{EED} ramp-up, (up to 50% of its final steady-state value – V_{EEA}/V_{EED} <–2.5V).

To make sure that initialization is effective, the clock should not toggle before V_{EED}/V_{EEA} exceed 90% of their final value.

This asynchronous reset allows correct initialization of the divide/4 timing circuitry that drives the 4:1 MUX, therefore providing synchronous DSP output clock signals (DSP_CK_T,DSP_CK_F) and synchronous analog output signals between multiple DACs.

During the power-up reset phase, the applied (CW_IN_T,CW_IN_F) master clock should not toggle.

For initialization, three clock input configurations are authorized:

• Differential clock input: the master clock can start indifferently at a logical high or low.
• Single-ended clock input on CW_IN_T: the master clock must be at a logical high during reset and start with a falling edge.
• Single-ended clock input on CW_IN_F: the master clock must be at a logical low during reset and start with a rising edge.

In all cases, the first pulse width of the master clock should last at least 100 ps and should not toggle in an undetermined way in order to avoid metastability of the clock.

For DSP systems that require several MUXDACs to be synchronized, the following design and protocol rules apply:

1. The MUXDACs must be powered-up under DSP executive control, with their clocks kept inactive. If used in differential mode (recommended), the clocks should be previously set to either a high or low state, and in any case the clocks should not be toggling.
2. A delay equalling the settling time of the power supplies (time until they reach at least 90% of their steady state) must be respected before proceeding to step 3.
3. The MUXDAC clocks can then be commanded to their active state. In order to reduce the probability of clock meta-stability, the first pulse should last at least 100 ps and should not toggle in an undetermined way.
4. All MUXDAC clock paths within a given DSP should be designed according to the standard high-speed design rules.

Figure 6-1. Synchronization of Multiple TS86101G2B Devices
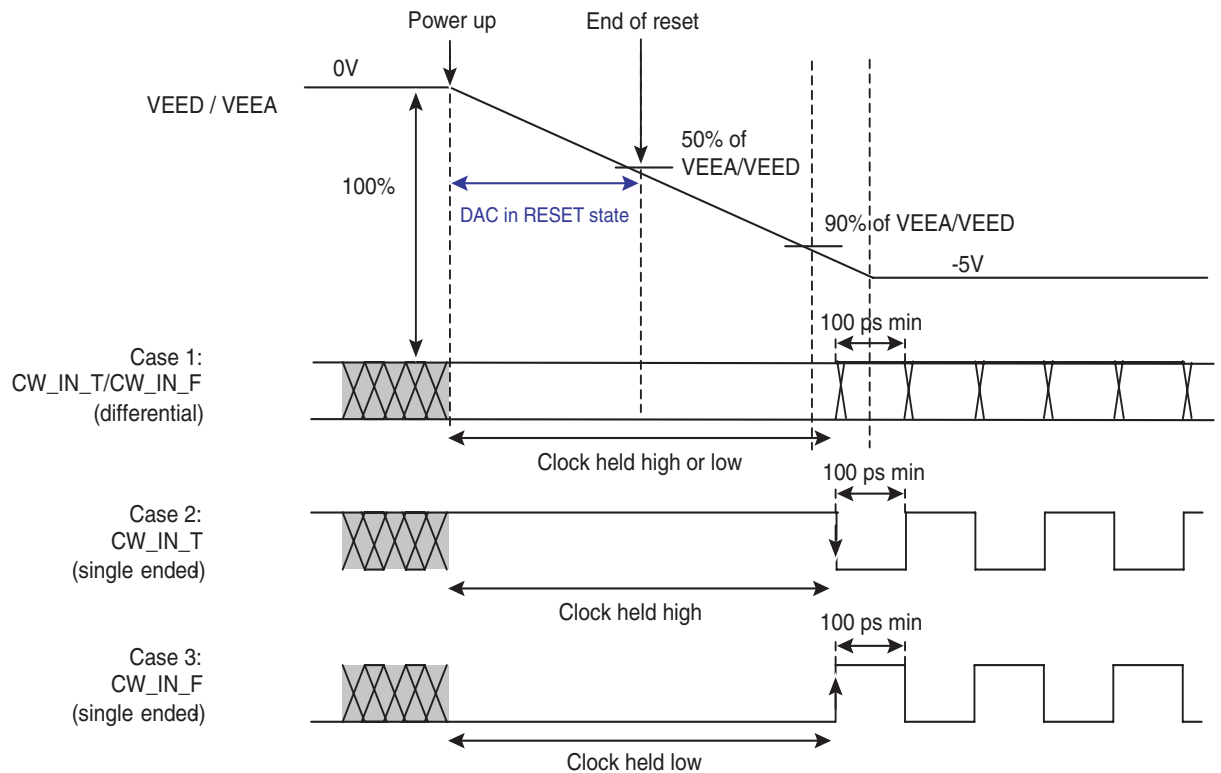
Notes: 1. A counter can be used to determine when the clock can be enabled after power-up.

2. If the clock starts as illustrated below, there is no guarantee that the DACs will start synchronously (they may start on different edges of the clock). It is essential that the clock starts with clean transitions.

Figure 6-2. Clock Transition at Power-up
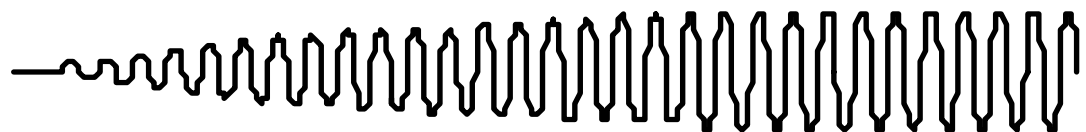
6.3 Programmable DSP Clock

For correct synchronization of the MUXDAC with the DSP/FPGA/ASIC circuit intended to send the digital data to the MUXDAC, a DSP output clock is provided by the MUXDAC.

To finely synchronize the two devices (MUXDAC and DSP/FPGA/ASIC), a programmable delay can be applied to the DSP clock. This delay is controlled via the CS_0, CS_1, CS_2 and CS_3 bits and has a range of 3.1 ns in 200 ps discrete steps.

Please also refer to "Functional Description" on page 20.

The [CS_0;3] bits are TTL signals (*1* = TTL high, 10 kΩ or left open, *0* = TTL low or ground via 10Ω or less) but can also be implemented as shown in Figure 6-3 on page 26.

Figure 6-3. Synchronization of the MUXDAC with DSP/FPGA/ASIC Circuit
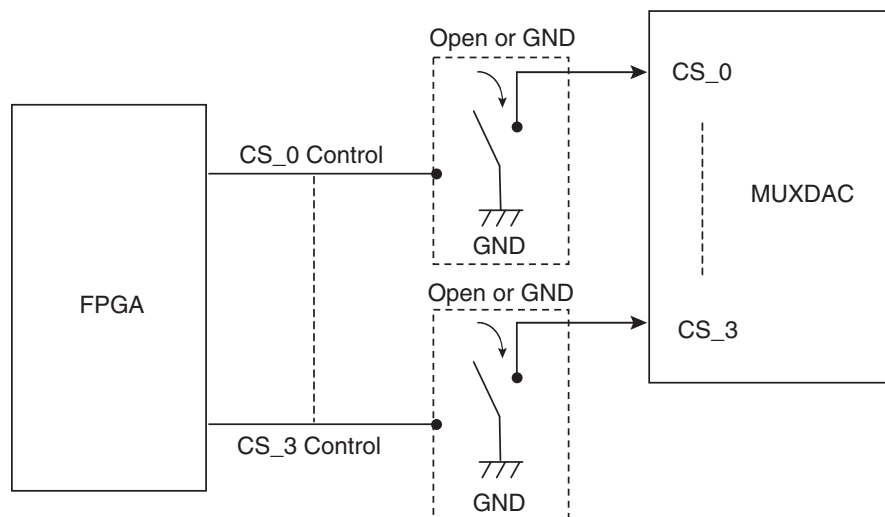
6.4 Diode Pin for Die Junction Temperature Monitoring Function

The diode pin is provided for the die junction temperature monitoring function.

Figure 6-4. Die Junction Temperature Monitoring
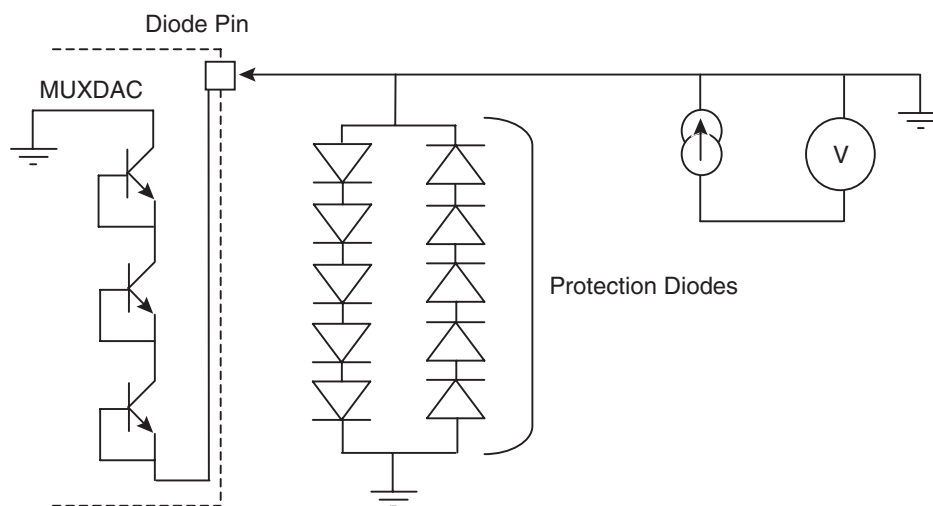
For a given forced current in the diode pin, the voltage across the diode-mounted transistor is linearly dependent on the temperature. Since the characteristic of the diode may vary from one device to another, the voltage across the diode must first be measured to obtain a junction temperature.

Once the diode-mounted transistor is measured, Vbe values according to the junction temperature at I = 1 mA are given in .

Figure 6-5. Vdiode at I = 1 mA
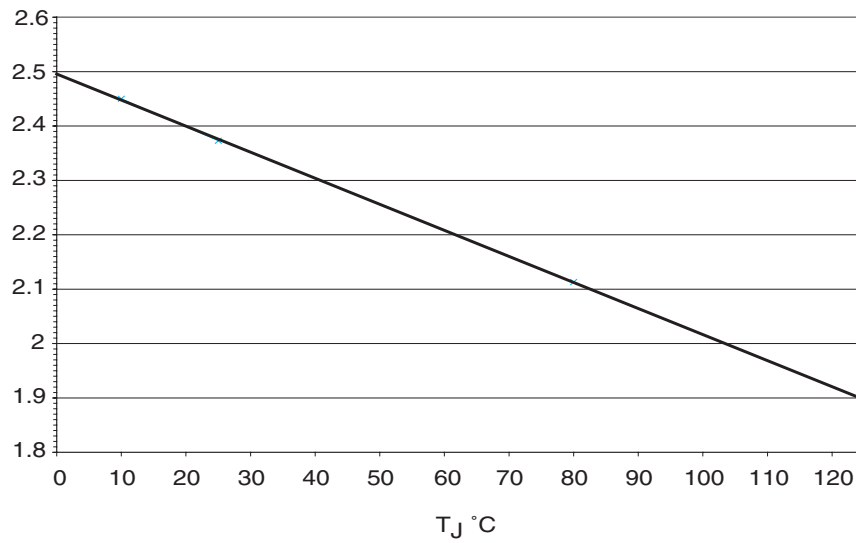
6.5 GA Pin

The GA pin (P16) must be connected to the REF pin (R16) with the shortest possible trace between the two balls/columns as depicted in Figure 6-6.

Figure 6-6. GA Pin

TS86101G2B

7. Block Diagram

Figure 7-1. Block Diagram

8. Timing Diagram

Figure 8-1. Simplified Timing Diagram

Propagation Delay TPD = Pipeline Delay + TOD = 1 Clock Cycle + TOD
TOD Includes Internal Propagation Delay: (Phi4, Tconv and Package Propagation Delay)

Note: All timing parameters are defined under "Definitions of Terms" on page 35.

Figure 8-2. Detailed Timing Diagram

Jitter = 300 ps p.p. max

Tsetup   Thold

TCW

Data In
Port A
Port B
Port C
Port D

Datas N−4 (PORT A)
Datas N−3 (PORT B)
Datas N−2 (PORT C)
Datas N−1 (PORT D)

Datas N (PORT A)
Datas N+1 (PORT B)
Datas N+2 (PORT C)
Datas N+3 (PORT D)

Datas N+4 (PORT A)
Datas N+5 (PORT B)
Datas N+6 (PORT C)
Datas N+7 (PORT D)

Datas N+8 (PORT A)
Datas N+9 (PORT B)
Datas N+10 (PORT C)
Datas N+11 (PORT D)

4 x 10   Data In

Jitter = 300 ps p.p. max

Data Ready
(D_CK_T, D_CK_F)

Shift Range: 3.1 ns
0000   1111

Data Ready

1st Master Latches
Port A and Port B
Port C and Port D

0000

1st Slave Latches
Port A and Port B
Port C and Port D

Data Skew

Shift Range: 3.1 ns
0000   1111

CW Master Clock
(CW_IN_T, CW_IN_F)

F = 1.2 GHz

%2

CW/2 at TMV Output

Tdiv2

Tdiv2

CW/4 at TMV Output

Tdiv2

Tdiv2

%2

CW/2 at TMV Output Delayed

Delay ~ Tdiv2

Delay ~ Tdiv2

CW Resynchro
(CW_IN_T, CW_IN_F)

Tdiv4 ~ 2 x Tdiv2

Tdiv4 ~ 2 x Tdiv2

CW/2

1 CW Period

1 CW Period

CW/4

DSP Out
(DSP_CK_T, DSP_CK_F)

TDSP   Clock Shift

0000   1111

Clock Shift Range:
200 ps to 3.1 ns
(15 steps of 200 ps)

Clock Shift   4   Shift Select

DSP Clock Out

2nd Master Latches
Port A and Port B
Port C and Port D

Datas N−8 (PORT A)
Datas N−7 (PORT B)
Datas N−6 (PORT C)
Datas N−5 (PORT D)

Datas N−4 (PORT A)
Datas N−3 (PORT B)
Datas N−2 (PORT C)
Datas N−1 (PORT D)

Datas N (PORT A)
Datas N+1 (PORT B)
Datas N+2 (PORT C)
Datas N+3 (PORT D)

Datas N+4 (PORT A)
Datas N+5 (PORT B)
Datas N+6 (PORT C)
Datas N+7 (PORT D)

2nd Slave Latches
Port A and Port B
Port C and Port D

Datas N−8 (PORT A)
Datas N−7 (PORT B)
Datas N−6 (PORT C)
Datas N−5 (PORT D)

Datas N−4 (PORT A)
Datas N−3 (PORT B)
Datas N−2 (PORT C)
Datas N−1 (PORT D)

Datas N (PORT A)
Datas N+1 (PORT B)
Datas N+2 (PORT C)
Datas N+3 (PORT D)

Port Select A

Phi 3

Port Select B

Port Select C

Port Select D

Tmux

4 - 1 MUX Output

Data N−8 Data N−7 Data N−6 Data N−5 Data N−4 Data N−3 Data N−2 Data N−1 Data N Data N+1 Data N+2 Data N+3 Data N+4

Phi 4

3rd MS DAC Bank Clock

DAC Bank
3rd Master Latches

Data N−8 Data N−7 Data N−6 Data N−5 Data N−4 Data N−3 Data N−2 Data N−1 Data N Data N+1 Data N+2 Data N+3 Data N+4

DAC Bank
3rd Slave Latches

Data N−8 Data N−7 Data N−6 Data N−5 Data N−4 Data N−3 Data N−2 Data N−1 Data N Data N+1 Data N+2 Data N+3 Data N+4

Tdiv 4 + Phi 3

Phi 4

Tconv   1 Pipeline Delay

TPD

Analog Output
(OUT_T, OUT_F)
1 Vpp Single on 50Ω
2 VPP Differential on 100Ω

Data N − 8   Data N − 6   Data N − 5   Data N − 3   0   Data N + 1   Data N + 3

0

Data N − 7   Data N − 4   Data N − 2   Full-scale Step   Data N + 2

Data N −1

DSP

Propagation Delay TPD = Pipeline Delay + TOD = 1 Clock Cycle + TOD
TOD Includes Internal Propagation Delay: (Phi4, DAC Core Conversion Time and Package Propagation Delay)

Note: All timing parameters are defined under "Definitions of Terms" on page 35.

9. Equivalent Input/Output Schematics

Figure 9-1.   Equivalent Digital Input Circuit and ESD Protections (Input Data and Data Ready Input Clock)
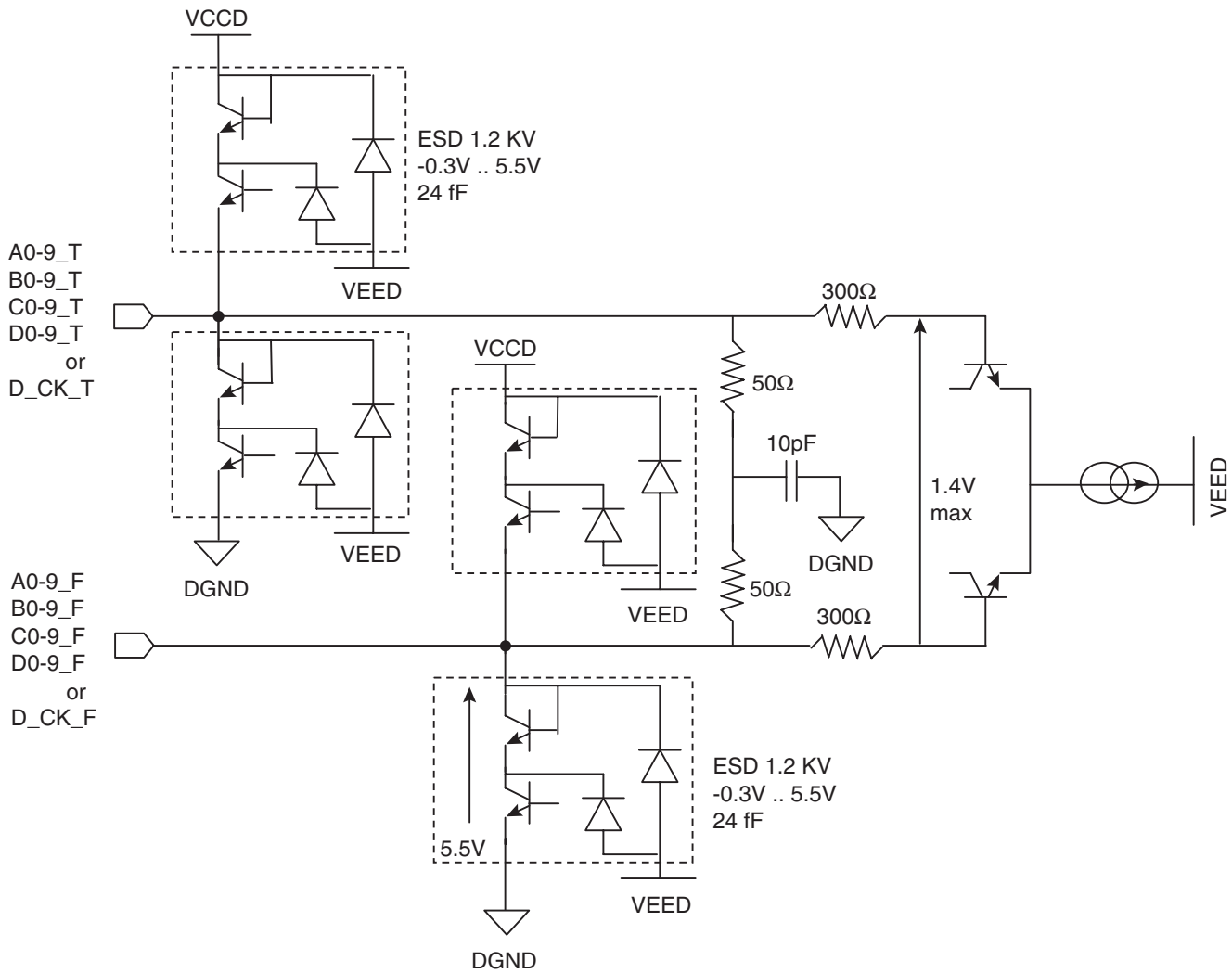
Figure 9-2. Equivalent CW_IN Master Input Clock Circuit and ESD Protections
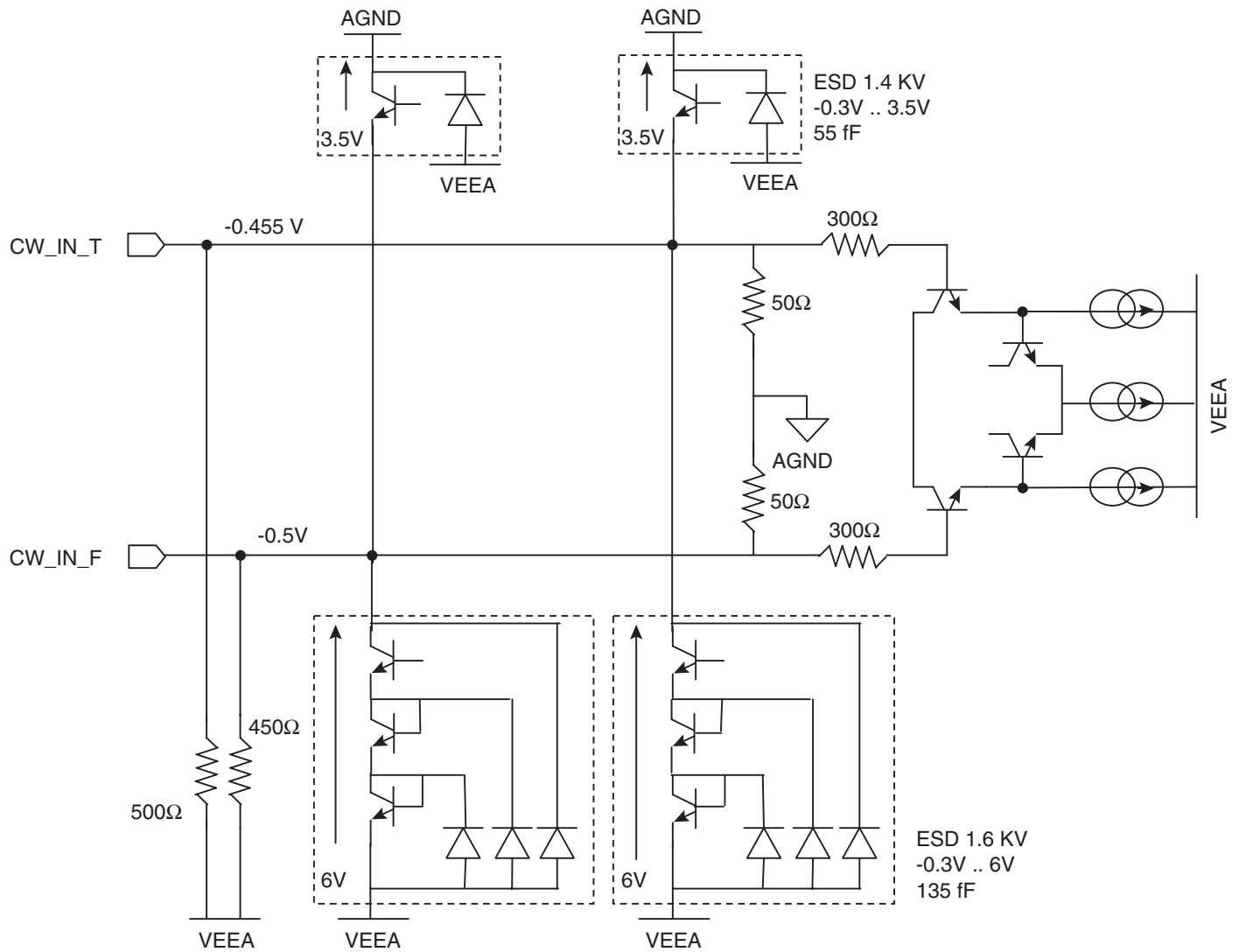
Figure 9-3. Equivalent DSP Clock Output Buffer and ESD Protections
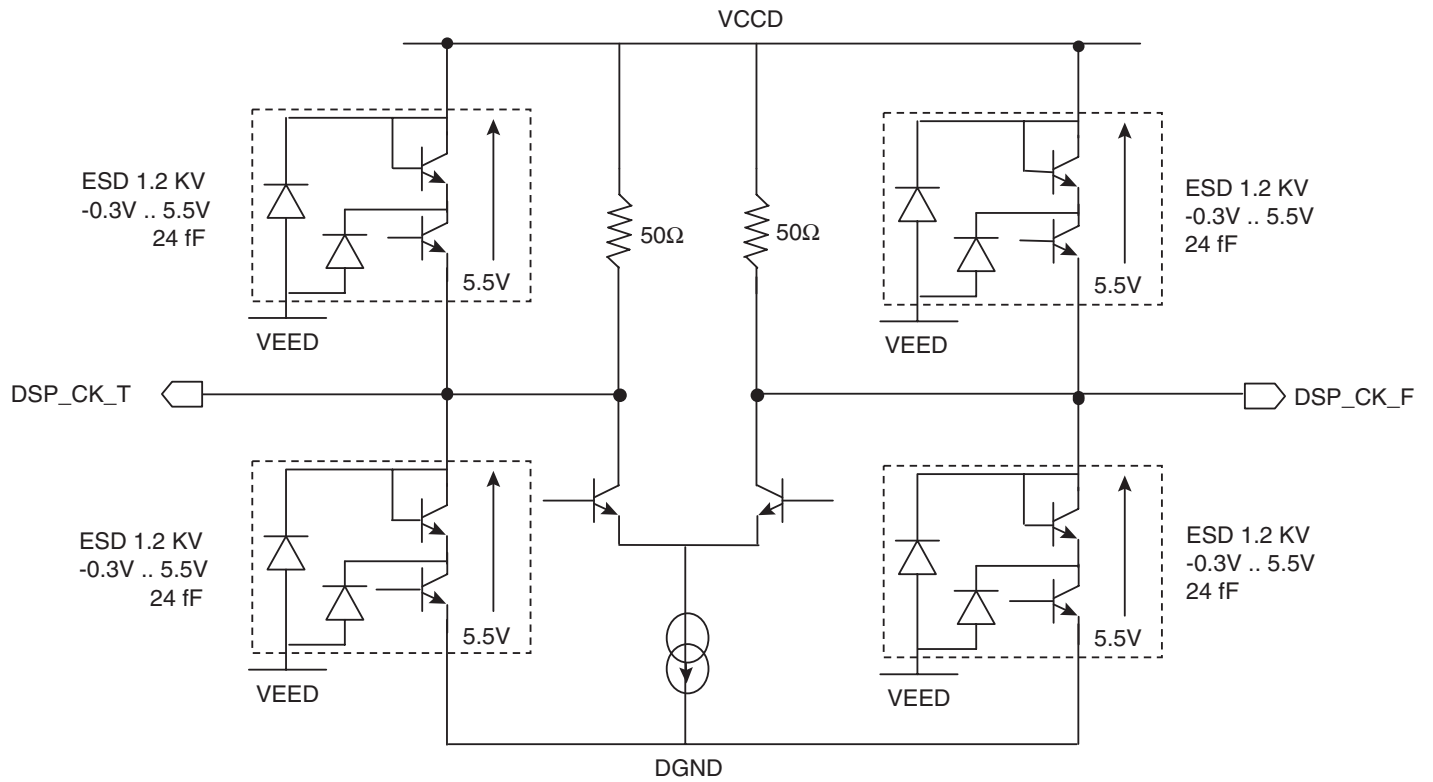
Figure 9-4. Equivalent DAC Analog Output and ESD Protections
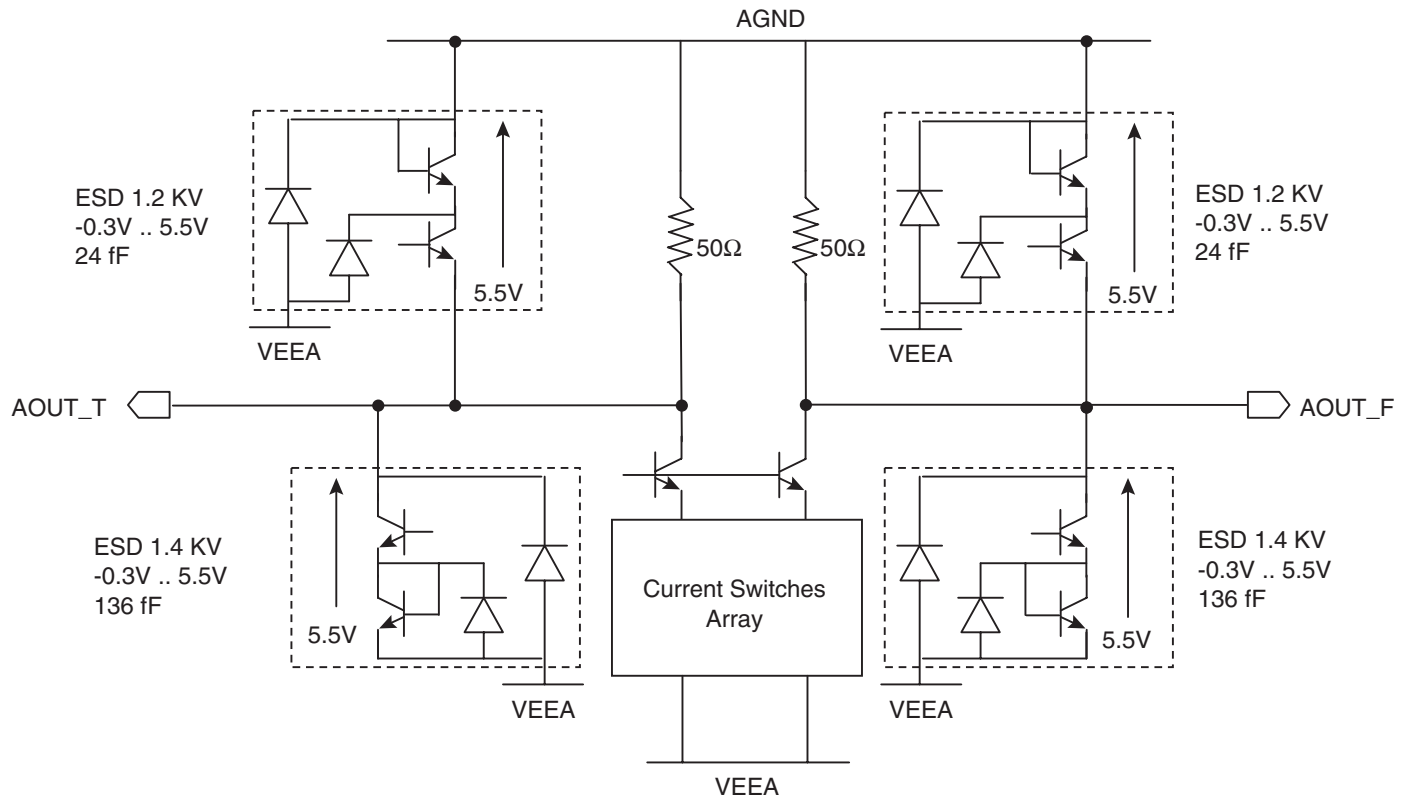
10. Definitions of Terms

Table 10-1. Definitions of Terms

Abbreviation	Definition	Description
(ACPR)	Adjacent Channel Power Ratio	The ratio in dB between the power in the adjacent channel and the power in the channel carrying the modulated signal
(DNL)	Differential Non-linearity	The maximum deviation in the output step size from the ideal value of one least significant bit (LSB). A DNL of –1 LSB means that a DAC converter guarantees the transfer function is monotonic
(FSR)	Full-scale Range	The maximum difference between the highest and lowest input levels for which various device performance specifications prevail, unless otherwise noted
(IMD)	Inter-modulation Distortion	The two tones intermodulation (IMD) rejection is the ratio of either output tone to the worst intermodulation products. The output tone levels are at –6 dB full-scale
(INL)	Integral Non-linearity	The maximum deviation of the output transfer curve at each code from the ideal one after the gain and offset error are corrected
(NPR)	Noise Power Ratio	The NPR is measured to characterize the DAC's capacity to synthesize a broadband signal. When using a notch-filtered broadband white-noise DAC input pattern, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitude at the DAC's output spectrum
(SFDR)	Spurious Free Dynamic Range	The ratio expressed in dB of the RMS signal amplitude to the RMS value of the next highest spectral component (peak spurious spectral component) measured in the frequency band DC to Fclk/2. SFDR is the key parameter for selecting a converter to be used in a frequency domain application. It may be reported in dBc (degrades as signal levels are lowered) or in dBFS (always full-scale when related back to the converter)
(SINAD)	Signal-to-Noise and Distortion Ratio	The ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics except DC
(SNR)	Signal-to-noise Ratio	The ratio expressed in dB of the RMS signal amplitude to the RMS sum of all other spectral components excluding the first five harmonics
(THD)	Total Harmonic Distortion	The ratio expressed in dBc of the RMS sum of the first 10 harmonic components, to the RMS value of the measured fundamental spectral component
TDSP		The time delay between the rising edge of the CW_IN master clock and the active DSP clock rising edge for a clock shift of 0000
THold	Hold Time	The time difference between the rising edge of the differential Data Ready input (zero crossing) and a point of change of the digital input data (zero crossing of differential input)
TPD/TOD	Output Propagation Delay	The analog output propagation delay. Measured between the rising edge of the differential CW_IN clock input (zero crossing point) and the zero crossing point of a full-scale analog output voltage step. TPD corresponds to one CW_IN clock cycle pipeline delay plus an internal propagation delay (TOD) including package access propagation delays and internal (on-chip) delays such as clock input buffers and DAC conversion times
TSetup	Set-up Time	The time difference between the point of change of the digital input data (zero crossing of differential input) and the rising edge of the differential data ready input (zero crossing)
(VSWR)	Voltage Standing Wave Ratio	The VSWR corresponds to the DAC output insertion loss due to output power reflection. As a reminder, a VSWR of 1.12 corresponds to a 20 dB return loss (99% power transmitted and 1% reflected) and therefore to a 0.0436 dB transmission loss

11. Thermal and Moisture Characteristics

**Figure 11-1.** Simplified Thermal Model for CBGA 255 Package
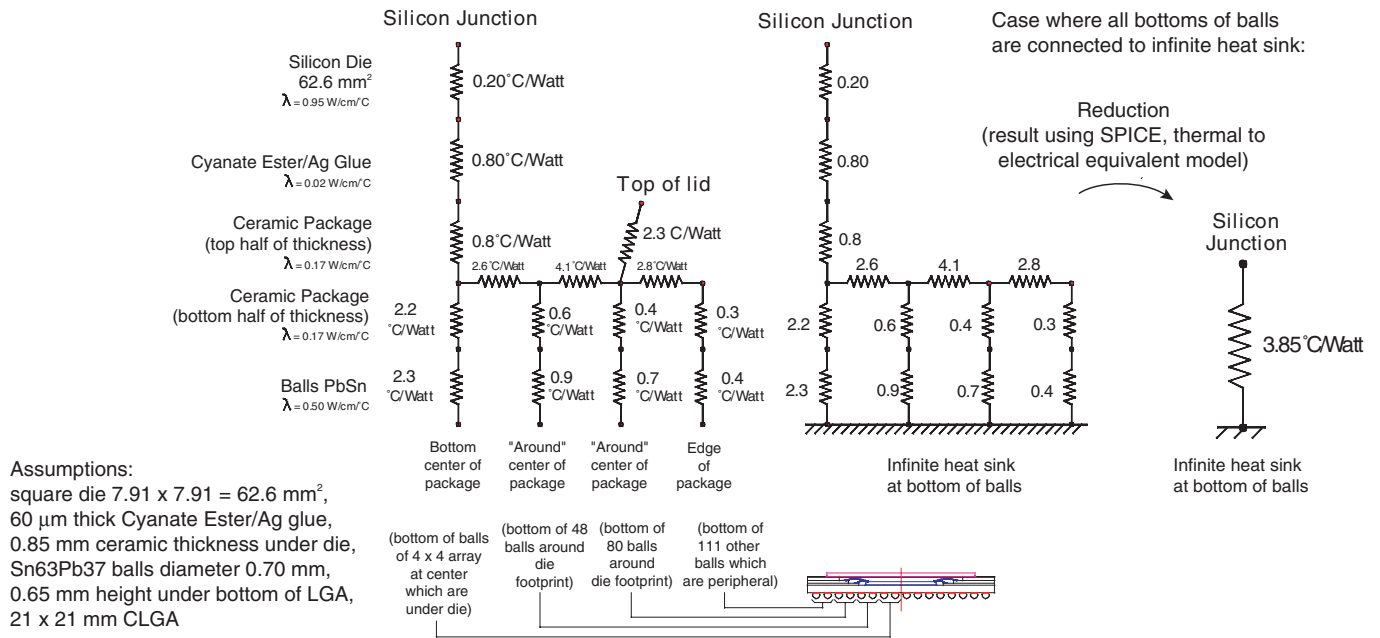
Notes: 1. Typical values, assuming that the power dissipation is uniform over 25% of the die's top surface, are extracted from ANSYS® thermal simulation.

  2. CBGA 255 package is hermetic.

Figure 11-2. Simplified Thermal Models for CI-CGA 255 Package
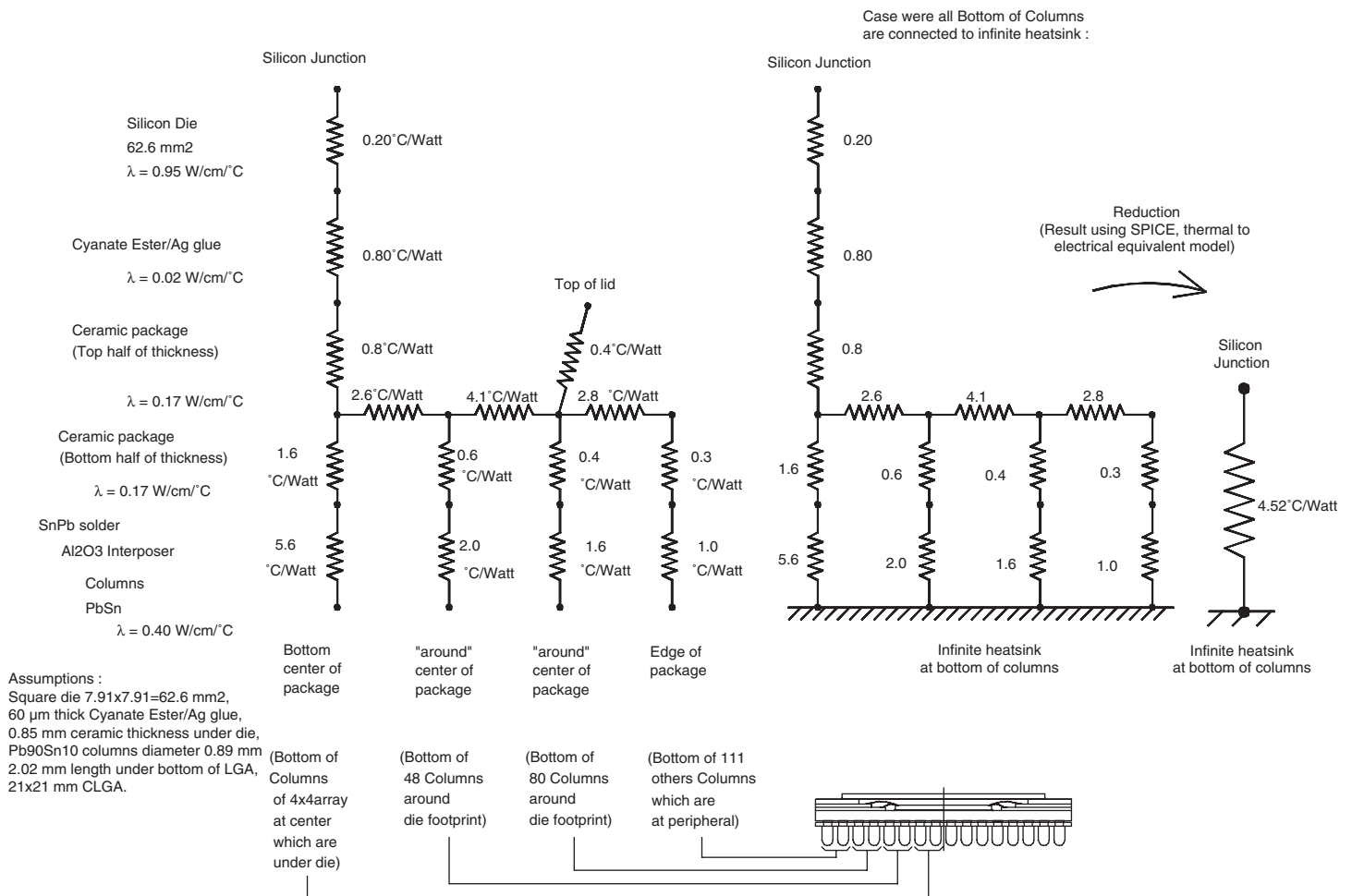
Notes: 1. Typical values, assuming that the power dissipation is uniform over 25% of the die's top surface, are extracted from ANSYS thermal simulation.
2. CI-CGA 255 package is hermetic.

12. Applying the TS86101G2B MUXDAC

12.1 Accessing Power Supplies

The TS86101G2B MUXDAC features three different power supplies (V_{CCD}, V_{EED} and V_{EEA}) as well as two different ground planes (analog ground plane AGND and digital ground plane DGND). We highly recommend that the analog and digital planes be fully separated (both at board level and externally).

Figure 12-1. V_{EEA} Bypassing and Grounding Scheme
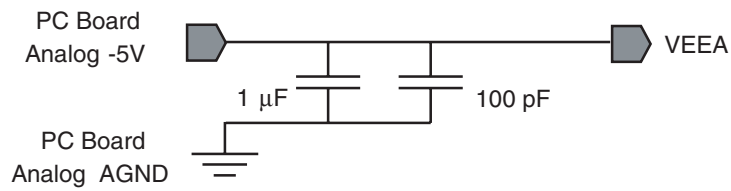
Note: The 1 µF and 100 pF capacitors must be placed as close as possible to the board connectors.

Figure 12-2. V_{EED} and V_{CCD} Bypassing and Grounding Scheme
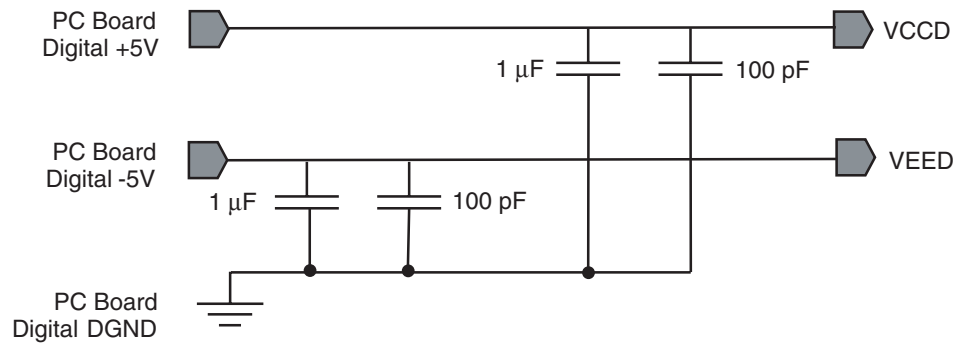
Note: The 1 µF and 100 pF capacitors must be placed as close as possible to the board connectors.

Figure 12-3. Decoupling Scheme of Power Supplies
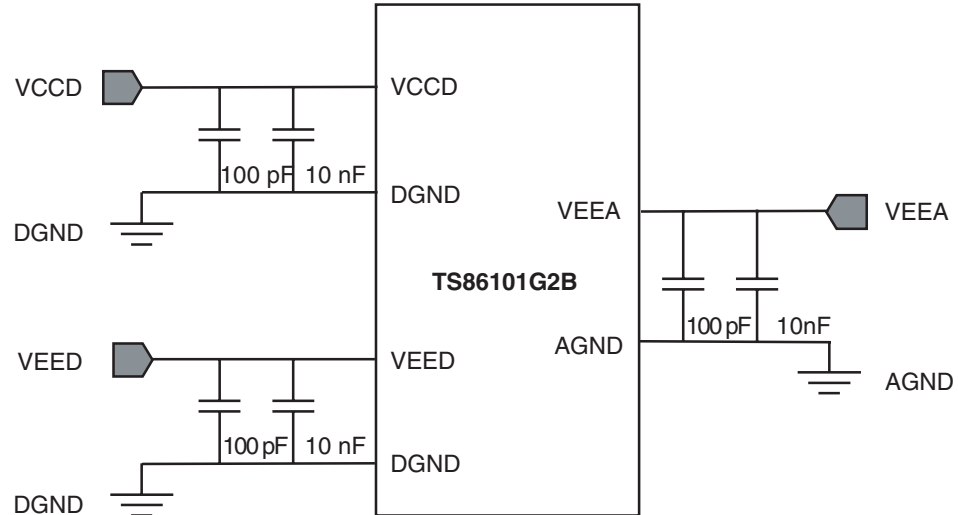
12.2   Digital Inputs and Data Ready Signal Implementation

Figure 12-4.   Differential 3.3V PECL
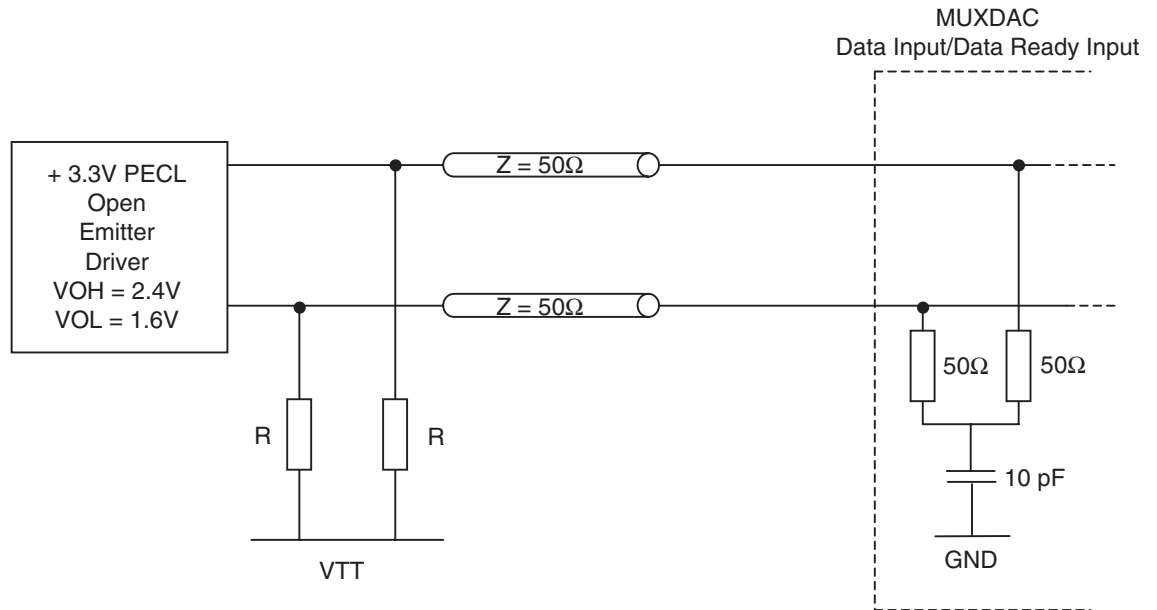
Note: Recommended values for R and VTT:
VTT = GND, R = 120 to 200Ω
VTT = 1V, R = 50Ω
Rule of thumb for determining R and VTT: (VOL-VTT)/R>Swing/100

Figure 12-5.   Differential 2.5V PECL
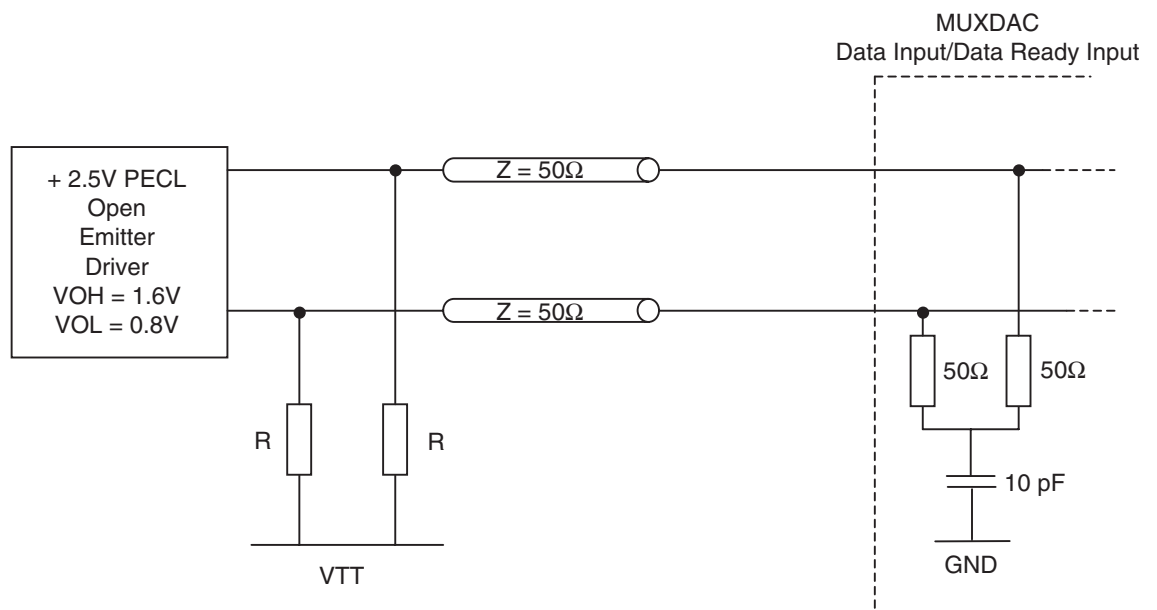
Note: Recommended values for R and VTT:
VTT = GND, R = 50Ω

0992D–BDC–04/09
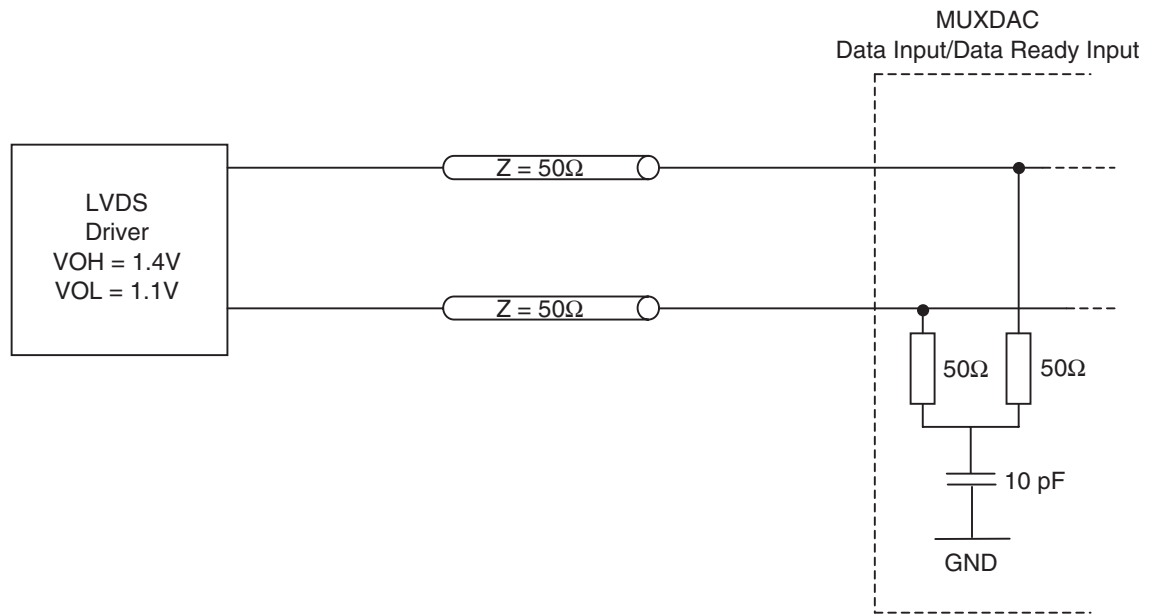
Figure 12-6. LVDS

Figure 12-7. Single-ended Implementation of DATA_IN and Data Ready Inputs
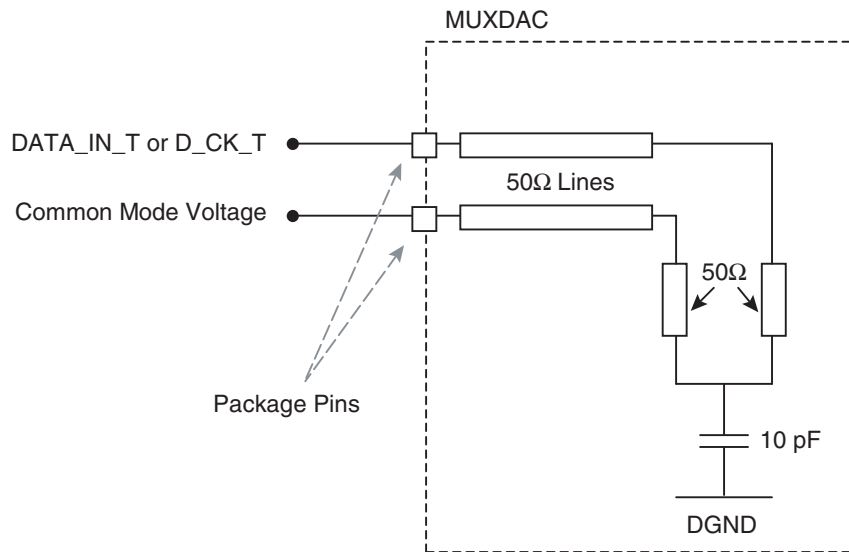
The TS86101G2B MUXDAC digital input and Data Ready input signals provide PECL and LVDS level formats in differential mode. When used in single-ended mode, the associated *false* signal must be tied to the common mode voltage of the *true* signal, as shown in Figure 12-7.

12.3 CW_IN Master Clock Implementation

In order to allow for any ECL/PECL/LVDS differential input levels, the CW_IN master input clock must be AC-coupled through 10 nF capacitors (for information only) as shown in Figure 12-8.

Figure 12-8. CW_IN Master Input Clock Implementation in AC-coupled Differential Mode
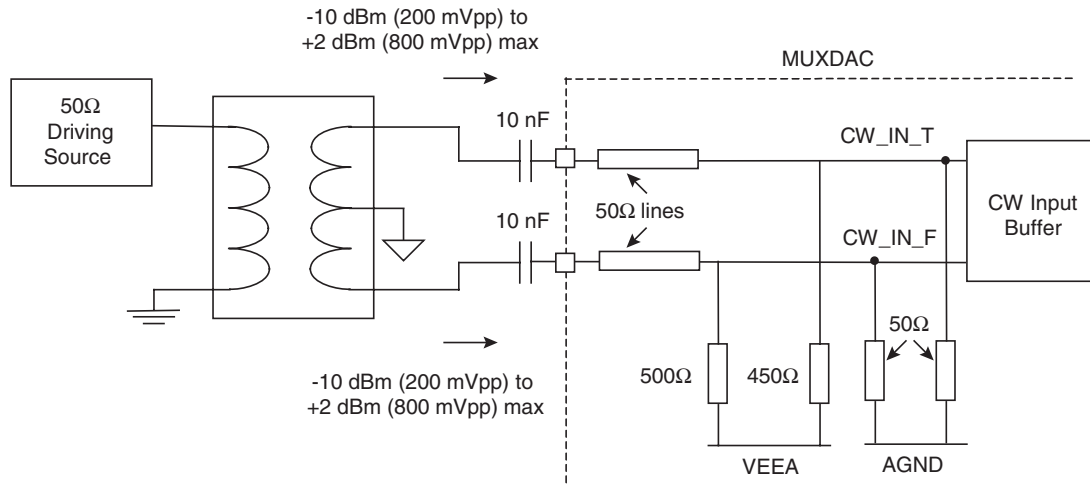
Figure 12-9. CW_IN Master Input Clock Implementation in AC-coupled Singled-ended Mode
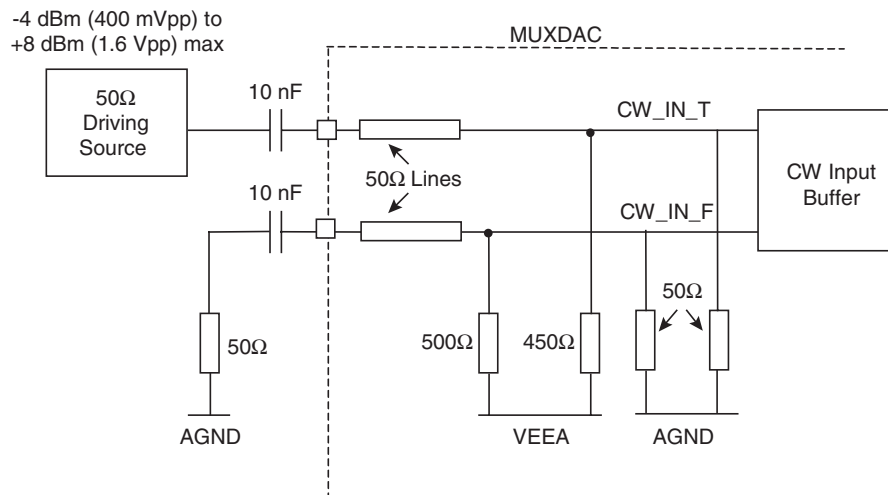
12.4 DSP Output Clock Implementation

In order to make the DSP output clock compatible with standard differential levels such as LVDS and PECL, the signals must be AC-coupled with 10 pF capacitors and used with pull-down resistors to ensure appropriate biasing, as shown in the following three figures.

Three configurations are depicted:

- The load has a high impedance input buffer
- The load has a 100Ω differential buffer
- The DSP_CLK is sent to the load via a driver

Figure 12-10. DSP Output Clock Implementation (General Case – Values Given For Information Only)
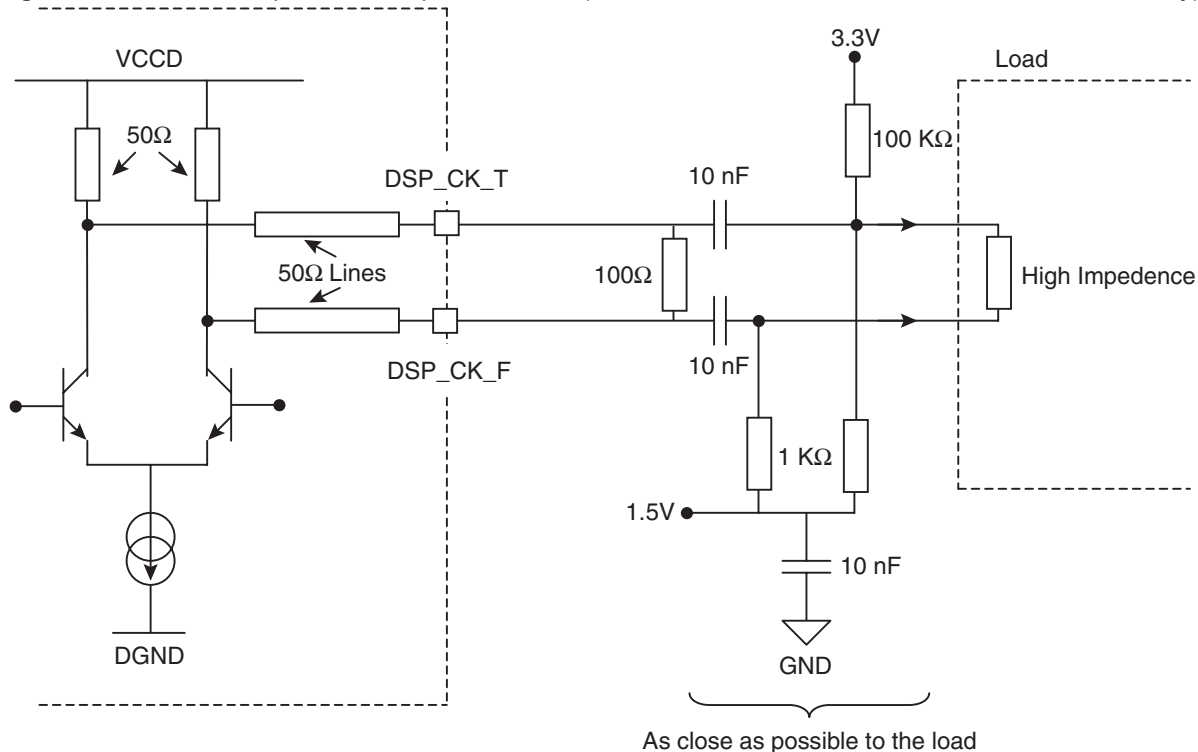
Notes: 1. The 100Ω differential resistor is required for impedance matching of the output buffer of the MUXDAC. It must be placed right after the MUXDAC buffer and not at the end of the line (i.e. close to the load) because of the biasing resistors used after the AC coupling capacitors (it would change the biasing).

2. The 100Ω differential resistor, the AC coupling capacitors and the resistors used for the biasing should all be placed as close as possible to the load.

3. Even without 100Ω differential resistor, the impedance of the output buffer is sufficient. In that case the swing of DSP output clock is twice larger and common mode remains unchanged.

Figure 12-11. DSP Output Clock Implementation (General Case, Values Given for Information Only)
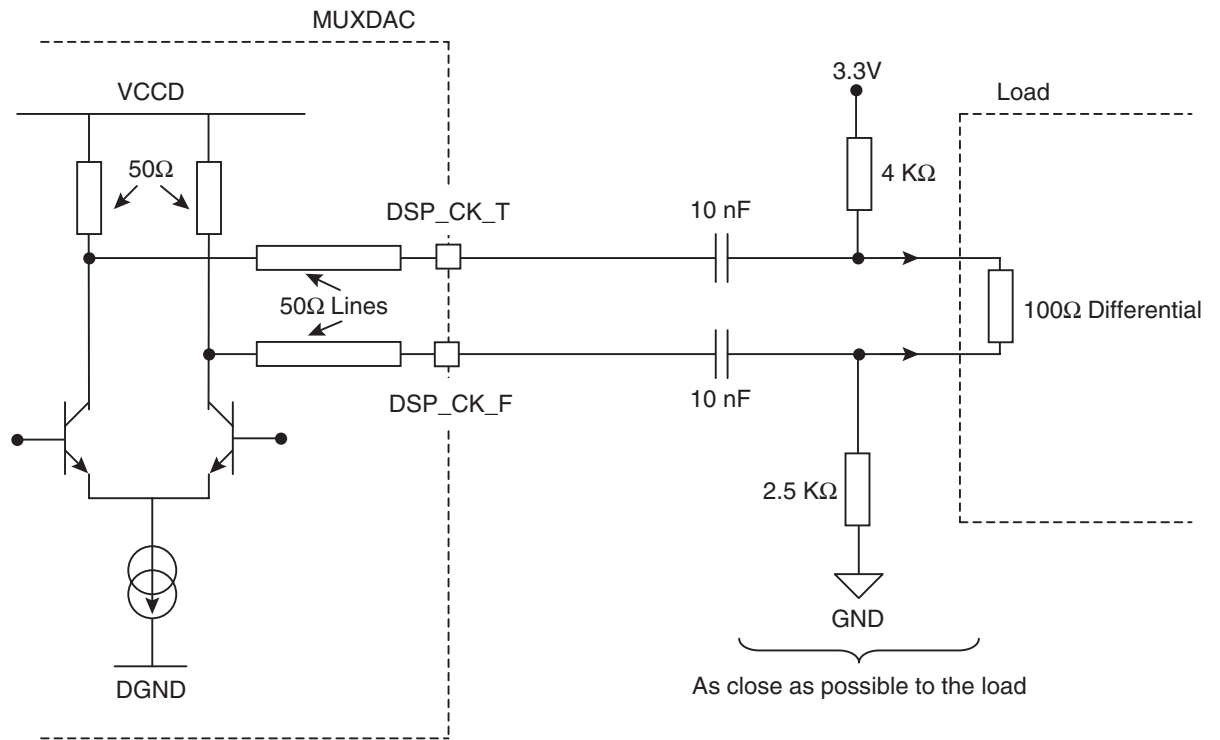
Figure 12-12. DSP Output Clock Implementation (General Case, Values Given for Information Only)
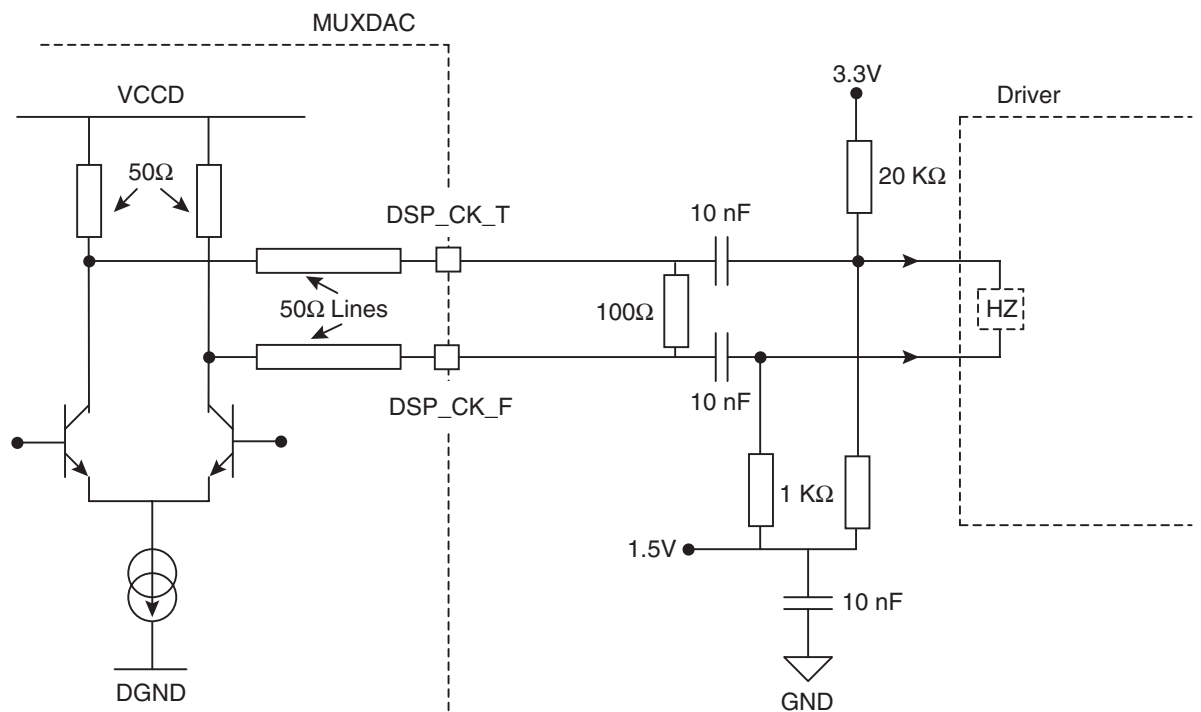
Note: 1. For reference only, MC100EP17 (for a translation to PECL standard level on DSP_CLK) or NBSG16 drivers from On Semiconductor® are well-suited to this application.

2. The 100Ω differential resistor is not mandatory see note .

12.5   Analog Output Termination Scheme

Figure 12-13. Analog Output $2 \times 50\Omega$ Differential Termination Scheme
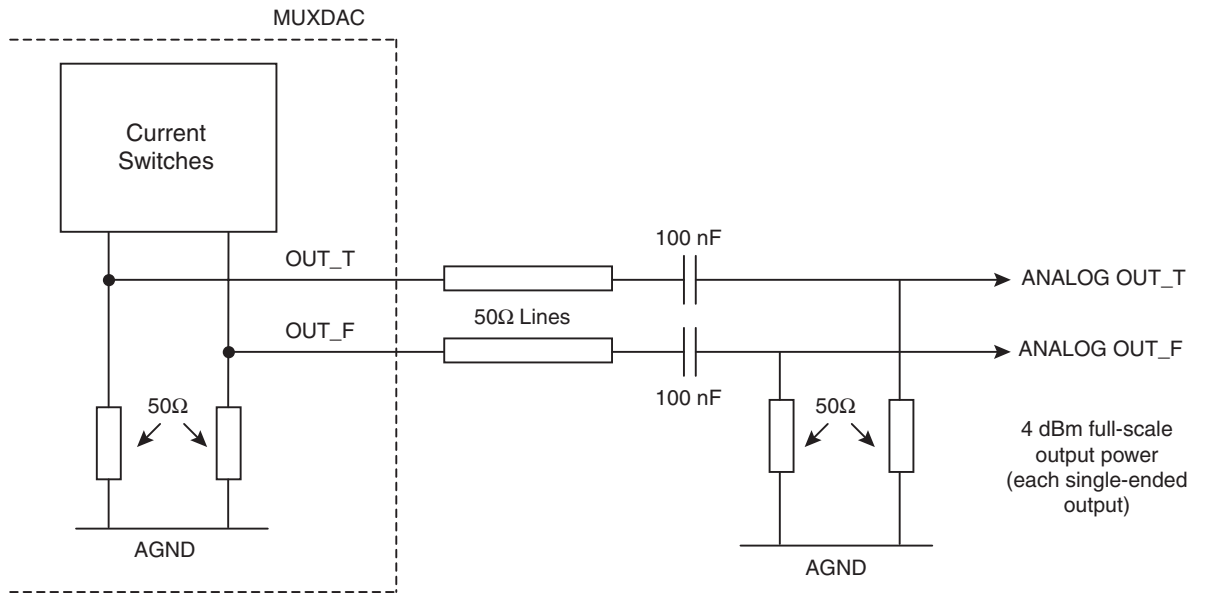
Note: The AC coupling capacitors are necessary to remove the DC component of the signals (–0.6V).

Figure 12-14. 50Ω Single-ended Output through a Differential to Single-ended $1/\sqrt{2}$ Balun
($1/\sqrt{2}$ voltage ratio is necessary for correct 100Ω differential to 50Ω single-ended impedance transformation)
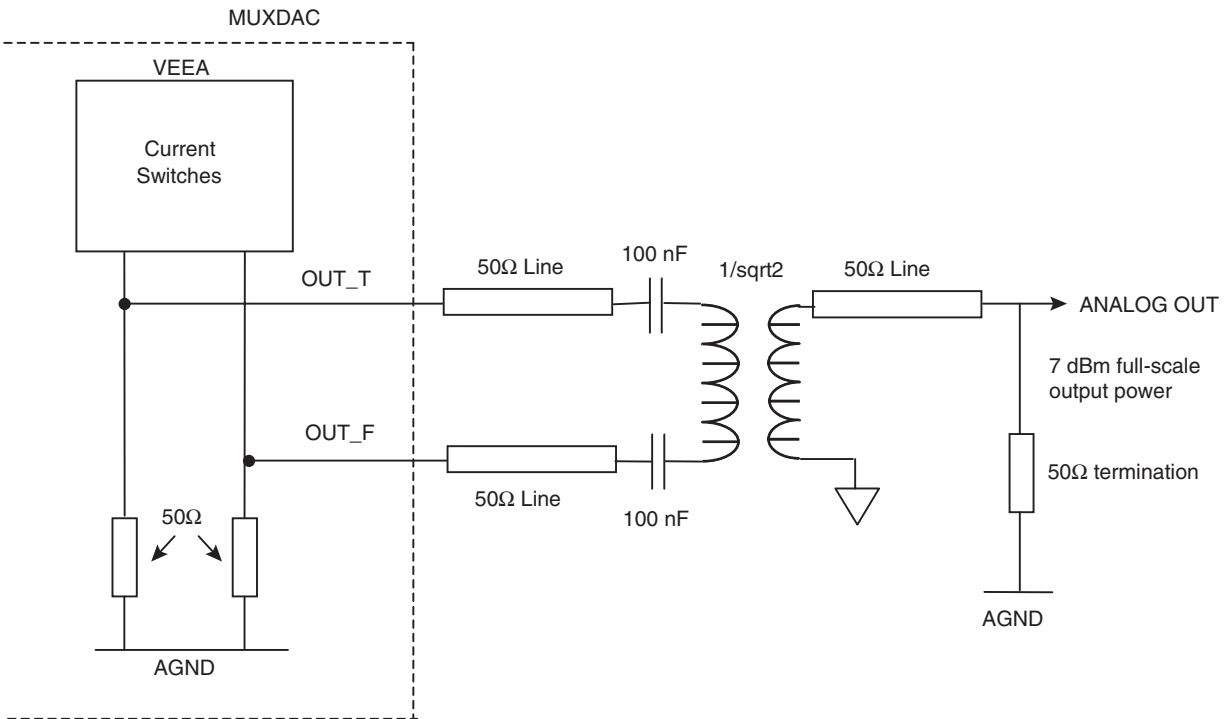
12.6   Interfacing the TS86101G2B MUXDAC with a Digital Signal Processor

Figure 12-15. Interfacing with a Digital Signal Processor
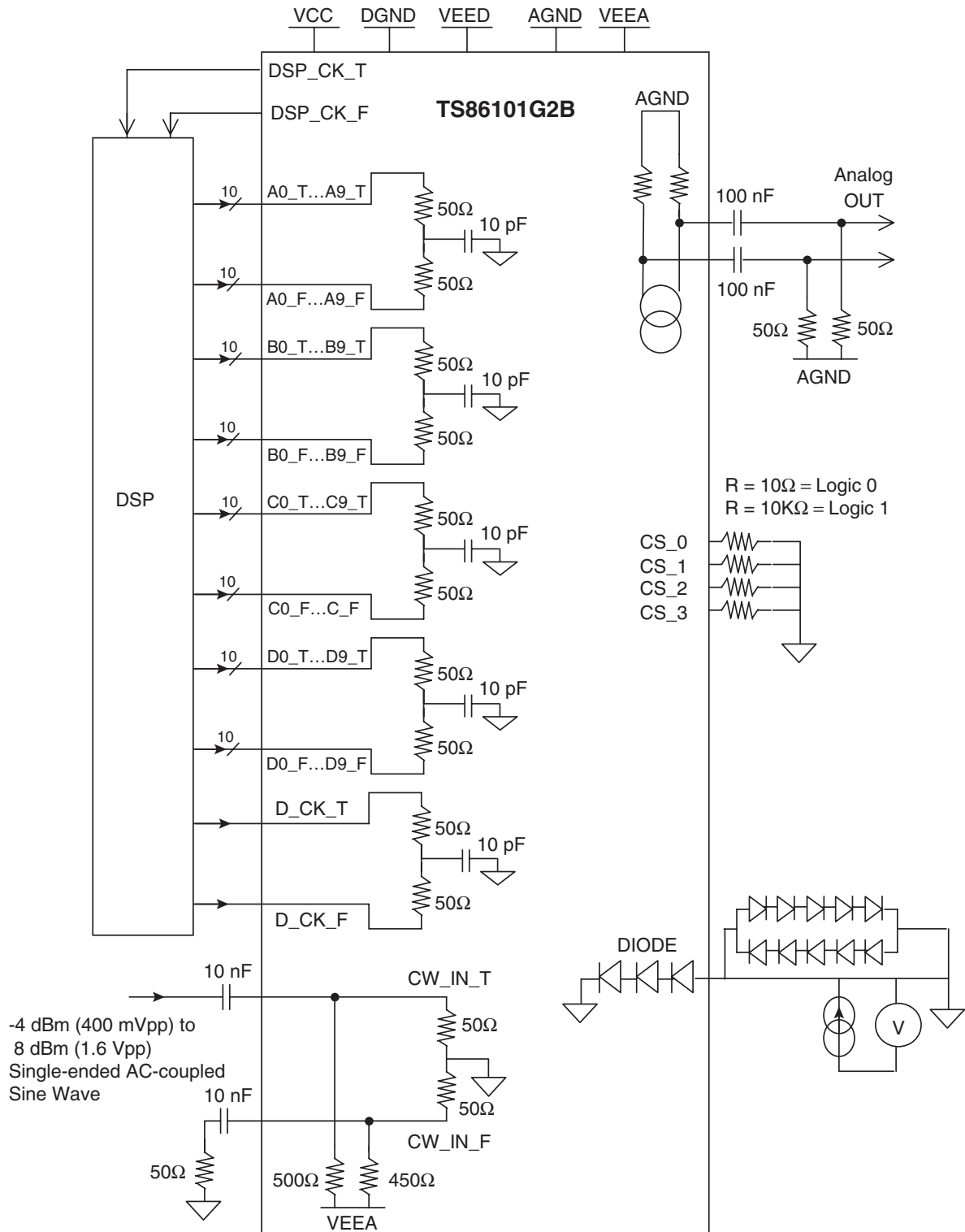
Note: All the data and clock inputs/outputs are connected via 50Ω impedance lines.

13. Mechanical Description of CBGA 255 Package

Figure 13-1. CBGA 255 Package Outline –Top View

No ball on A1 = index corner

Package Chamfer 0.4 (x4)

- A -

- B -

21.00 +/- 0.20 mm

16.64 mm

21.00 +/- 0.20 mm

(1.27)

(1.27)

255 x Ø
D = 0.80 +/- 0.10 mm

⊕ 0.40 T A B (Position of array of balls/edges A and B)
⊕ 0.15 T (Position of balls within array)
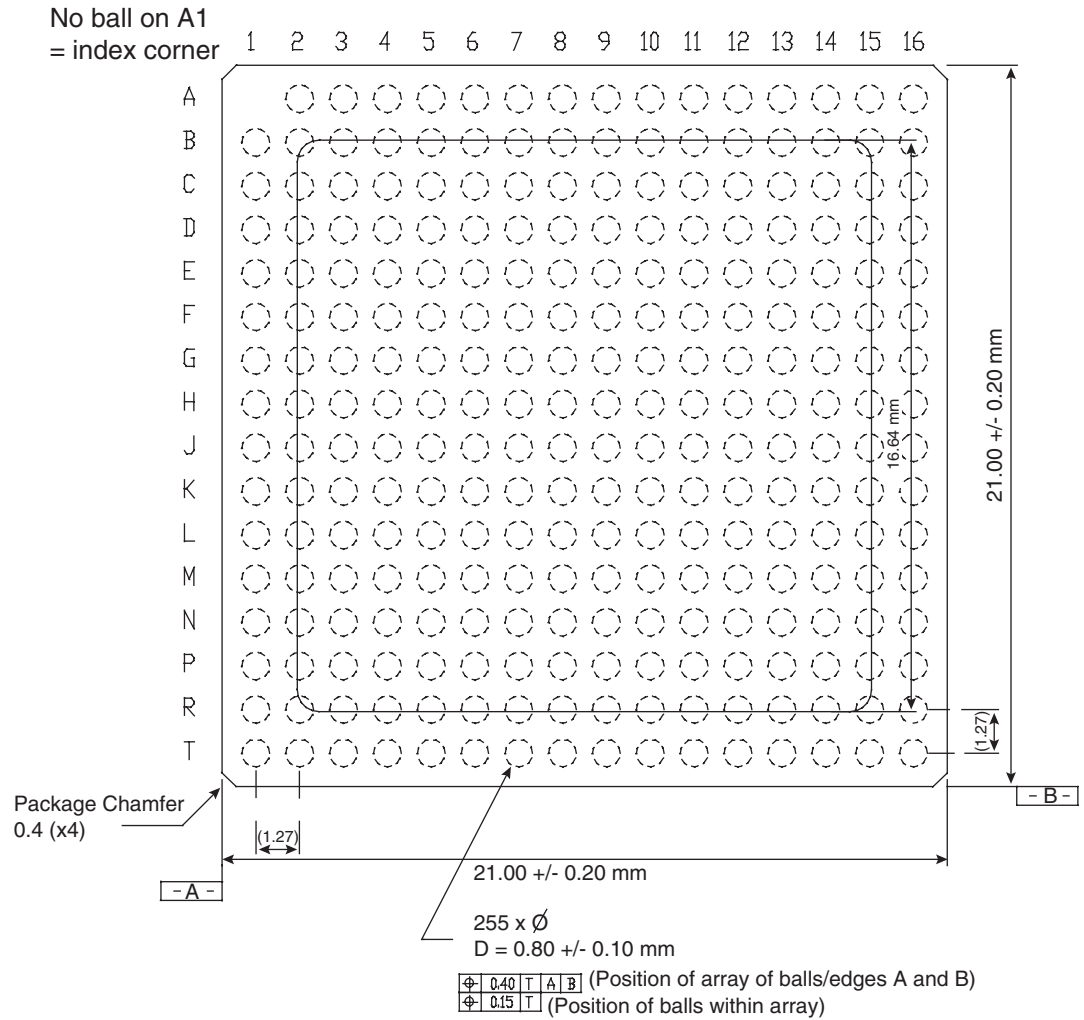
Figure 13-2. CBGA 255 Package Outline – Side View

Balls
Eutectic Solder
Sn63Pb37

Lid 0.38 mm thickness
+ 0.05 solder
16.64 mm² lid
Au finish

0.25 T

– T –

0.15

0.80 mm
+/- 0.10

0.43 mm
+/- 0.05

0.65 +/- 0.10

1.80 mm
+/- 0.15

2.88 mm
+/- 0.29

All units in mm
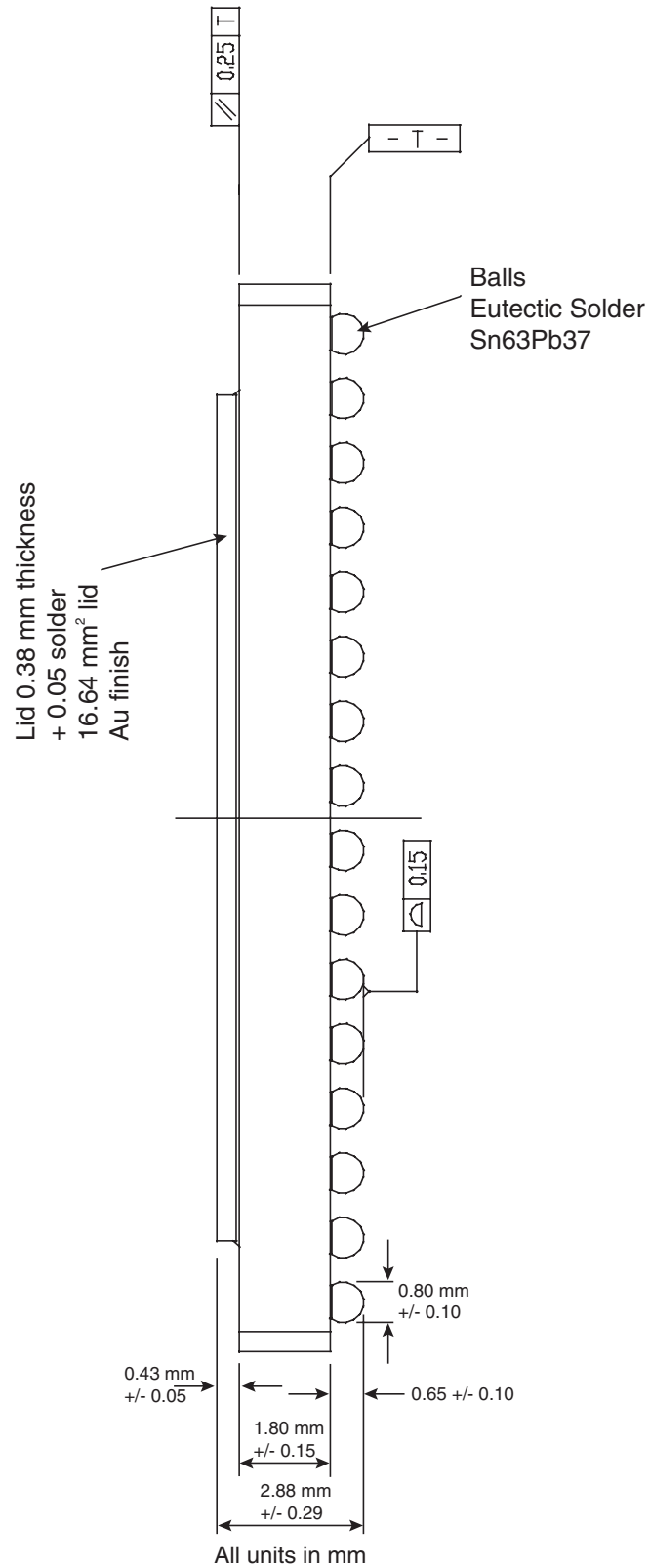
For lead free roadmap, please contact your local e2v sales office.

Figure 13-3. CBGA 255 Package Outline – Cross Section

Metallic lid 0.381 mm thickness
16.64 mm^2 lid
(Kovar, Ni-Au plated)
Grounded
Hermetically soldered to package

0.43 +/- 0.05

2.88 +/- 0.29

1.80 +/- 0.15

0.40
0.20
0.25
0.20
0.50

0.10
0.15

0.65 +/- 0.10

0.80 mm +/- 0.10

Al203 Ceramic Package

Balls
Eutectic Solder
Sn63Pb37
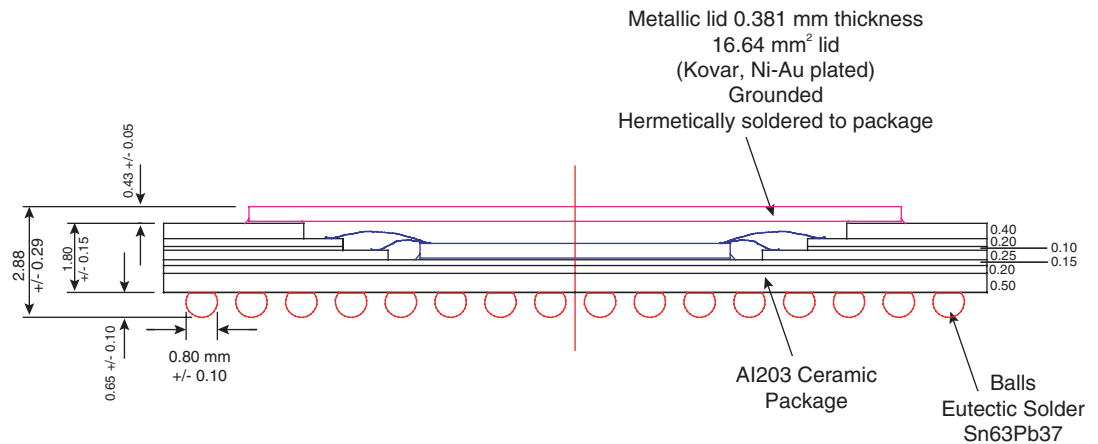
Figure 13-4. CBGA 255 Side View after Reflow

0.55 +/- 0.10

0.85 mm +/- 0.10

Balls
Eutectic Solder
Sn63Pb37
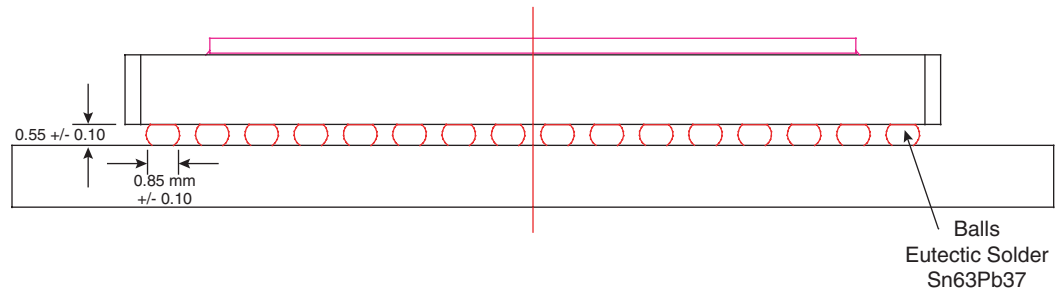
Note: After reflow, the height of the balls decreases from 0.65 to 0.55 mm because of the package weight. The diameter increases from 0.80 to 0.85 mm. This data is for information only and does not constitute part of e2v's specification.

14. Mechanical Description of CI-CGA 255 Package

Figure 14-1. CI-CGA 255 Package Outline - Top View

Top View

No column on A1
= Index corner

SCI Chanfer 15

Package Chanfer
0.4 (x4)
SCI Chanfer 0.4 (x3)

-A-

-B-

21.00 +/- 0.20 mm

21.00 +/- 0.20 mm

(1.27)

(1.27)

255x⌀ D=0.89+/-0.10 mm

⊕ 0.40 T A B (Position of array of columns/edges A and B)
⊕ 0.15 T (Position of columns within array)
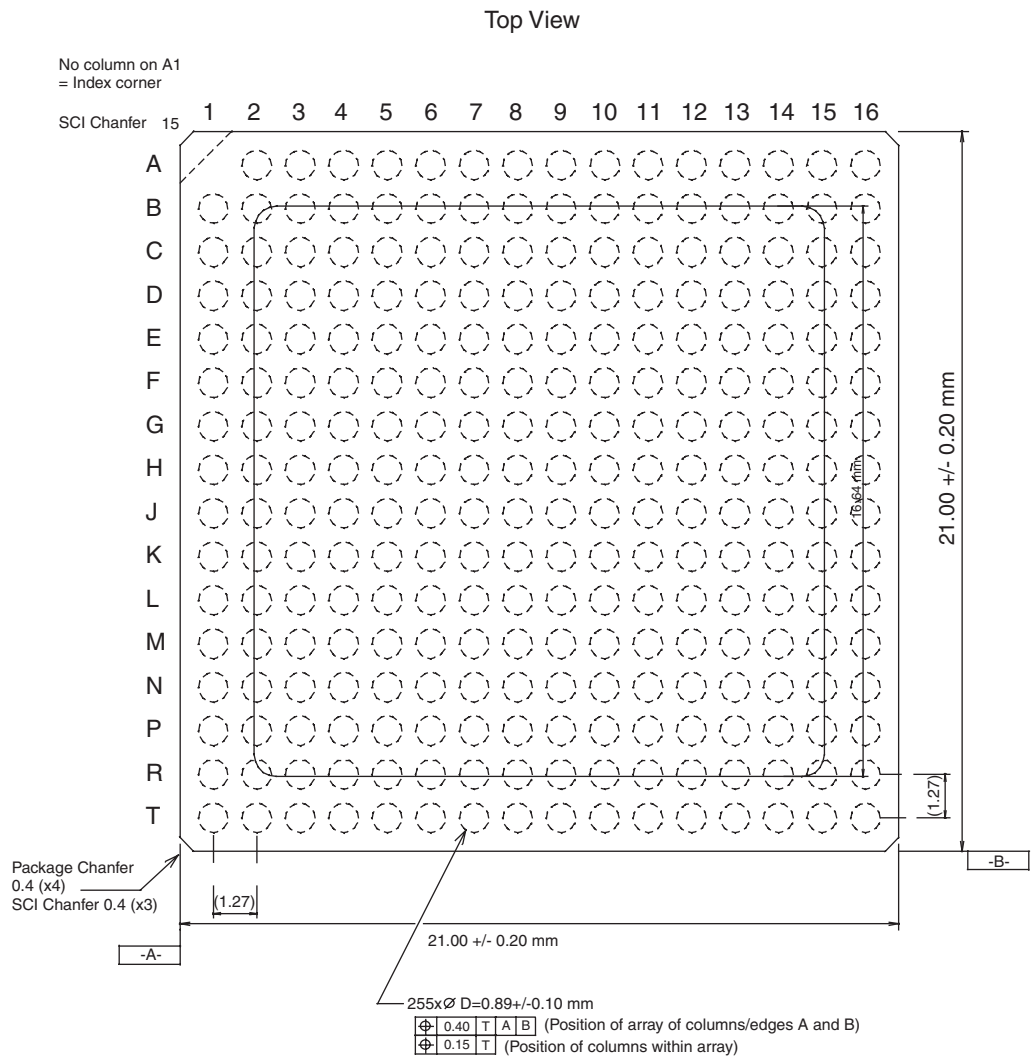
Figure 14-2. CI-CGA 255 Package Outline - Side View

All units in mm
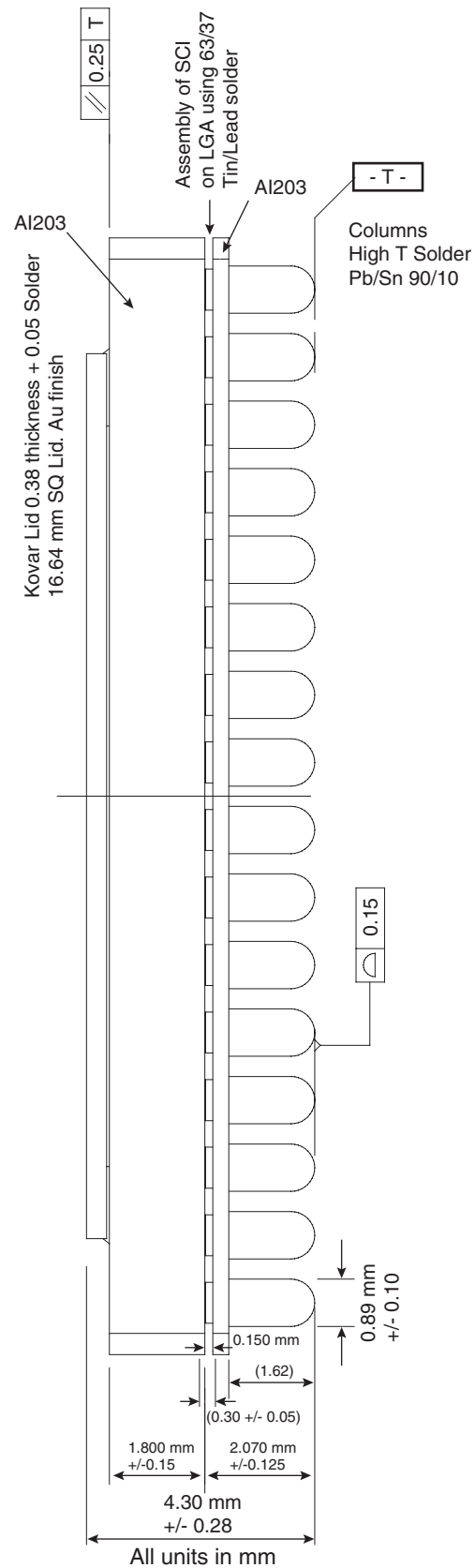
15. TSEV86101G2BGL Evaluation Kit

Figure 15-1. TSEV86101G2BGL Evaluation Board
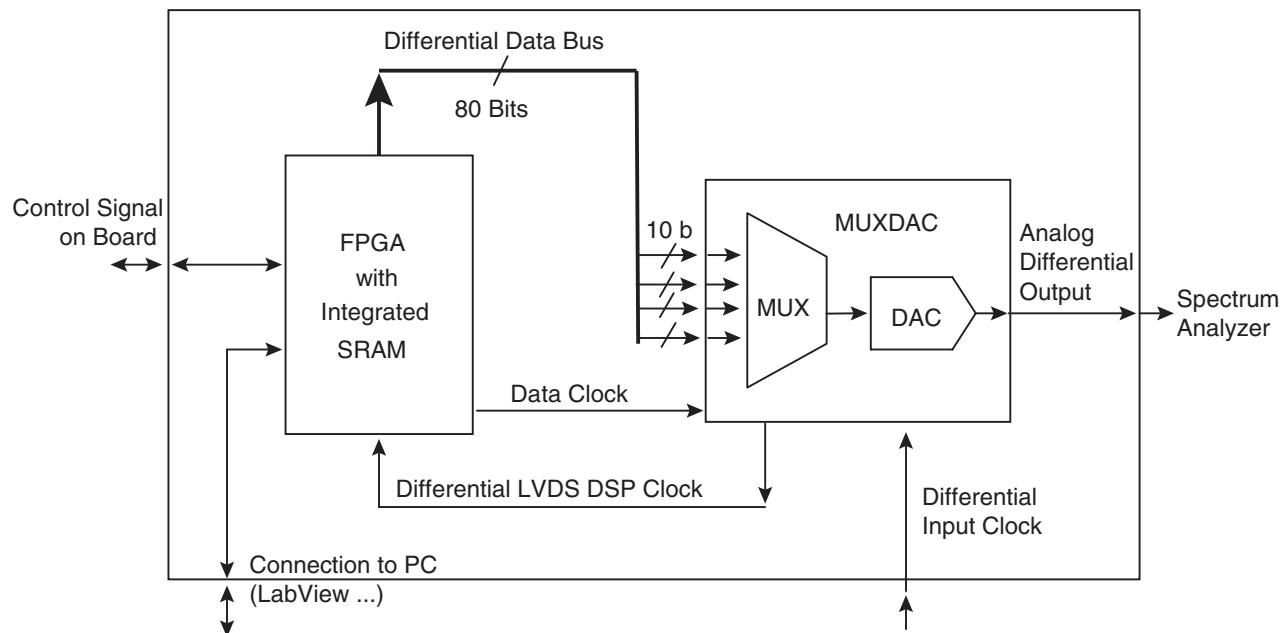
The TSEV86101G2BGL Evaluation Board is the main component of the Evaluation Kit needed to perform characterization of the TS86101G2B MUXDAC for sampling frequencies up to 600 Msps.

The evaluation system of the TS86101G2B MUXDAC device comprises a configurable printed circuit board (the evaluation board itself), including the soldered MUXDAC device (CBGA-255 package), an FPGA chip, a serial interface to a PC and a user interface.

The TSEV86101G2BGL evaluation kit contains all necessary software and hardware for setting up the board and performing its characterization.

16. Test Bench Description

Figure 16-1. Test Bench
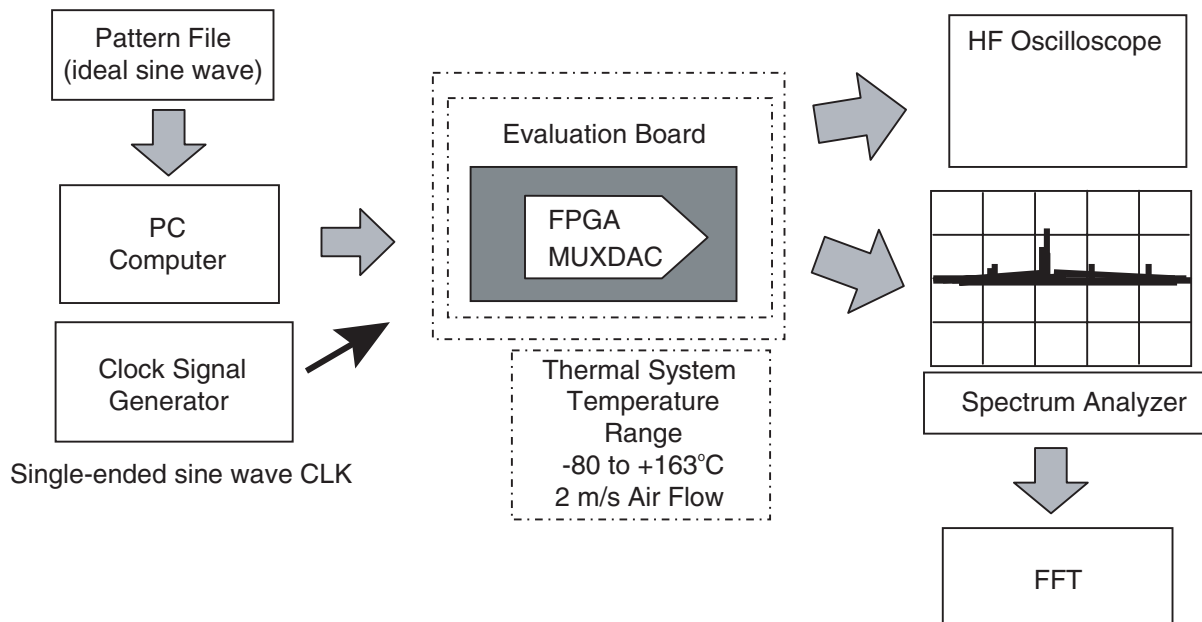
The test bench, implemented to characterize the TS86101G2B MUXDAC using the evaluation kit (TSEV86101G2BGL), can be described as follows:

• A single-ended sine wave clock signal is sent to the board

• A pattern file loaded in a PC is sent to the FPGA via an RS-232 serial interface (the patterns correspond to ideal sinusoids using different frequencies)

• A thermal system above the evaluation board enables testing of the MUXDAC against temperature variations

• An oscilloscope helps define the time domain characteristics of the MUXDAC

• A spectrum analyzer helps locate/identify the MUXDAC's FFTs

17. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
TS86101G2BCGL	CBGA 255	*C* grade $0°C < T_C; T_J < 90°C$	Standard	
TS86101G2BVGL	CBGA 255	*V* grade $−40°C < T_C; T_J < 110°C$	Standard	
TS86101G2BMGS	CI-CGA 255	*M* grade $−55°C < T_C; T_J < 125°C$	Standard	
TSEV86101G2BGL	CBGA 255	Ambient	Prototype	Evaluation board

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18. Appendix

Datasheet Status

Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with the client and application validation	Before design phase
Target specification	This datasheet contains target and goal specifications for product development	Valid during the design phase
Preliminary specification Alpha-site	This datasheet contains preliminary data. Additional data may be published an a later date and could include simulation results	Valid before the characterization phase
Preliminary specification Beta-site	This datasheet also contains characterization results	Valid before the industrialization phase
Product specification	This datasheet contains final product specifications	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability		
Application Information		
Where application information is given, it is advisory and does not form part of the specification		

18.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from improper use or sale.

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