

300mA CMOS LDO

Pb Rohs

Adjustable Voltage with Enable & Power Good

SOT-26

Pin Definition:



- 1. Input
- 2. Ground
- 3. Enable
- 4. Power Good
- 5. Adjustable
- 6. Output

SOT-25



Pin Definition:

- 1. Input
- 2. Ground
- 3. Enable
- 4. Adjustable
- 5. Output

General Description

The TS9004 is a positive voltage linear regulator developed utilizing CMOS technology featured low quiescent current (35uA typ.), low dropout voltage, and high output voltage accuracy, making them ideal for battery applications. The Chip Enable (CE) includes a CMOS or TTL compatible input allows the output to be turned off to prolong battery life. The TS9004 is included a precision voltage reference, current fold-back, error correction circuit, a current limited output driver, over temperature shutdown, and a "Power Good" detector, which pulls low when the output is out of regulation.

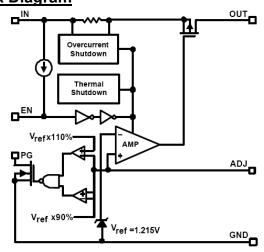
Features

- Very Low Dropout
- Low power consumption: 35uA(typ.)
- Output voltage ±2%
- Internal current limit and thermal shutdown
- Short circuit current fold-back
- Power saving shutdown mode
- Power good output function
- Adjustable output voltage

Applications

- Palmtops
- Video recorders
- Battery powered equipment
- PC peripherals
- High-efficiency linear power supplies
- Digital Signal Camera

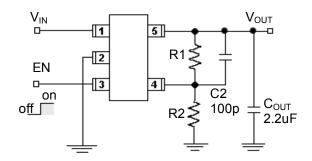
Block Diagram

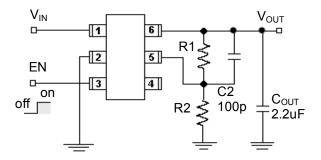


Ordering Information

Part No.	Package	Packing		
TS9004CX5 RF	SOT-25	3Kpcs / 7" Reel		
TS9004CX6 RF	SOT-26	3Kpcs / 7" Reel		

Typical Application Circuit





V_{OUT} = 1.215 (R1+R2)/R2 C2 is unnecessary when R1 or R2 < 20K PG pin is only available in the SOT-26 package Connected to output for Power Good or left floating



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Absolute Maximum Rating

Parameter	Symbol	Limit	Unit
Input Supply Voltage	V _{IN}	+8	V
Enable Input Voltage	V _{CE}	Gnd-0.3 ~ V _{IN} +0.3	V
Output Current	Io	$P_D / (V_{IN} - V_{OUT})$	mA
Power Dissipation	P_{D}	Internal Limited	
Thermal Resistance	Θ_{JA}	140	°C/W
Operating Ambient Temperature Range	T _A	-40 ~ +85	°C
Operating Junction Temperature Range	T _J	-40 ~ +125	°C
Storage Temperature Range	T _{STG}	-65 ~ +150	°C
Lead Soldering Temperature (260°C)		10	S
ESD Classification	HBM	2k	V

Notes: Stress above the listed absolute rating may cause permanent damage to the device.

Electrical Characteristics (Ta = 25°C, unless otherwise noted)

Parameter	Symbol	Test Condition			Min	Тур	Max	Units
Input Voltage	V _{IN}	(Note 1)					7	V
Output Voltage Accuracy	Vo	I _O =1mA			-2		+2	%
		1 000 1	1.5V<	V _{O(NOM} ≤2.0V			1300	
Dropout Voltage	V_{DROP}	$I_{O} = 300 \text{mA}$ $V_{O} = V_{O(NOM)} - 2.0\%$	2.0V< V _{O(NOM} ≤2.8V			See chart	400	mV
			2.8V<	V _{O(NOM} <3.8V		Chart	300	
Output Current	Ιο	V _O >1.2V			300		1	mA
Current Limit	I _{LIM}	V _O >1.2V			300	450		mA
Short Circuit Current	I _{SC}	V _O <0.8V (Note 2)				150	300	mA
Ground Pin Current	I _{GND}	$I_O = 1 \text{mA to } 300 \text{mA}$				35		mA
Line Regulation	DEC	I _O =5mA		V _O < 2.0V			0.15	%
Line Regulation	REG _{LINE}	$V_{IN} = V_O + 1 \text{ to } V_O + 2$ $V_O \ge 2.0 \text{ V}$			0.02	0.1	%	
Load Regulation	REG _{LOAD}	I _O =1mA to 300mA			0.2	1	%	
Over Temperature Shutdown	OTS				150		°C	
Over Temperature Hysterisis	ОТН					30		°C
VO Temperature Coefficient	T _C				30		ppm/°C	
	PSRR			f=100Hz		60		
Power Supply Rejection				f=1kHz		50	1	dB
				f=10kHz	-	20	1	
Output Voltage Noise	eN	f=10Hz to 100kHz I _O =10mA,CBYP=0mF			30		mVrms	
ADJ Input Bias Current	I _{ADJ}	1			1		mA	
ADJ Reference Voltage	V_{REF}			1.2	1.215	1.23	V	
CNI Innest Throughold	V_{EH}	V _{IN} =2.7V to 7V			2.0		V _{IN}	V
EN Input Threshold	V _{EL}	V _{IN} =2.7V to 7V			0		0.4	V



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Electrical Characteristics (Ta = 25°C, unless otherwise noted) (Continue)

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
EN Input Bias Current	I _{EH}	$V_{EN} = V_{IN}$, $V_{IN} = 2.7V$ to $7V$			0.1	mA
EN IIIput bias Current	I _{EL}	V _{EN} =0V, V _{IN} =2.7V to 7V			0.5	mA
Shutdown Supply Current	I _{SD}	V _{IN} =5V, VO=0V V _{EN} < V _{EL}		0.5	1	mA
Shutdown Output Voltage	VO,SD	I _O =35mA, V _{EN} < V _{EL}	0		0.1	V
Output Under Voltage	V_{UV}				85	% V _{O (NOM)}
Output Over Voltage	V_{OV}		115			% V _{O (NOM)}
PG Leakage Current	I _{LC}	V _{PG} =7V			1	mA
PG Voltage Rating	V_{PG}	V _O in regulation			7	V
PG Voltage Low	V_{OL}	I _{SINK} =0.4mA			0.4	V

Note1: V_{IN(MIN)}=V_{OUT}+V_{DROPOUT}

Note2: To prevent the Short Circuit Current protection feature from being prematurely activated, the input voltage must be applied before a current source load is applied.

Detailed Description

The TS9004 family of CMOS regulators contain a PMOS pass transistor, voltage reference, error amplifier, over-current protection, thermal shutdown, and Power Good detection circuitry. The P-channel pass transistor receives data from the error amplifier, over-current shutdown, and thermal protection circuits. During normal operation, the error amplifier compares the output voltage to a precision reference. Over-current and Thermal shutdown circuits become active when the junction temperature exceeds 150 C, or the current exceeds 300mA. During thermal shutdown, the output voltage remains low. Normal operation is restored when the junction temperature drops below 120 C. The TS9004 switches from voltage mode to current mode when the load exceeds the rated output current. This prevents over-stress. The TS9004 also incorporates current foldback to reduce power dissipation when the output is short circuited. This feature becomes active when the output drops below 0.8volts, and reduces the current flow by 65%. Full current is restored when the voltage exceeds 0.8 volts.

External Capacitors

The TS9004 is stable with an output capacitor to ground of 2.2 μ F or greater. Ceramic capacitors have the lowest ESR, and will offer the best AC performance. Conversely, Aluminum Electrolytic capacitors exhibit the highest ESR, resulting in the poorest AC response. Unfortunately, large value ceramic capacitors are comparatively expensive. One option is to parallel a 0.1 μ F ceramic capacitor with a 10 μ F Aluminum Electrolytic. The benefit is low ESR, high capacitance, and low overall cost. A second capacitor is recommended between the input and ground to stabilize ν F. The input capacitor should be at least 0.1 μ F to have a beneficial effect.

All capacitors should be placed in close proximity to the pins. A "Quiet" ground termination is desirable. This can be achieved with a "Star" connection.

Enable

The Enable pin normally floats high. When actively, pulled low, the PMOS pass transistor shuts off, and all internal circuits are powered down. In this state, the quiescent current is less than 1mA. This pin behaves much like an electronic switch.

Power Good

The TS9004 includes the Power Good feature. When the output is not within +10% of the specified voltage, it pulls low. This can occur under the following conditions:

(1) Input Voltage too low. (2) During Over-Temperature. (3) During Over-Current. (4) If output is pulled up. (Note: PG pin is an open-drain output.)



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Electrical Characteristics Curve

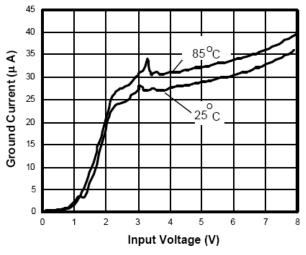


Figure 1. Ground Current vs. Input Voltage

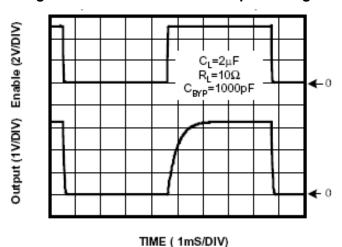


Figure 3. Line Transient Response

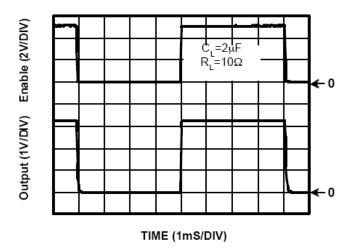


Figure 5. Chip Enable Transient Response

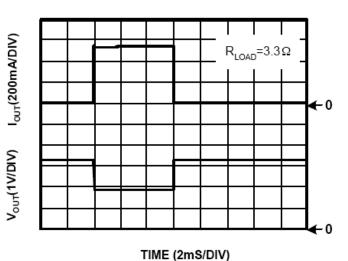


Figure 2. Current Limit Response

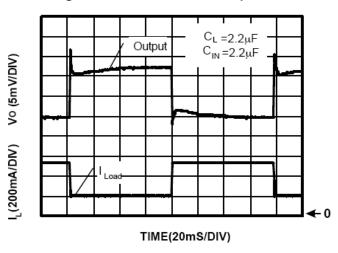


Figure 4. Load Step (1mA~300mA)

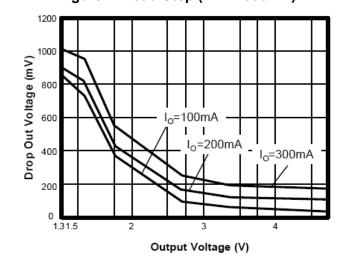


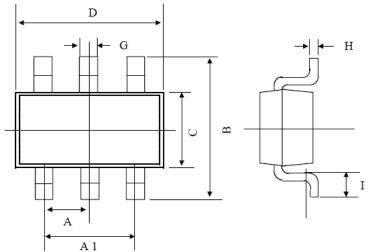
Figure 6. Vdrop vs. Vout



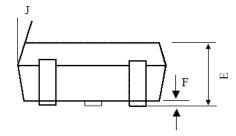
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SOT-26 Mechanical Drawing



	SOT-26 DIMENSION							
DIM	MIL	LIMETE	RS	INCHES				
DIM	MIN	TYP	MAX	MIN	TYP	MAX		
Α	(0.95 BSC		0.0374 BSC				
A1		1.9 BSC		0	.0748 BS	748 BSC		
В	2.60	2.80	3.00	0.1024	0.1102	0.1181		
С	1.40	1.50	1.70	0.0551	0.0591	0.0669		
D	2.80	2.90	3.10	0.1101	0.1142	0.1220		
Е	1.00	1.10	1.20	0.0394	0.0433	0.0472		
F	0.00		0.10	0.00		0.0039		
G	0.35	0.40	0.50	0.0138	0.0157	0.0197		
Н	0.10	0.15	0.20	0.0039	0.0059	0.0079		
Ī	0.30		0.60	0.0118		0.0236		
J	5°		10°	5°		10°		



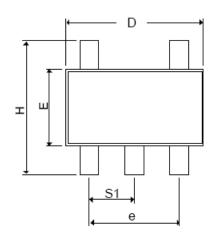


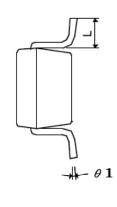
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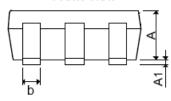
SOT-25 Mechanical Drawing





SOT-25 DIMENSION						
DIM	MILLIM	ETERS	INCHES			
DIIVI	MIN	MAX	MIN	MAX.		
A+A1	0.09	1.25	0.0354	0.0492		
В	0.30	0.50	0.0118	0.0197		
С	0.09	0.25	0.0035	0.0098		
D	2.70	3.10	0.1063	0.1220		
E	1.40	1.80	0.0551	0.0709		
E	1.90 BSC		0.0748 BSC			
Н	2.40	3.00	0.09449	0.1181		
L	0.35 BSC		0.0138 BSC			
θ1	0°	10°	0°	10°		
S1	0.95	BSC	0.0374	4 BSC		

Front View





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