



TSB4N60M / TSI4N60M

600V N-Channel MOSFET

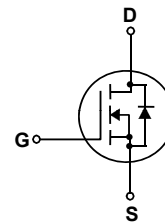
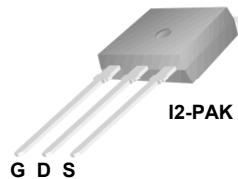
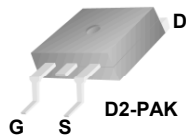
General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 4.0A, 600V, $R_{DS(on)} = 2.6\Omega @ V_{GS} = 10V$
- Low gate charge (typical 16nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	TSB4N60M	TSI4N60M	Units
V _{DSS}	Drain-Source Voltage	600		V
I _D	Drain Current - Continuous (T _C = 25°C) - Continuous (T _C = 100°C)	4.0	4.0*	A
		2.4	2.4 *	A
I _{DM}	Drain Current - Pulsed (Note 1)	16	16 *	A
V _{GSS}	Gate-Source Voltage	± 30		V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	160		mJ
E _{AR}	Repetitive Avalanche Energy (Note 1)	10		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P _D	Power Dissipation (T _C = 25°C) - Derate above 25°C	100	33	W
		0.8	0.26	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150		°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	TSB4N60M	TSI4N60M	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	1.25	3.79	°C/W
R _{θCS}	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W



TSB4N60M / TSI4N60M

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.6	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.0\text{ A}$	--	2.0	2.6	Ω
Y_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 2.0\text{ A}$	-	4.5	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	560	--	pF
C_{oss}	Output Capacitance		--	55	--	pF
C_{rss}	Reverse Transfer Capacitance		--	7	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 4.0\text{ A},$ $R_G = 25\ \Omega$	--	10	--	ns	
t_r	Turn-On Rise Time		--	40	--	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	40	--	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	--	50	--	ns
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 4.0\text{ A},$ $V_{GS} = 10\text{ V}$	--	16	-	nC	
Q_{gs}	Gate-Source Charge		(Note 4, 5)	--	2.5	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4, 5)	--	6.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	4.0	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	16	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 4.0\text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 4.0\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$	--	280	--	ns
Q_{rr}	Reverse Recovery Charge	(Note 4)	--	1.8	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 20\text{ mH}, I_{AS} = 4.0\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 4.0\text{ A}, dI/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature



Typical Characteristics

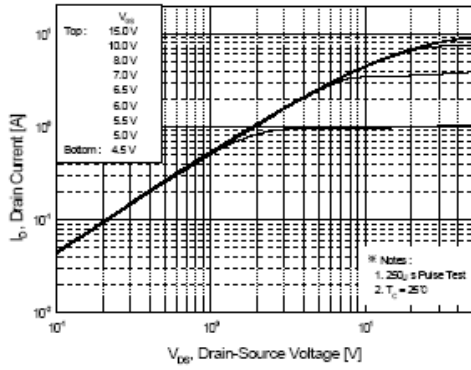


Figure 1. On-Region Characteristics

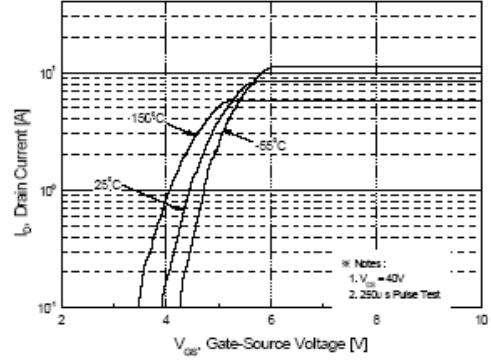


Figure 2. Transfer Characteristics

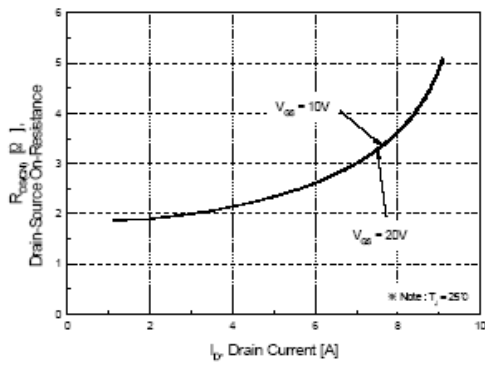


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

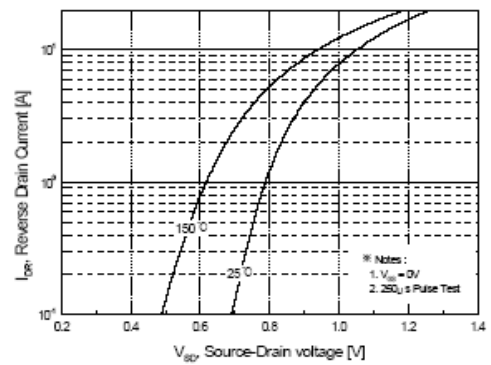


Figure 4. Body Diode Forward Voltage Variation with Source Current

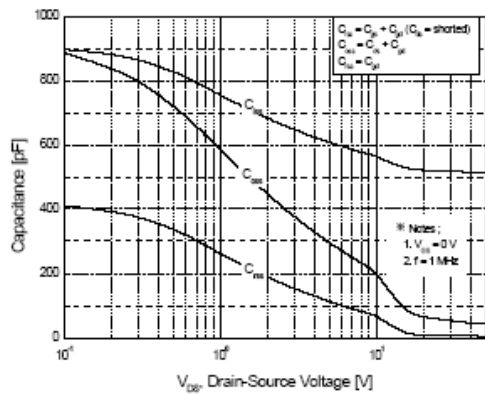


Figure 5. Capacitance Characteristics

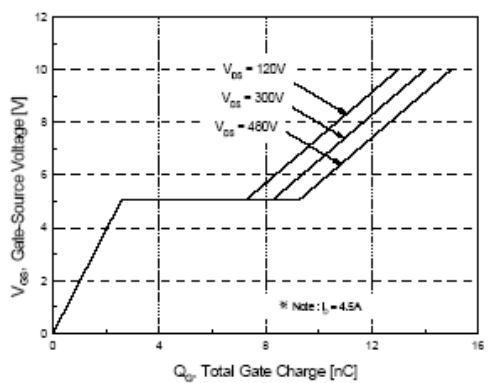


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

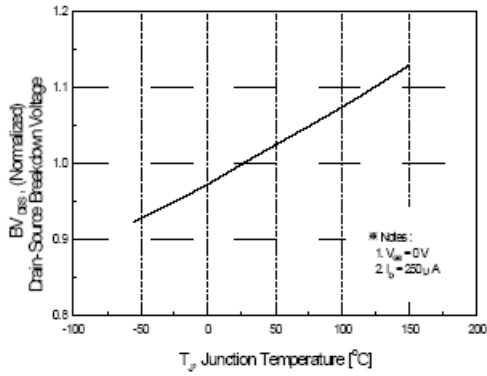


Figure 7. Breakdown Voltage Variation vs Temperature

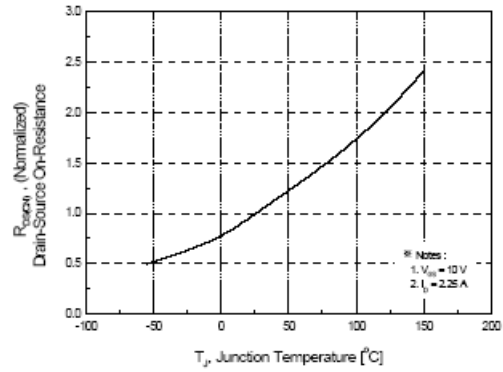


Figure 8. On-Resistance Variation vs Temperature

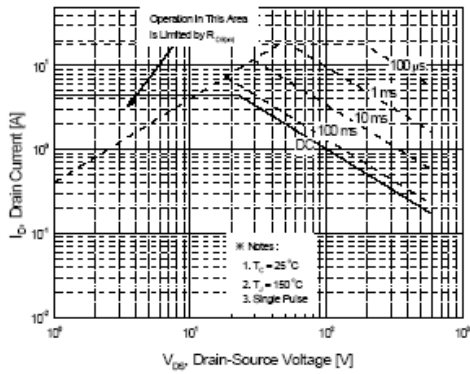


Figure 9-1. Maximum Safe Operating Area for TSB4N60M

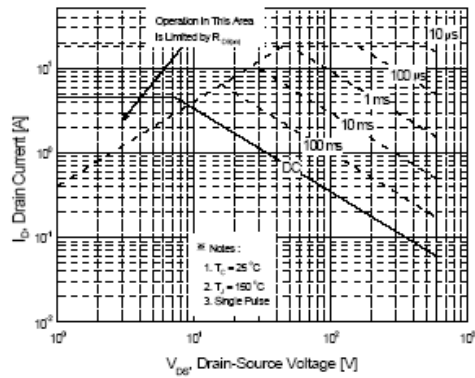


Figure 9-2. Maximum Safe Operating Area for TSI4N60M

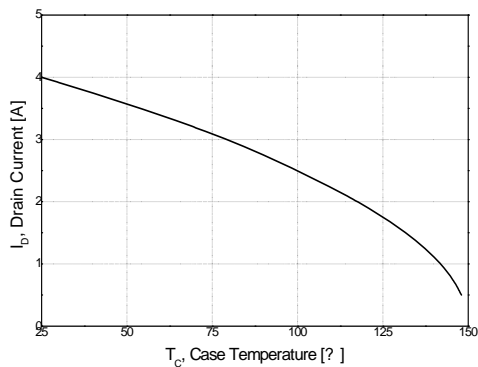


Figure 10. Maximum Drain Current vs Case Temperature



Typical Characteristics (Continued)

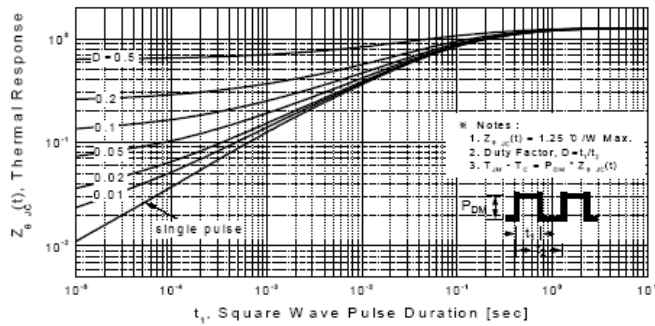


Figure 11-1. Transient Thermal Response Curve for TSB4N60M

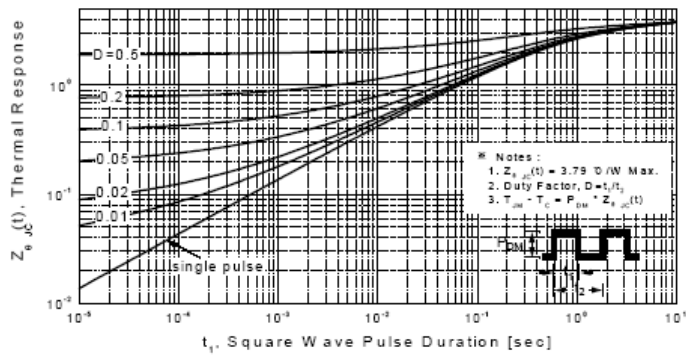
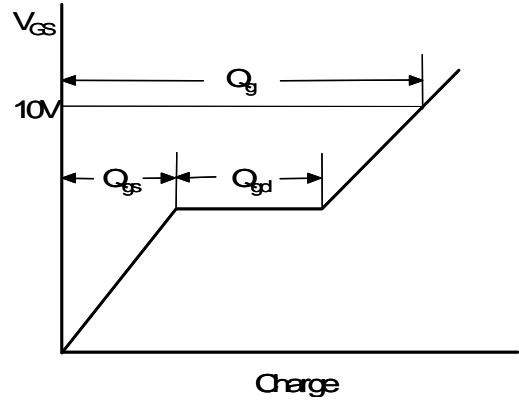
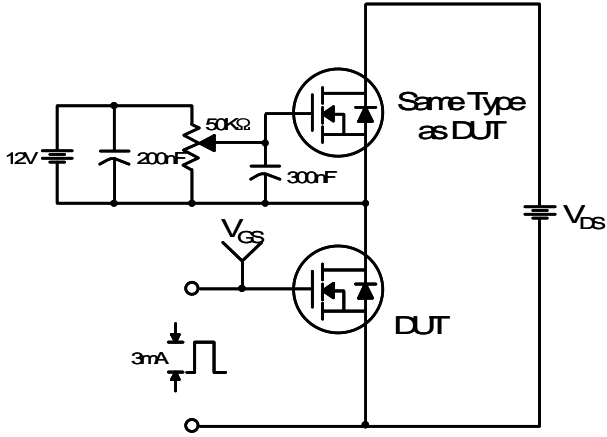


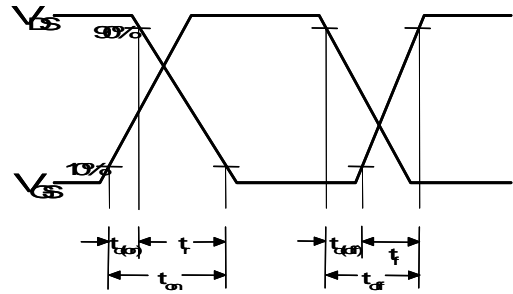
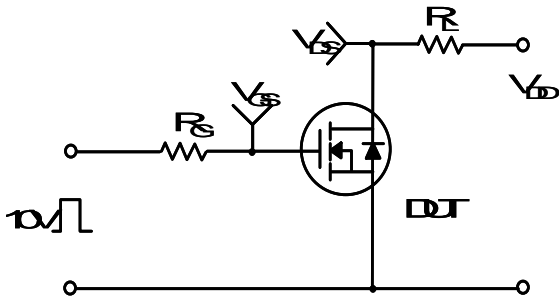
Figure 11-2. Transient Thermal Response Curve for TSI4N60M



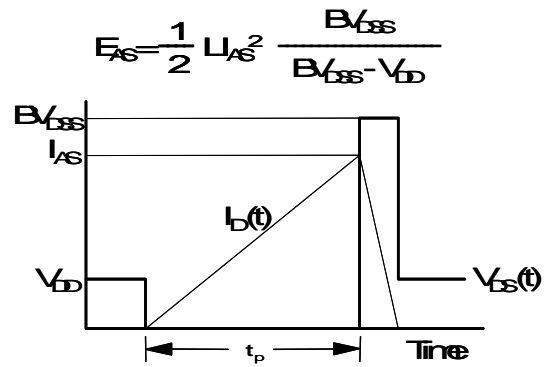
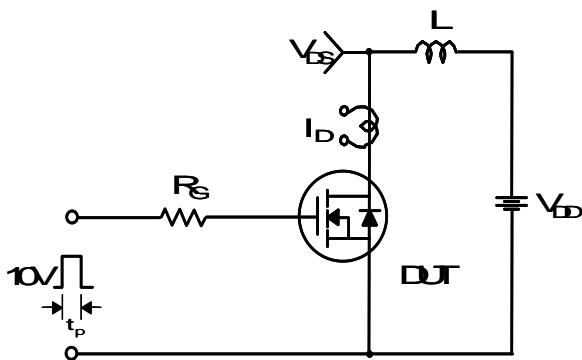
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

