

Very high accuracy (0.5%) high bandwidth (2.1 MHz) bidirectional low-side current sense amplifier



SOT23-6

Features

- Wide supply voltage range: 2.0 V to 5.5 V
- Fixed gain: 20 V/V
- Total output error < 0.5%
- Offset voltage: $\pm 200 \mu\text{V}$ max.
- Gain error: 0.1% max.
- Bandwidth: 2.1 MHz
- Extended temperature range: -40°C to $+125^\circ\text{C}$
- Automotive AEC-Q100 qualified
- Safety capable: documentation available to aid functional safety system design
- Benefits:
 - Total error guaranteed
 - Reduced bill of material

Applications

- High bandwidth low-side current sensing
- Low-side motor control
- Power management in Solar Powered Systems
- Power management in HEV and EV
- Solenoid control

Description

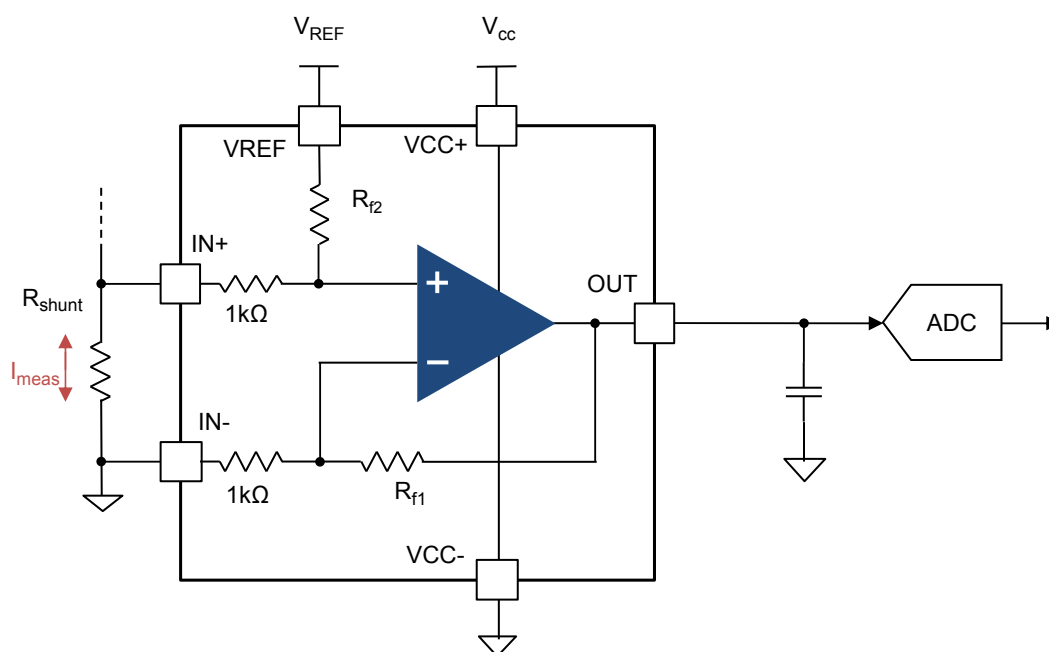
The **TSC1801** is a low-side current measurement amplifier. The **TSC1801** is designed to sense drops across shunt resistors at low common-mode voltages. The gain value is set to 20 V/V, selectable by part number.

Maternity status link

[TSC1801](#)

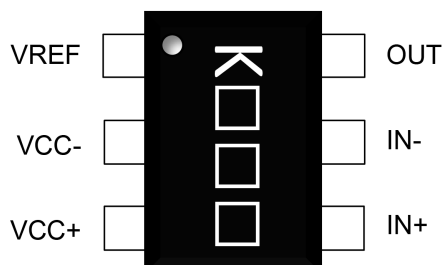
1 Schematic diagram

Figure 1. Internal schematic diagram



2 Pin description

Figure 2. Pin connections (top view)



Dot or letter K denotes pin 1 position

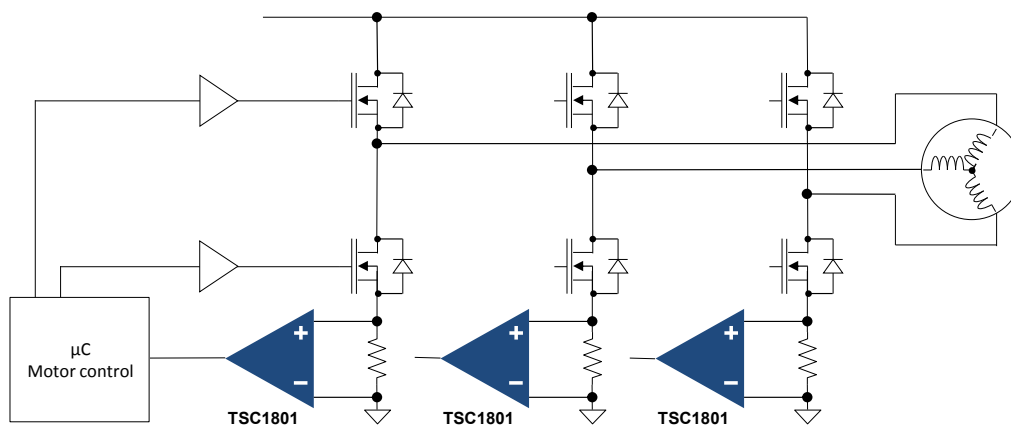
Table 1. Pin description

Pin n°	Pin name	Description
1	VREF	Voltage reference input for zero-current mid-point setting
2	VCC-	Negative supply voltage
3	VCC+	Positive supply voltage
4	IN+	Non-inverting input channel
5	IN-	Inverting input channel
6	OUT	Output channel

3 Typical application schematic

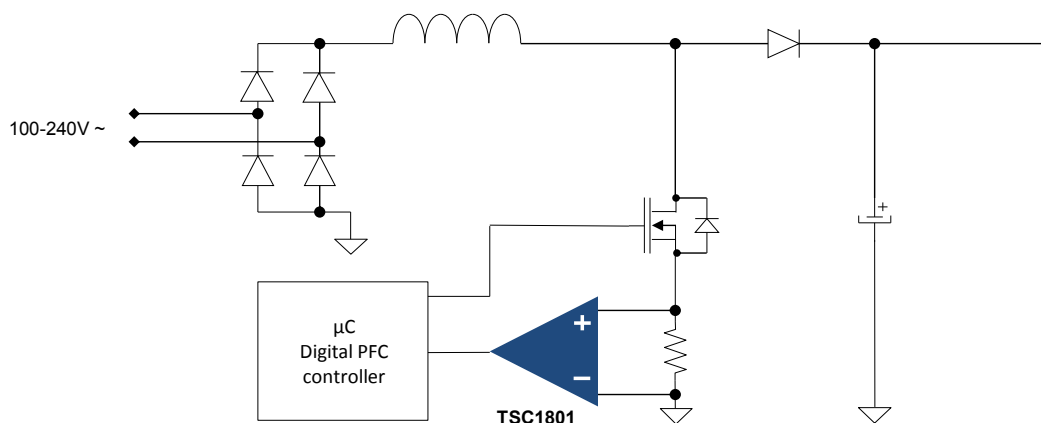
3.1 Motor control

Figure 3. 3-phase motor-control with low-side current measurement by TSC1801



3.2 PFC converter

Figure 4. Power Factor Corrector with low-side current measurement by TSC1801



4 Maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter ⁽¹⁾	Value	Unit
V _{CC}	Supply voltage	6	V
V _{id}	Input voltage differential (V _{IN+} - V _{IN-}) ⁽²⁾	±V _{CC}	V
V _{in}	Input voltage: IN+, IN-, VREF pins ⁽²⁾	(V _{CC-}) - 0.4 to (V _{CC+}) + 0.3	V
I _{in}	Input current	±10	mA
T _{stg}	Storage temperature	-65 to +150	°C
T _j	Maximum junction temperature	150	
R _{th-ja} ⁽³⁾	Thermal resistance junction-to-ambient SOT23-6	240	°C / W
ESD	HBM: human body model (industrial grade) ⁽⁴⁾	4	kV
	HBM: human body model (automotive grade) ⁽⁵⁾	4	kV
	CDM: charged device model ⁽⁶⁾	1.5	kV

1. All voltage values are with respect to the V_{CC}- pin, unless otherwise specified.
2. The maximum input voltage value may be extended to the condition that the input current is limited to ±10 mA.
3. R_{th-ja} is a typical value, obtained with PCB according to JEDEC 2s2p without vias.
4. Human body model: HBM test according to the standard ESDA-JS-001-2017.
5. Human body model: HBM test according to the standard AEC-Q100-002.
6. Charged device model: the CDM test is done according to the standard AEC-Q100-011.

Table 3. Operating conditions

Symbol	Parameter	Value
V _{CC}	Supply voltage	2.0 V to 5.5 V
V _{ref}	VREF pin voltage	V _{CC-} to V _{CC+}
V _{icm}	Common-mode input voltage range	V _{CC-} - 0.1 V to V _{CC+} - 1.5 V
V _{sense}	V _{IN+} - V _{IN-} operating range with total error < 0.3%	
	Gain 20 V/V	± 122 mV
T _{oper}	Operating free air temperature range	-40 °C to +125 °C

5 Electrical characteristics

Table 4. DC electrical characteristics at $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 5\text{ V}$, $V_{ref} = V_{CC}/2$, $V_{IN-} = 0\text{ V}$, $V_{sense} = V_{IN+} - V_{IN-} = 0\text{ V}$, $T = 25\text{ °C}$, $C_L = 47\text{ pF}$ and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Gain	TSC1801B			20		V/V
ΔV_{OUT}	Total output error Gain = 20, $V_{CC} = 5\text{ V}$, $V_{sense} = \pm 100\text{ mV}$ ⁽¹⁾	$T = 25\text{ °C}$			± 0.5	%
		$-40\text{ °C} \leq T \leq 125\text{ °C}$			± 1	
Eg	Gain error	$100\text{ mV} < V_{out} < V_{CC} - 150\text{ mV}$, $T = 25\text{ °C}$			0.1	%
		$100\text{ mV} < V_{out} < V_{CC} - 150\text{ mV}$, $-40\text{ °C} \leq T \leq 125\text{ °C}$			0.15	
V_{io}	Input offset voltage, referred to input	$T = 25\text{ °C}$		± 50	± 200	μV
		$-40\text{ °C} \leq T \leq 125\text{ °C}$			± 700	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift	$-40\text{ °C} \leq T \leq 125\text{ °C}$			± 5	$\mu\text{V}/\text{°C}$
R_{diff}	Differential input resistor			2		k Ω
$\Delta Eg/\Delta T$	Gain error drift				10	ppm/ °C
NLE	Non-linearity error	$100\text{ mV} < V_{out} < V_{CC} - 150\text{ mV}$		± 0.01		%
CMR	Common-mode rejection ratio $20 \cdot \log(\Delta V_{io}/\Delta V_{icm})$	$V_{CC-} \leq V_{icm} \leq V_{CC+} - 1.5\text{ V}$, $T = 25\text{ °C}$	83	100		dB
		$V_{CC-} \leq V_{icm} \leq V_{CC+} - 1.5\text{ V}$, $-40\text{ °C} \leq T \leq 125\text{ °C}$	83	100		
REFR	Reference voltage rejection ratio $20 \cdot \log(\Delta V_{io}/\Delta V_{ref})$	$10\% \cdot V_{CC} \leq V_{ref} \leq 90\% \cdot V_{CC}$, $T = 25\text{ °C}$	85	100		dB
		$10\% \cdot V_{CC} \leq V_{ref} \leq 90\% \cdot V_{CC}$, $-40\text{ °C} \leq T \leq 125\text{ °C}$	85	100		
SVR	Supply-voltage rejection ratio $20 \cdot \log(\Delta V_{io}/\Delta V_{CC})$	$2.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $T = 25\text{ °C}$		109		dB
		$2.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $-40\text{ °C} \leq T \leq 125\text{ °C}$	90	108		
V_{OH}	High-level output voltage drop ($V_{OH} = V_{CC+} - V_{OUT}$)	$V_{sense} = 1\text{ V}$, $T = 25\text{ °C}$			20	mV
		$V_{sense} = 1\text{ V}$, $-40\text{ °C} \leq T \leq 125\text{ °C}$			25	
V_{OL}	Low-level output voltage drop ($V_{OL} = V_{OUT}$)	$V_{sense} = -1\text{ V}$, $T = 25\text{ °C}$			10	mV
		$V_{sense} = -1\text{ V}$, $-40\text{ °C} \leq T \leq 125\text{ °C}$			20	
I_{OUT}	I_{SINK} , $V_{sense} = -1\text{ V}$	Output shorted to V_{CC+} , $T = 25\text{ °C}$	55	70		mA
		Output shorted to V_{CC+} , $-40\text{ °C} \leq T \leq 125\text{ °C}$	40			
	I_{SOURCE} , $V_{sense} = 1\text{ V}$	Output shorted to V_{CC-} , $T = 25\text{ °C}$	50	63		
		Output shorted to V_{CC-} , $-40\text{ °C} \leq T \leq 125\text{ °C}$	40			
C_{Lmax}	Maximum capacitive load Gain = 20	No sustained oscillations		1		nF
$\Delta V_{out}/\Delta I_{out}$	Load regulation	$-10\text{ mA} \leq I_{out} \leq 10\text{ mA}$		0.3	2	mV/mA
Power supply						
I_{CC}	Supply current $V_{IN+} = V_{IN-} = V_{CC}/2$	$T = 25\text{ °C}$		3.3	3.6	mA
		$-40\text{ °C} \leq T \leq 125\text{ °C}$			3.6	

1. Total output error defined by the formula: $\Delta V_{out} = \frac{V_{outmeas} - V_{sense} \cdot \text{Gain} - V_{ref}}{V_{sense} \cdot \text{Gain}}$

Table 5. AC electrical characteristics at $V_{CC} = 3.3\text{ V}$ and $V_{CC} = 5\text{ V}$, $V_{ref} = V_{CC}/2$, $V_{IN-} = 0\text{ V}$, $V_{sense} = V_{IN+} - V_{IN-} = 0\text{ V}$, $T = 25\text{ °C}$, $C_L = 47\text{ pF}$ and $R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
BW	Bandwidth at -3 dB	Gain 20 V/V		2.1		MHz
SR	Slew rate, V_{out} 10% to 90%	V_{out} from 300 mV to $V_{CC} - 300\text{ mV}$		14		V/ μ s
en	Input voltage noise density	$f = 10\text{ Hz}$		170		nV/ $\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		50		
		$f = 10\text{ kHz}$		9		
en p-p	Input noise voltage Gain = 20	$0.1\text{ Hz} \leq f \leq 10\text{ Hz}$		8		μV_{pp}
t_s	Settling time	$V_{sense} = 0$ to 40 mV, $V_{out} \pm 1\%$		300		ns
t_{init}	Initialization time	$V_{sense} = 40\text{ mV}$, $V_{out} \pm 1\%$		25		μ s
EMIRR	EMI rejection ratio $\text{EMIRR} = 20 \log (V_{RF}/\Delta V_{io})$	$V_{RF} = 200\text{ mV}_{peak-peak}$, $f = 400\text{ MHz}$		60		dB
		$V_{RF} = 200\text{ mV}_{peak-peak}$, $f = 900\text{ MHz}$		85		
		$V_{RF} = 200\text{ mV}_{peak-peak}$, $f = 1800\text{ MHz}$		90		
		$V_{RF} = 200\text{ mV}_{peak-peak}$, $f = 2400\text{ MHz}$		90		

6 Typical performance characteristics

$R_L = 10\text{ k}\Omega$ connected to $V_{CC}/2$, unless otherwise specified.

Figure 5. Input offset voltage distribution

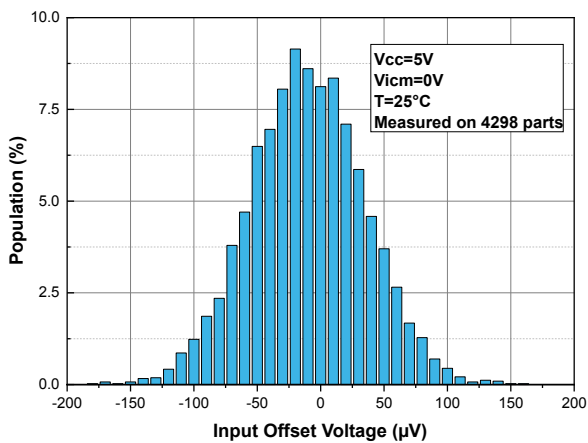


Figure 6. Gain error distribution

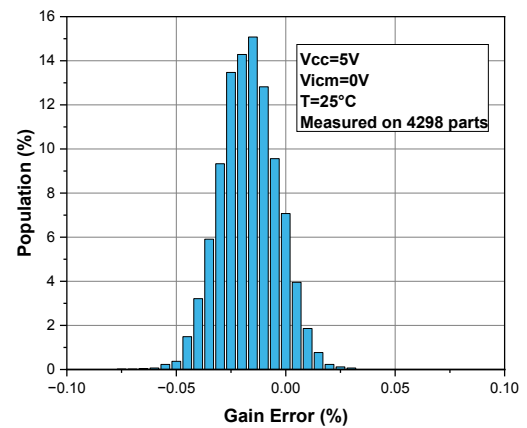


Figure 7. Common-mode rejection ratio distribution

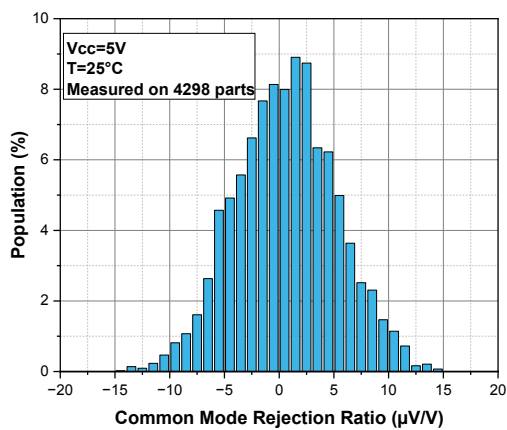


Figure 8. Supply current vs. supply voltage

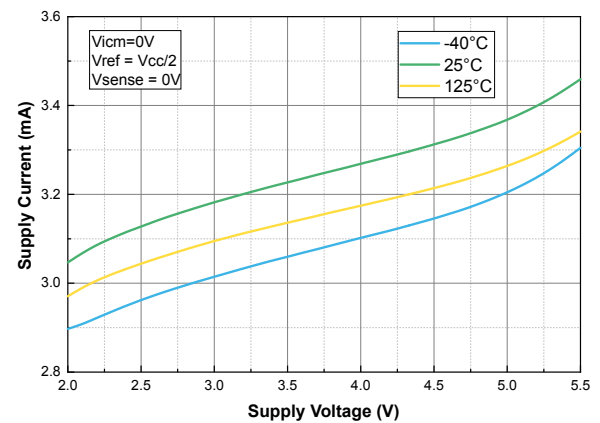


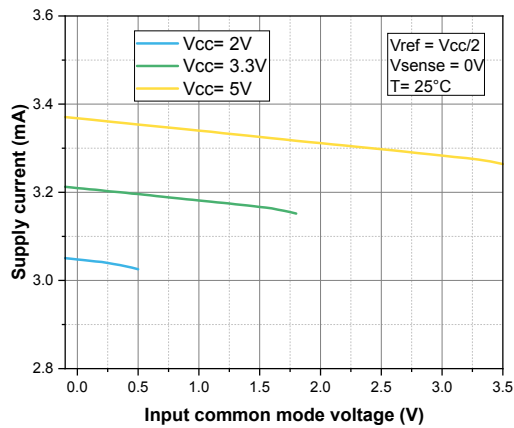
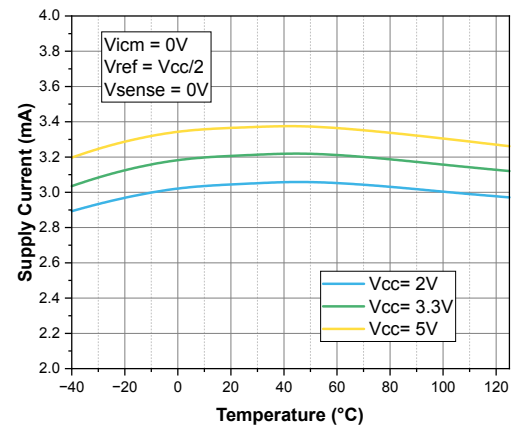
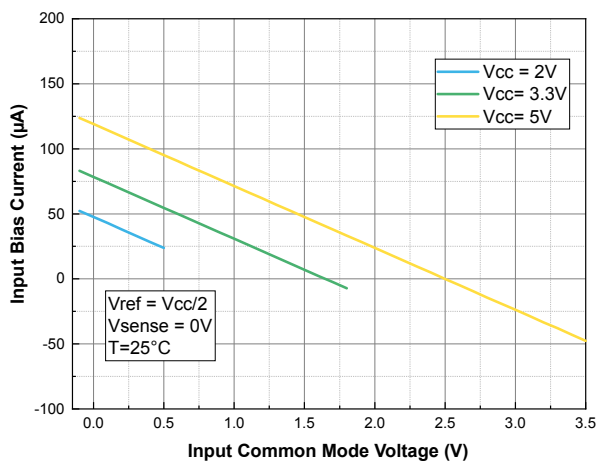
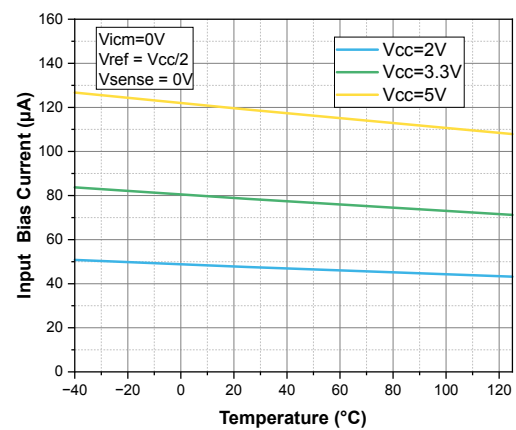
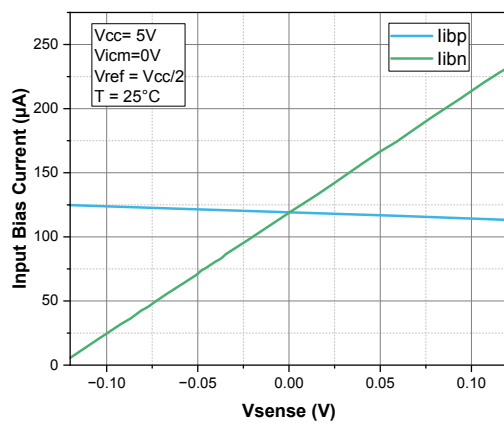
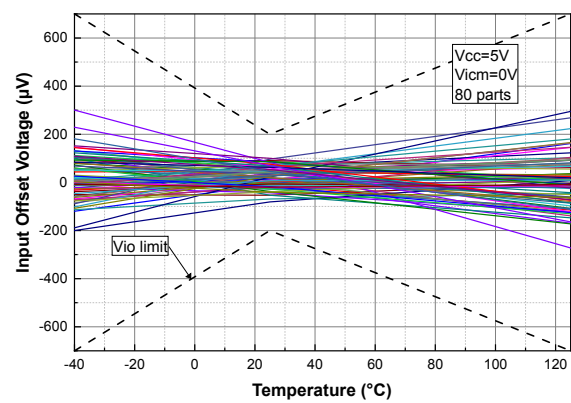
Figure 9. Supply current vs. input common-mode voltage

Figure 10. Supply current vs. temperature

Figure 11. Input bias current vs. input common-mode

Figure 12. Input bias current vs. temperature

Figure 13. Input bias current vs. Vsense

Figure 14. Input offset voltage vs. temperature


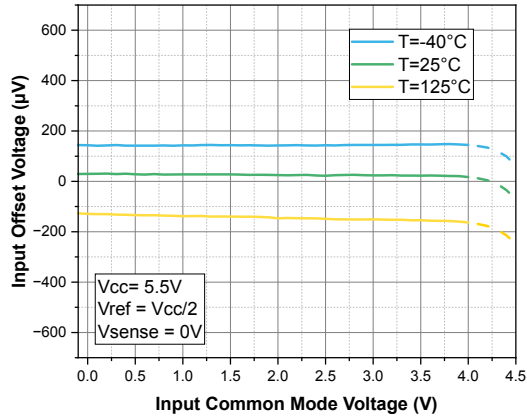
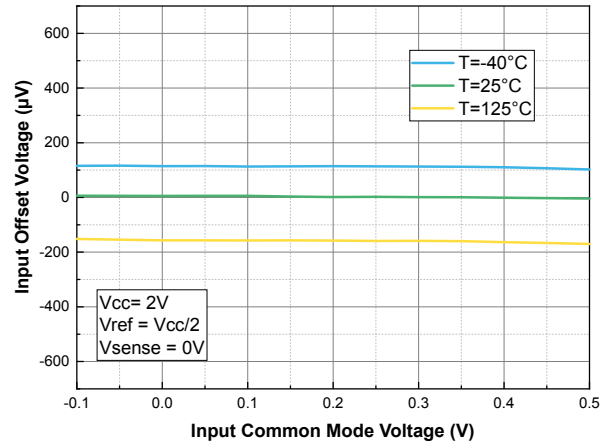
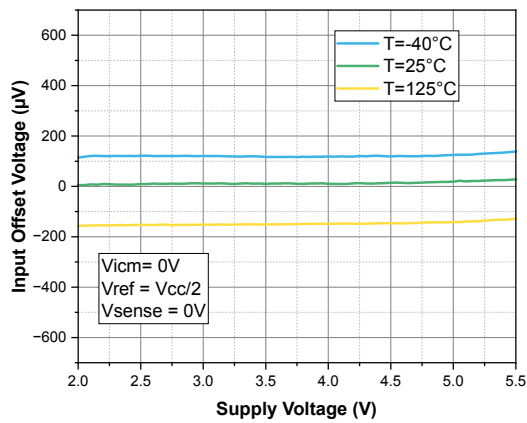
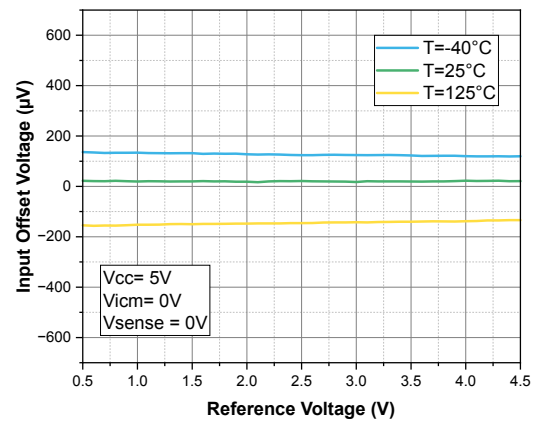
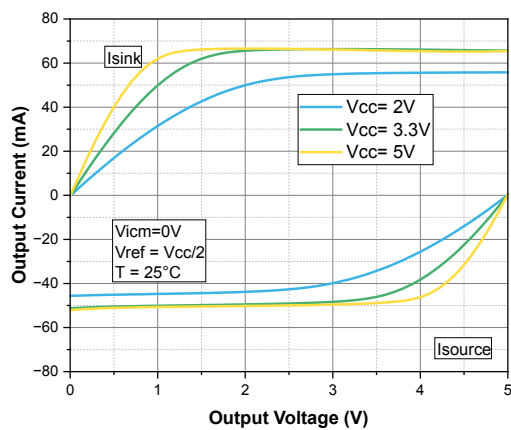
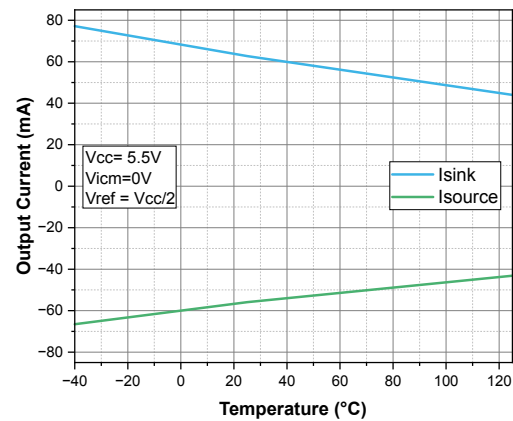
Figure 15. Input offset voltage vs. input common-mode with $V_{CC} = 5.5\text{ V}$

Figure 16. Input offset voltage vs. input common-mode with $V_{CC} = 2\text{ V}$

Figure 17. Input offset voltage vs. supply voltage

Figure 18. Input offset voltage vs. reference voltage

Figure 19. Output current vs. output voltage

Figure 20. Output current vs. temperature with $V_{CC} = 5.5\text{ V}$


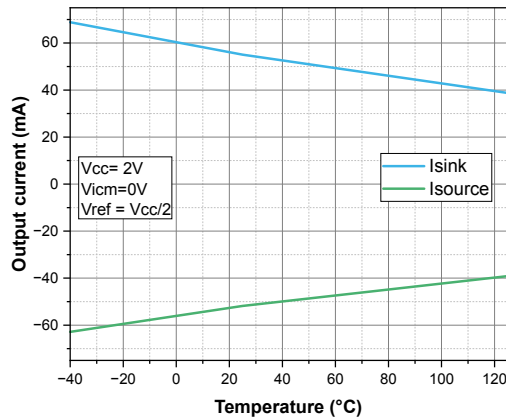
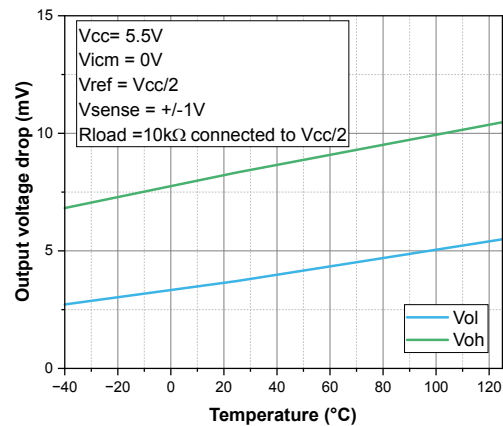
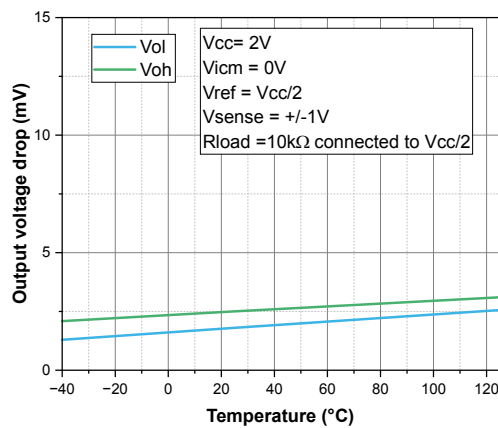
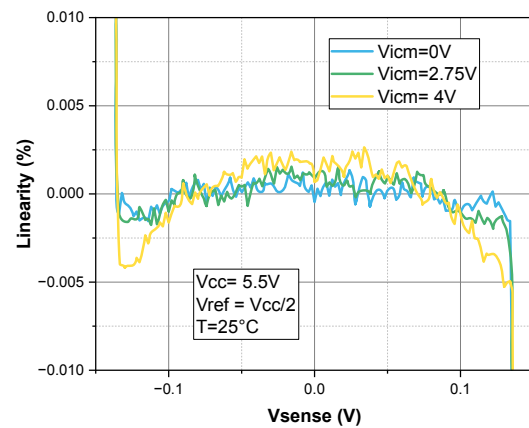
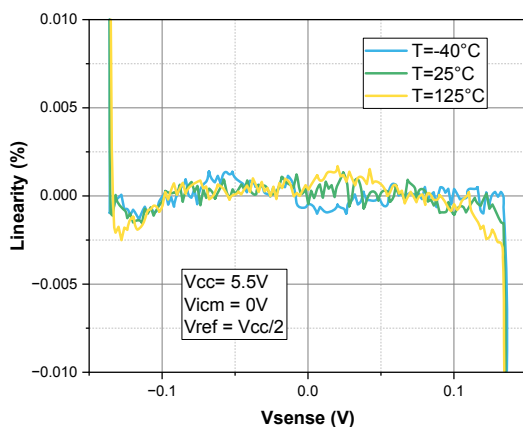
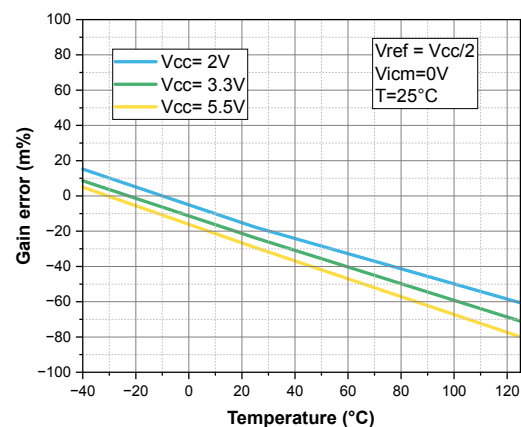
Figure 21. Output current vs. temperature with $V_{CC} = 2\text{ V}$

Figure 22. Voh and Vol vs. temperature with $V_{CC} = 5.5\text{ V}$

Figure 23. Voh and Vol vs. temperature with $V_{CC} = 2\text{ V}$

Figure 24. Linearity vs. Vsense with $V_{CC} = 5.5\text{ V}$

Figure 25. Linearity vs. Vsense and temperature

Figure 26. Gain error vs. temperature at $V_{icm} = 0\text{ V}$


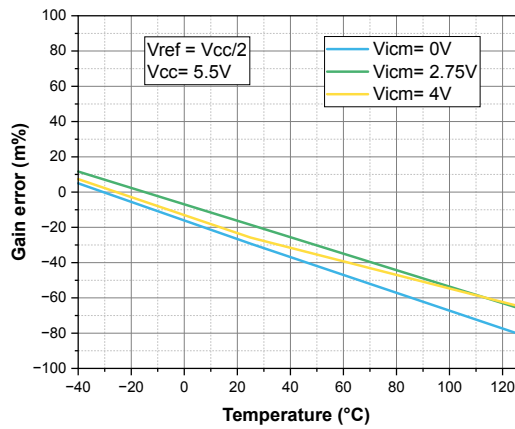
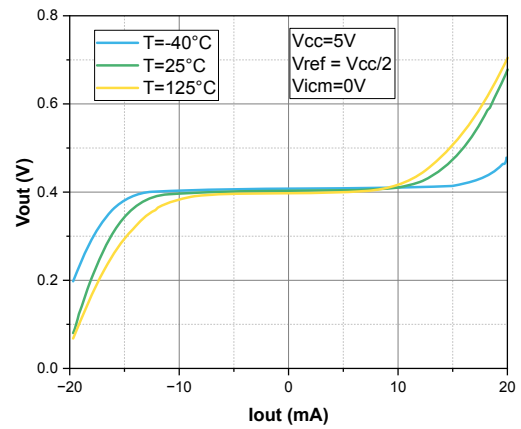
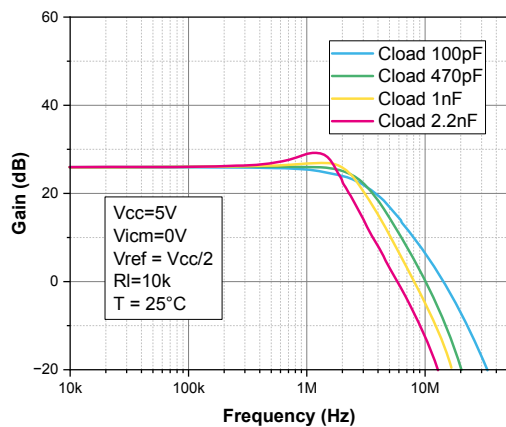
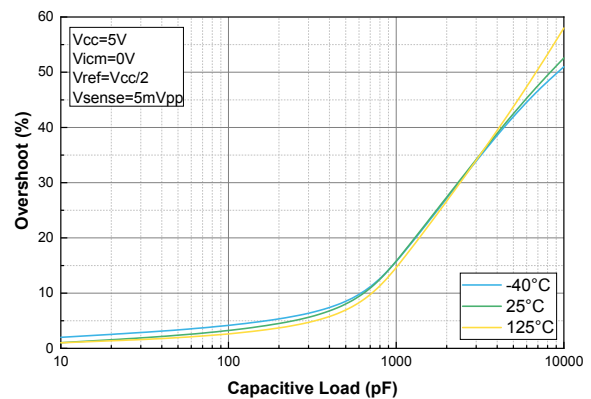
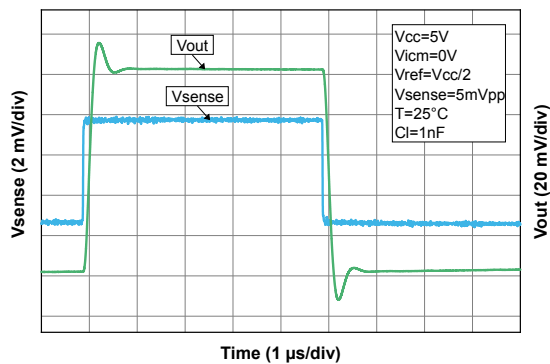
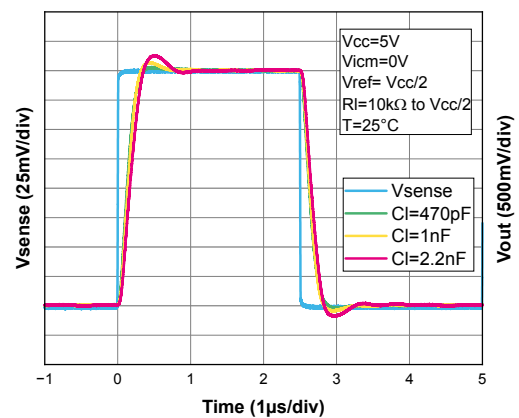
Figure 27. Gain error vs. temperature at $V_{CC} = 5.5\text{ V}$

Figure 28. Load regulation with $V_{CC} = 5\text{ V}$

Figure 29. Gain vs. frequency for different capacitive loads

Figure 30. Overshoot vs. capacitive load

Figure 31. Small signal response with $V_{CC} = 5\text{ V}$

Figure 32. Large signal response with $V_{CC} = 5\text{ V}$


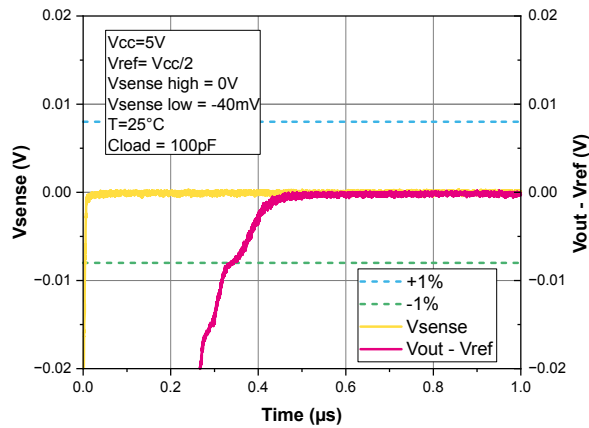
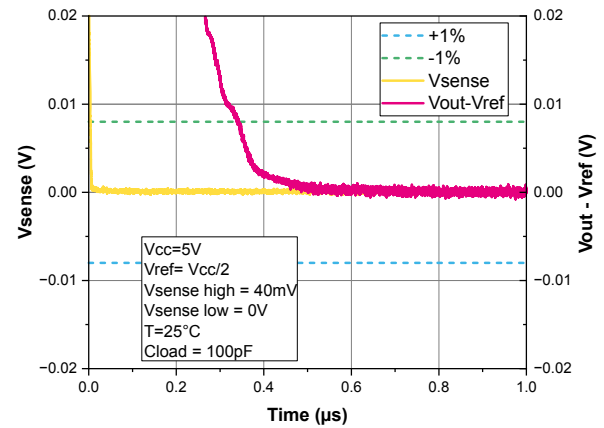
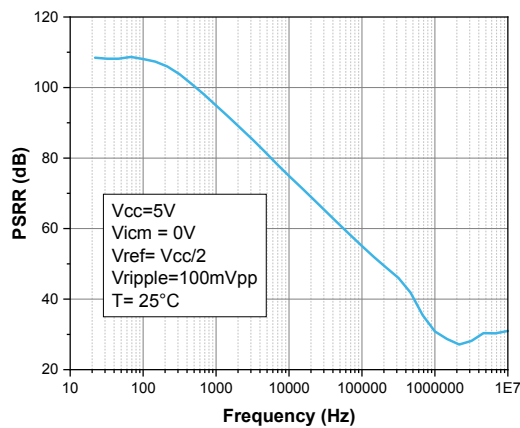
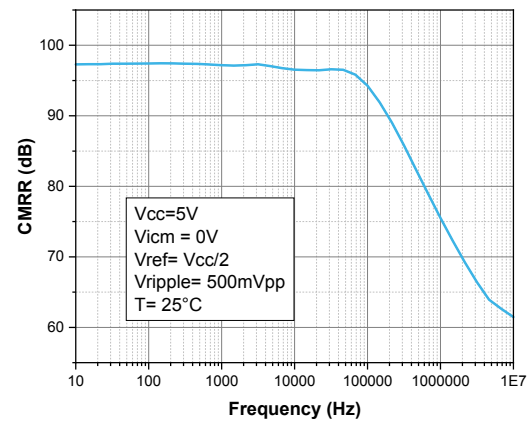
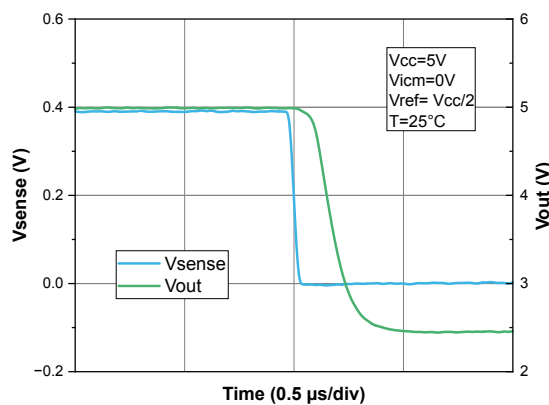
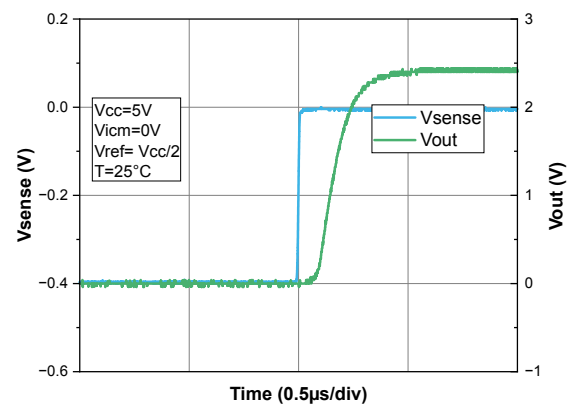
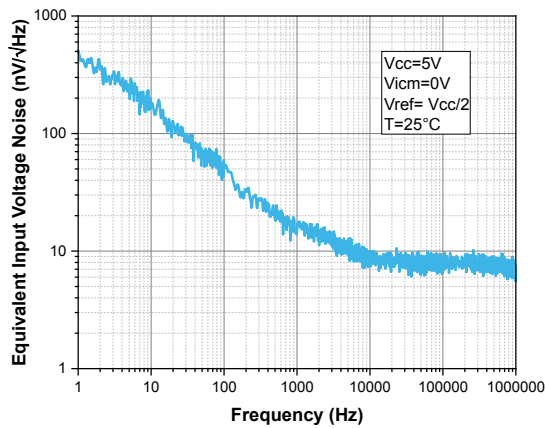
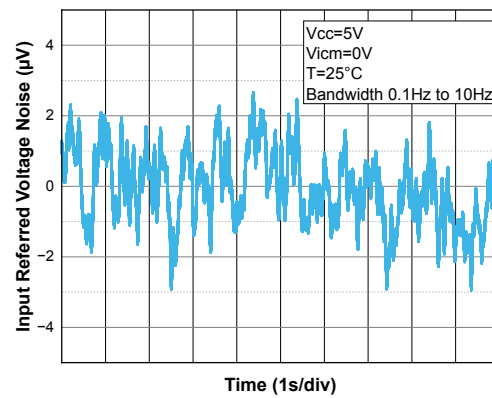
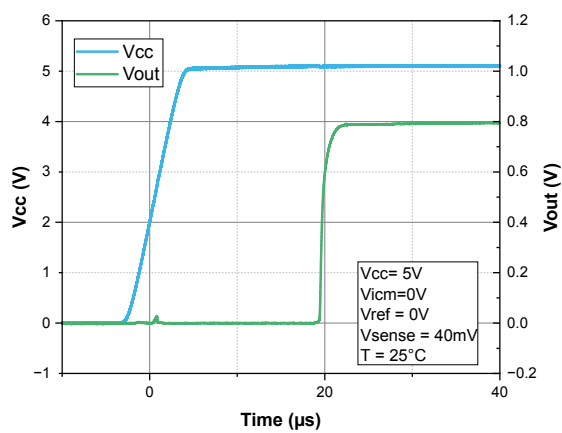
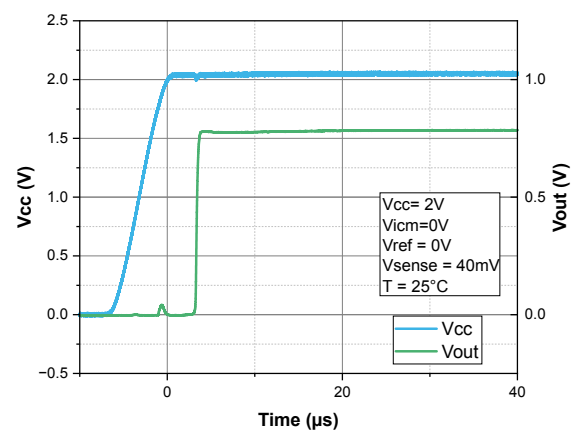
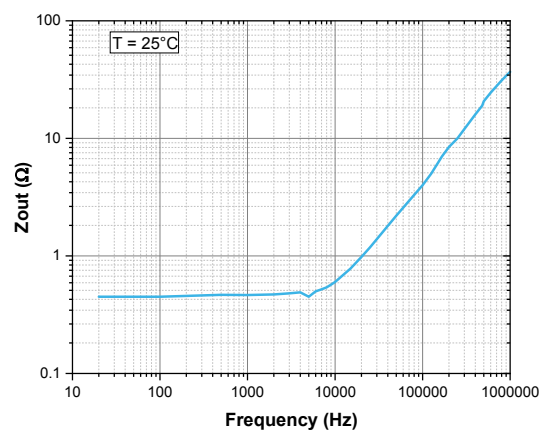
Figure 33. Settling time on rising edge

Figure 34. Settling time on falling edge

Figure 35. PSRR vs. frequency

Figure 36. CMRR vs. frequency

Figure 37. Positive overvoltage recovery

Figure 38. Negative overvoltage recovery


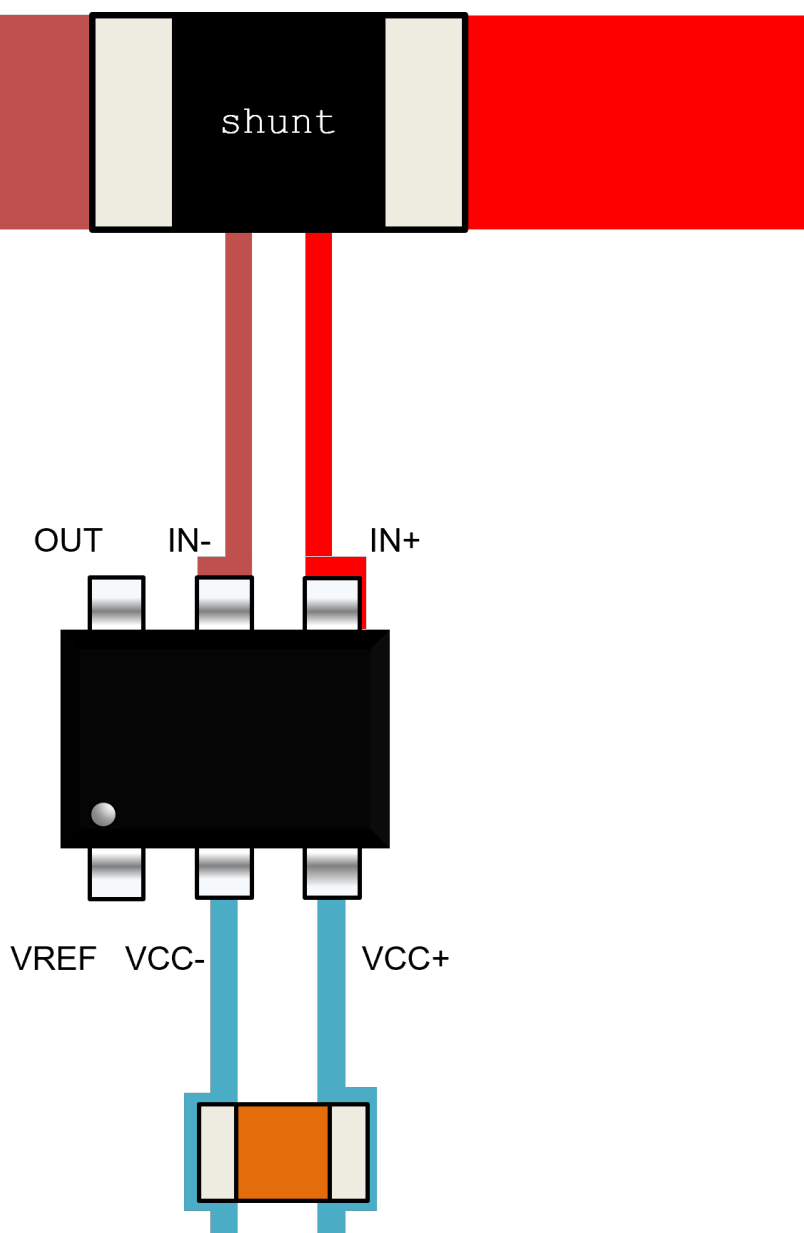
Figure 39. Noise vs. frequency

Figure 40. 0.1 Hz to 10 Hz voltage noise

Figure 41. Power up $V_{CC} = 5$ V

Figure 42. Power up $V_{CC} = 2$ V

Figure 43. Output impedance vs. frequency


7 Application information

7.1 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

Figure 44. PCB traces



7.2 Decoupling capacitor

In order to ensure op amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op amp supply pin. A good decoupling helps to reduce electromagnetic interference impact.

7.3

Macromodel

Accurate macromodels of the TSC1801 device are available on the STMicroelectronics' website at: www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSC1801 operational amplifier. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace on-board measurements.

8 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 SOT23-6 package information

Figure 45. SOT23-6 package outline

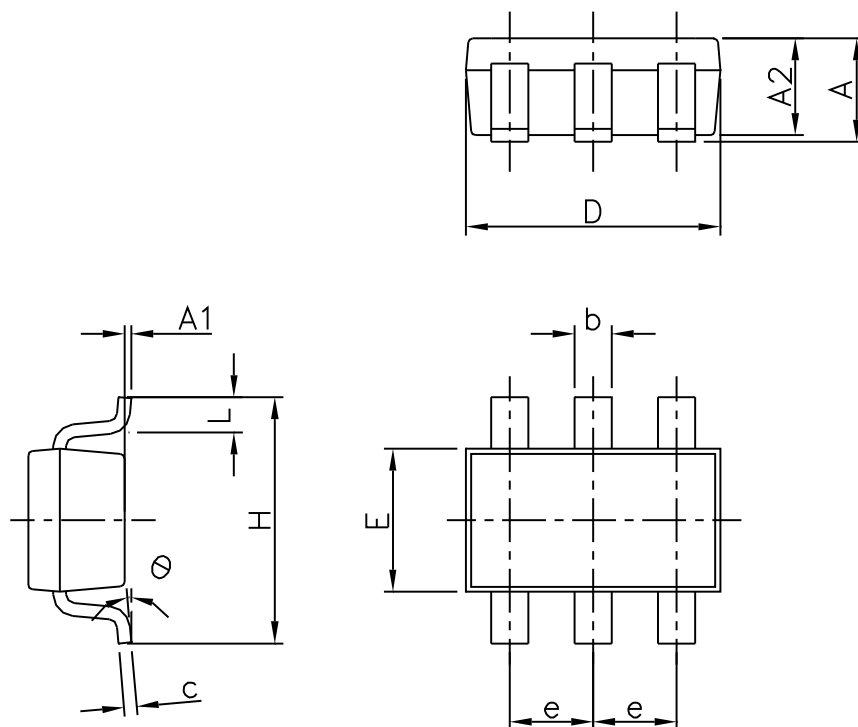


Table 6. SOT23-6 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1			0.10			0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.013		0.019
c	0.09		0.20	0.003		0.008
D	2.80		3.05	0.110		0.120
E	1.50		1.75	0.060		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0 °		10 °	0 °		10 °

9 Ordering information

Table 7. Order codes

Order code	Temperature range	Package	Marking
TSC1801BILT	-40 °C to 125 °C	SOT23-6	K314
TSC1801BIYLT	-40 °C to 125 °C automotive grade ⁽¹⁾	SOT23-6	K317

1. Qualified and characterized according to AEC-Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent. For qualification status details, click on the "Maturity Status Link" on the datasheet first page. On the product page in www.st.com, check "Quality and Reliability" tab.

Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Dec-2024	1	Initial release.
17-Jan-2025	2	Added new Section 6: Typical performance characteristics.
24-Feb-2025	3	Updated title, features, applications on the cover page, Figure 2 and Figure 44 .

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