TSC2013-Q1 12-Bit, Nanopower, 4-Wire Dual-Touch Screen Controller With I²C Interface

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- 4-Wire Touch Screen Interface
- Ratiometric Conversion
- Single 1.6-V to 3.6-V Supply:
  - I/OVDD 1.2 to 3.6 V
  - SNSVDD: 1.6 to 3.6 V
- Preprocessing to Reduce Bus Activity
- High-Speed I²C-Compatible Interface
- Internal Detection of Screen Touch
- Register-Based Programmable:
  - 10-Bit or 12-Bit Resolution
  - Sampling Rates
  - System Timing
- Touch Pressure Measurement
- Auto Power-Down Control
- Low Power:
  - 430 µA at 1.8 V, 50 SSPS
  - 320 µA at 1.6 V, 50 SSPS
  - 58 µA at 1.6 V, 8.2 kSPS Eq. Rate

2 Applications

- Automotive Infotainment Display
- Automotive Navigation System
- Industrial User Interfaces
- Medical Devices
- Portable Consumer Electronics

3 Description

The TSC2013-Q1 device is a very low-power dual-touch screen controller designed to work with power-sensitive, low-cost touch-screen displays in automotive infotainment and navigation systems. It contains a complete, ultralow-power, 12-bit, analog-to-digital (ADC) resistive touch-screen converter, including drivers and the control logic to measure touch pressure.

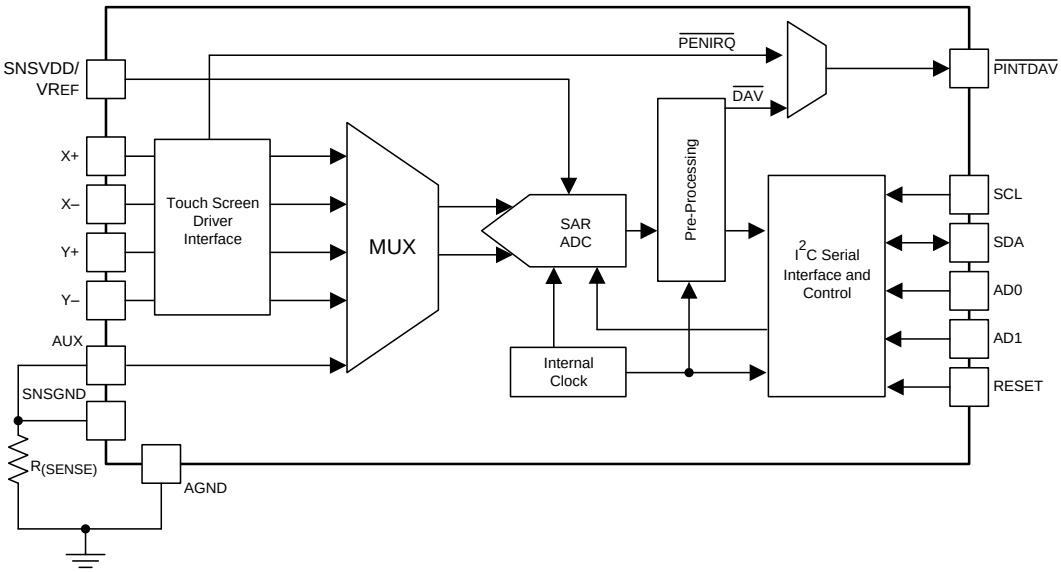
The TSC2013-Q1 device enables pinch, rotate, and zoom functionality over a standard four-wire interface. The device supports an I²C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. The 10 or 12-bit ADC within is easily programmable to customize system and user experience.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TSC2013-Q1	PVQFN (16)	4.00 mm × 4.00 mm
	TSSOP (16)	4.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram



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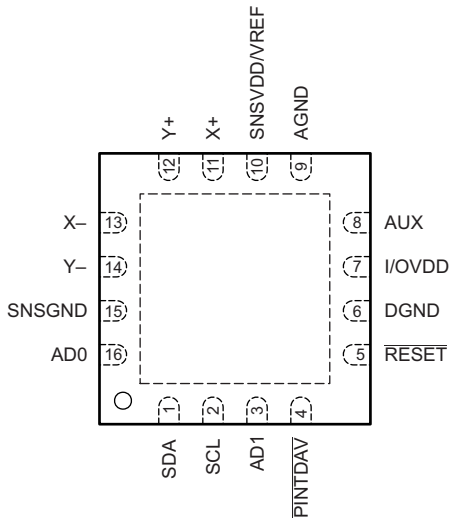
4 Revision History

Changes from Original (June 2014) to Revision A **Page**

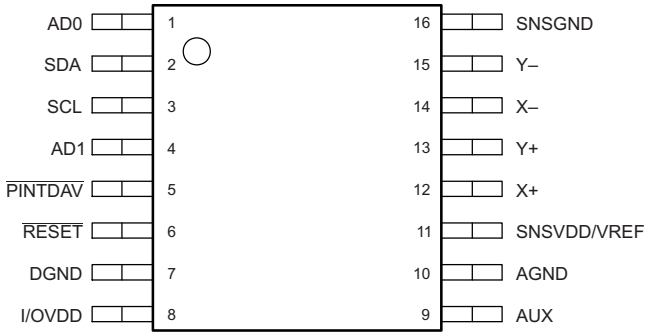
- Released full version of data sheet ... 1
- Changed device status from *Product Preview* to *Production Data* ... 1

5 Pin Configurations and Functions

16-Pin VQFN With Thermal Pad
RSA Package
Top View



16-Pin TSSOP
PW Package
Top View



Pin Functions

PIN			I/O	ADC	DESCRIPTION
NAME	RSA	PW			
AD0	16	1	I	D	I^2C bus TSC address input bit 0
AD1	3	4	I	D	I^2C bus TSC address input bit 1
AGND	9	10	—	—	Analog, digital, and ESD ground(1)
AUX	8	9	—	A	Auxiliary channel
DGND	6	7	—	—	No internal connection. Connect this pin to analog ground for mechanical stability.
I/OVDD	7	8	I	—	Digital interface voltage
$\overline{\text{PINTDAV}}$	4	5	O	D	Interrupt output. Data available or the pen-detect interrupt ($\overline{\text{PENIRQ}}$), depending on setting. Pin polarity is active-low.
$\overline{\text{RESET}}$	5	6	I	D	External hardware reset input (active-low).
SDA	1	2	I/O	D	Serial data I/O
SCL	2	3	I	D	Serial clock
SNSGND	15	16	—	—	Sensor driver return
SNSVDD/VREF	10	11	I	—	Power supply for sensor drivers and other analog blocks
X+	11	12	—	A	X+ channel
X–	13	14	—	A	X– channel
Y+	12	13	—	A	Y+ channel
Y–	14	15	—	A	Y– channel

(1) For optimized system IEC ESD performance, contact Texas Instruments for schematic and layout reviews and suggestions.

6 Specifications

6.1 Absolute Maximum Ratings[1]

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
Voltage	Analog input X+, Y+, AUX to SNSGND	–0.4	SNSVDD + 0.1	V
	Analog input X–, Y– to SNSGND	–0.4	SNSVDD + 0.1	V
	SNSVDD to SNSGND	–0.3	5	V
	SNSVDD to AGND	–0.3	5	V
	I/OVDD to AGND	–0.3	5	V
	SNSVDD to I/OVDD	–2.4	0.3	V
Digital input voltage to AGND		–0.3	I/OVDD + 0.3	V
Digital output voltage to AGND		–0.3	I/OVDD + 0.3	V
Power dissipation		$(T_{Jmax} – T_A) / R_{\theta JA}$		
Operating free-air temperature range, T_A		–40	125	°C
Junction temperature, T_{Jmax}			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (RSA: 1, 4, 5, 8, 9, 12, 13, and 16; PW: 1, 8, 9, and 16)	–750	750	
			Other pins	–500	500	
	IEC contact discharge[2]	X+, X–, Y+, Y–		–15	15	kV
	IEC air discharge[2]	X+, X–, Y+, Y–		–25	25	kV

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Test method based on IEC standard 61000-4-2. Contact Texas Instruments for test details.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage SNSVDD/VR	1.6	3.3	3.6	V
Input voltage I/OVDD	1.2	3.3	3.6	V

6.4 Thermal Information

THERMAL METRIC[1]		RSA 16 PINS	PW 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.7	100.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	36.7	36.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.5	45.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.5	45.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	2.5	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = –40°C to 125°C, $V_{(SNSVDD/VREF)}$ = 1.6 V to 3.6 V, and $V_{(I/OVDD)}$[1] = 1.2 V to $V_{(SNSVDD/VREF)}$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUXILIARY ANALOG INPUT							
	Input voltage			0		V_{ref}	V
	Input capacitance				12		pF
	Input leakage current		No ADC conversion	–1		1	µA
	Full-scale average input current		$V_{(SNSVDD/VREF)}$ = 1.6 V, continuous AUX, $f_{(ADC)}$ = 2 MHz		2		µA
ADC							
	Resolution		Programmable: 10 or 12 bits			12	Bits
	No missing codes		12-bit resolution	11			Bits
	Integral linearity		12-bit resolution mode, $f_{(ADC)}$ = 2 MHz	–3	–0.5 to 0.5	3	LSB[2]
	Differential linearity		12-bit resolution mode, f_{ADC} = 2MHz	–2	–0.5 to 0.5	4	LSB
	Offset error		$V_{(SNSVDD/VREF)}$ = 1.6 V, 12-bit mode, $f_{(ADC)}$ = 2 MHz, filter off		0.2		LSB
	Gain error		$V_{(SNSVDD/VREF)}$ = 1.6 V, 12-bit mode, $f_{(ADC)}$ = 2 MHz, filter off		2		LSB
	Data format				Straight binary		
REFERENCE INPUT							
	V_{ref} range			1.6		$V_{(SNSVDD/VREF)}$	V
	SNSVDD/VREF input-current drain		Continuous AUX mode, $V_{(SNSVDD/VREF)}$ = 1.6 V, $f_{(ADC)}$ = 2 MHz		5		µA
	Input impedance		No ADC conversion		> 100		MΩ
TOUCH SENSORS							
	X+ 50-kΩ pullup resistor, $R_{(IRQ)}$				52		kΩ
	Switch on-resistance	Y+, X+	T_A = 25°C, $V_{(SNSVDD/VREF)}$ = 1.6 V		7		Ω
		Y–, X–	T_A = 25°C, $V_{(SNSVDD/VREF)}$ = 1.6 V		5		Ω
	Switch drivers drive current		100-ms duration			50	mA
INTERNAL OSCILLATOR							
$f_{(OSC)}$	Clock frequency		$V_{(SNSVDD/VREF)}$ = 1.6 V, T_A = 25°C	3.3	3.7	4.3	MHz
			$V_{(SNSVDD/VREF)}$ = 3 V, T_A = 25°C		3.8		MHz
	Frequency drift		$V_{(SNSVDD/VREF)}$ = 1.6 V		–0.008		%/°C
			$V_{(SNSVDD/VREF)}$ = 3 V		–0.021		%/°C
DIGITAL INPUT/OUTPUT							
	Logic family				CMOS		
V_{IH}	Input-voltage logic-level high		1.2 V ≤ $V_{(I/OVDD)}$ < 3 V	0.7 × $V_{(I/OVDD)}$		3.6	V
V_{IL}	Input-voltage logic-level low		1.2 V ≤ $V_{(I/OVDD)}$ < 3 V	–0.3		0.2 × $V_{(I/OVDD)}$	V
I_{IL}, I_{IH}	Input-current logic-level low and high			–1		1	µA
C_I	Input-capacitance logic level					10	pF
V_{OH}	Output-voltage logic-level high		I_{OH} = 100 µA	$V_{(I/OVDD)}$ – 0.2		$V_{(I/OVDD)}$	V
V_{OL}	Output-voltage logic-level low		I_{OL} = –3.2 mA	0		0.2	V
I_{lkg}	Leakage-current logic level		SDA	–1		1	µA
C_O	Output-capacitance logic level		SDA			10	pF
POWER-SUPPLY REQUIREMENTS							
	Power-supply voltage						
	SNSVDD			1.6		3	V
	I/OVDD[1]			1.2		$V_{(SNSVDD/VREF)}$	V

(1) I/OVDD must be ≤ SNSVDD.
(2) LSB means least-significant bit. With SNSVDD/VREF= 2.5 V, one LSB is 610 µV.

Electrical Characteristics (continued)

At T_A = –40°C to 125°C, $V_{(SNSVDD/VREF)}$ = 1.6 V to 3.6 V, and $V_{(I/OVDD)}$[1] = 1.2 V to $V_{(SNSVDD/VREF)}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Quiescent supply current[3][4]	T_A = 25°C, filter off, M = W = 1, C[3:0] = (1, 0, 0, 0), RM = 1, CL[1:0] = (0, 1), cont AUX mode, $f_{(ADC)}$ = 2 MHz, without reading data register	$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V		420	570	µA
	T_A = 25°C, filter on, M = 15, W = 7, PSM = 1, C[3:0] = (0, 0, 0, 0), RM = 1, CL[1:0] = (0, 1), BTD[2:0] = (1, 0, 1), 50 SSPS, MAVEX = MAVEY = MAVEZ = 1, $f_{(ADC)}$ = 2 MHz, sensor drivers supply included[5]	$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V		200		µA
		$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 3 V		400		µA
	T_A = 25°C, filter off, M = W = 1, PSM = 1, C[3:0] = (0, 0, 0, 0), RM = 1, CL[1:0] = (0, 1), BTD[2:0] = (1, 0, 1), 50 SSPS, MAVEX = MAVEY = MAVEZ = 1, $f_{(ADC)}$ = 2 MHz, sensor drivers supply included[5]	$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V		180		µA
		$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 3 V		370		µA
	T_A = 25°C, filter off, M = W = 1, C[3:0] = (0, 1, 0, 1), RM = 1, CL[1:0] = (0, 1), non-cont AUX mode, $f_{(ADC)}$ = 2 MHz, high-speed mode	$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V, approximately 28 kSPS effective rate		190		µA
		$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 3 V, approximately 28.4 kSPS effective rate		370		µA
	T_A = 25°C, filter on, M = 7, W = 3, C[3:0] = (0, 1, 0, 1), RM = 1, CL[1:0] = (0, 1), MAVEAUX = 1, non-cont AUX mode, $f_{(ADC)}$ = 2 MHz, high-speed mode, full speed	$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V, approximately 10.5 kSPS effective rate		355		µA
		$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 3 V, approximately 10.9 kSPS effective rate		655		µA
	T_A = 25°C, filter on, M = 7, W = 3, C[3:0] = (0, 1, 0, 1), RM = 1, CL[1:0] = (0, 1), MAVEAUX = 1, non-cont AUX mode, $f_{(ADC)}$ = 2 MHz, high-speed mode, reduced speed (8.2-kSPS equivalent rate)	$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V, approximately 1.17 kSPS effective rate		36.2		µA
		$V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 3 V, approximately 1.17 kSPS effective rate		64.9		µA
Power-down supply current	T_A = 25°C, not addressed, SCL = SDA = 1, $\overline{RESET}$ = 1, $\overline{PINTDAV}$ = 1, $V_{(SNSVDD/VREF)}$ = I/OVDD = V_{ref} = 1.6 V			0.04	0.8	µA
Digital power-down supply current	T_A = 25°C, not addressed, SCL = SDA = 1, $\overline{RESET}$ = 1, $\overline{PINTDAV}$ = 1, $V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = V_{ref} = 1.6 V			0.04	0.8	µA

(3) Supply current from SNSVDD.
(4) For detailed information on test condition parameter and bit settings, see the section.
(5) Touch sensor modeled by 2 kΩ for X– plane and Y– plane, and 1 kΩ for Z-plane (touch resistance).

6.6 Timing Requirements — I²C Standard Mode ($f_{(SCL)}$ = 100 kHz)

All specifications typical at –40°C to 125°C, $V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V to 3 V, unless otherwise noted.

			MIN	MAX	UNIT
$t_{(WL\_RESET)}$	Reset low time(1)	See Figure 1 and Figure 37	10		µs
$f_{(SCL)}$	SCL clock frequency			100	kHz
$t_{(BUF)}$	Bus free time between a STOP and START condition	See Figure 1	4.7		µs
$t_{h(STA)}$	Hold time for (repeated) START condition		4		µs
$t_{(LOW)}$	Low period of SCL clock		4.7		µs
$t_{(HIGH)}$	High period of the SCL clock		4		µs
$t_{su(STA)}$	Setup time for a repeated START condition		4.7		µs
$t_{h(DAT)}$	Data hold time		0	3.45	µs
$t_{su(DAT)}$	Data setup time		250		ns
t_r	Rise time of both SDA and SCL signals	$C_{(b)}$ = total bus capacitance See Figure 1		1000	ns
t_f	Fall time of both SDA and SCL signals			300	ns
$t_{su(STO)}$	Setup time for STOP condition	See Figure 1	4		µs
$C_{(b)}$	Capacitive load for each bus line	$C_{(b)}$ = total capacitance of one bus line in pF		400	pF
$t_{d(SP)}$	Pulse duration of spikes that must be suppressed by the input filter		N/A	N/A	ns

(1) $V_{(SNSVDD/VREF)}$ ≥ 1.6 V

6.7 Timing Requirements — I²C Fast Mode ($f_{(SCL)}$ = 400 kHz)

All specifications typical at –40°C to 125°C, $V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V to 3 V, unless otherwise noted.

			MIN	MAX	UNIT
$t_{(WL\_RESET)}$	Reset low time(1)	See Figure 1 and Figure 37	10		µs
$f_{(SCL)}$	SCL clock frequency			400	kHz
$t_{(BUF)}$	Bus free time between a STOP and START condition	See Figure 1	1.3		µs
$t_{h(STA)}$	Hold time for (repeated) START condition		0.6		µs
$t_{(LOW)}$	Low period of SCL clock		1.3		µs
$t_{(HIGH)}$	High period of the SCL clock		0.6		µs
$t_{su(STA)}$	Setup time for a repeated START condition		0.6		µs
$t_{h(DAT)}$	Data hold time		0	0.9	µs
$t_{su(DAT)}$	Data setup time		100		ns
t_r	Rise time of both SDA and SCL signals	$C_{(b)}$ = total bus capacitance See Figure 1	20 + 0.1 × $C_{(b)}$	300	ns
t_f	Fall time of both SDA and SCL signals(2)		20 + 0.1 × $C_{(b)}$	300	ns
$t_{su(STO)}$	Setup time for STOP condition	See Figure 1	0.6		µs
$C_{(b)}$	Capacitive load for each bus line	$C_{(b)}$ = total capacitance of one bus line in pF		400	pF
$t_{d(SP)}$	Pulse duration of spikes that must be suppressed by the input filter		0	50	ns

(1) $V_{(SNSVDD/VREF)}$ ≥ 1.6 V
(2) $C_{(b)}$ = the total capacitance of one bus line in pF. If using both fast-mode and Hs-mode devices, one may use faster fall times according to the *Timing Requirements — I²C High-Speed Mode ($f_{(SCL)}$ = 3.4 MHz)* section. Note that the TSC2013-Q1 device is an Hs-mode device and follows the table requirements listed in the *Timing Requirements — I²C High-Speed Mode ($f_{(SCL)}$ = 3.4 MHz)* section.

6.8 Timing Requirements — I²C High-Speed Mode ($f_{(SCL)}$ = 1.7 MHz)

All specifications typical at –40°C to 125°C, $V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = to 3 V, unless otherwise noted.

			MIN	MAX	UNIT
$t_{(WL\_RESET)}$	Reset low time(1)	See Figure 2 and Figure 37	10		µs
$f_{(SCL)}$	SCL clock frequency			1.7	MHz
$t_{h(STA)}$	Hold time of (repeated) START condition	See Figure 2	160		ns
$t_{(LOW)}$	Low period of SCL clock		320		ns
$t_{(HIGH)}$	High period of the SCL clock		120		ns
$t_{su(STA)}$	Setup time for a repeated START condition		160		ns
$t_{h(DAT)}$	Data hold time		0	150	ns
$t_{su(DAT)}$	Data setup time		10		ns
$t_{r(CL)}$	Rise time of SCL signal	$C_{(b)}$ = total bus capacitance(2) See Figure 2	20	80	ns
$t_{r(DA)}$	Rise time of SDA signal		20	160	ns
$t_{f(CL)}$	Fall time of SCL signal		20	80	ns
$t_{f(DA)}$	Fall time of SDA signal		1	160	ns
$t_{r(CL1)}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit		20	160	ns
$t_{su(STO)}$	Setup time for STOP condition	See Figure 2	160		ns
$C_{(b)}$	Capacitive load for each bus line	$C_{(b)}$ = total capacitance of one bus line in pF		400	pF
$t_{d(SP)}$	Pulse duration of spikes that must be suppressed by the input filter		0	10	ns

(1) $V_{(SNSVDD/VREF)}$ ≥ 1.6 V
(2) For capacitive bus loads between 100 pF and 400 pF, interpolate the rise-time and fall-time values linearly.

6.9 Timing Requirements — I²C High-Speed Mode ($f_{(SCL)}$ = 3.4 MHz)

All specifications typical at –40°C to 125°C, $V_{(SNSVDD/VREF)}$ = $V_{(I/OVDD)}$ = 1.6 V(1) to 3 V, unless otherwise noted.

			MIN	MAX	UNIT
$t_{(WL\_RESET)}$	Reset low time(2)	See Figure 2 and Figure 37	10		µs
$f_{(SCL)}$	SCL clock frequency			3.4	MHz
$t_{h(STA)}$	Hold time for (repeated) START condition	See Figure 2	160		ns
$t_{(LOW)}$	Low period of SCL clock		160		ns
$t_{(HIGH)}$	High period of the SCL clock		60		ns
$t_{su(STA)}$	Setup time for a repeated START condition		160		ns
$t_{h(DAT)}$	Data hold time		0	70	ns
$t_{su(DAT)}$	Data setup time		10		ns
$t_{r(CL)}$	Rise time of SCL signal	$C_{(b)}$ = total bus capacitance(3) See Figure 2	10	40	ns
$t_{r(DA)}$	Rise time of SDA signal		10	80	ns
$t_{f(CL)}$	Fall time of SCL signal		10	40	ns
$t_{f(DA)}$	Fall time of SDA signal		1	80	ns
$t_{r(CL1)}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit		10	80	ns
$t_{su(STO)}$	Setup time for STOP condition	See Figure 2	160		ns
$C_{(b)}$	Capacitive load for each bus line	$C_{(b)}$ = total capacitance of one bus line in pF		100	pF
$t_{d(SP)}$	Pulse duration of spikes that must be suppressed by the input filter		0	10	ns

(1) Because of the low supply voltage of 1.2 V and the wide temperature range of –40°C to 125°C, the I²C system devices may not reach the maximum specification of I²C high-speed mode, and $f_{(SCL)}$ may not reach 3.4 MHz.
(2) $V_{(SNSVDD/VREF)}$ ≥ 1.6 V
(3) Capacitive load from 10 pF to 100 pF.

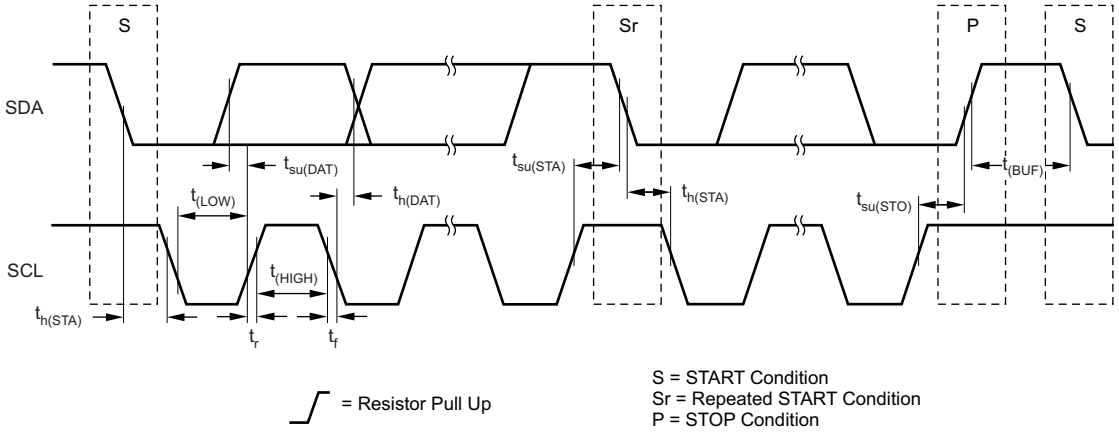
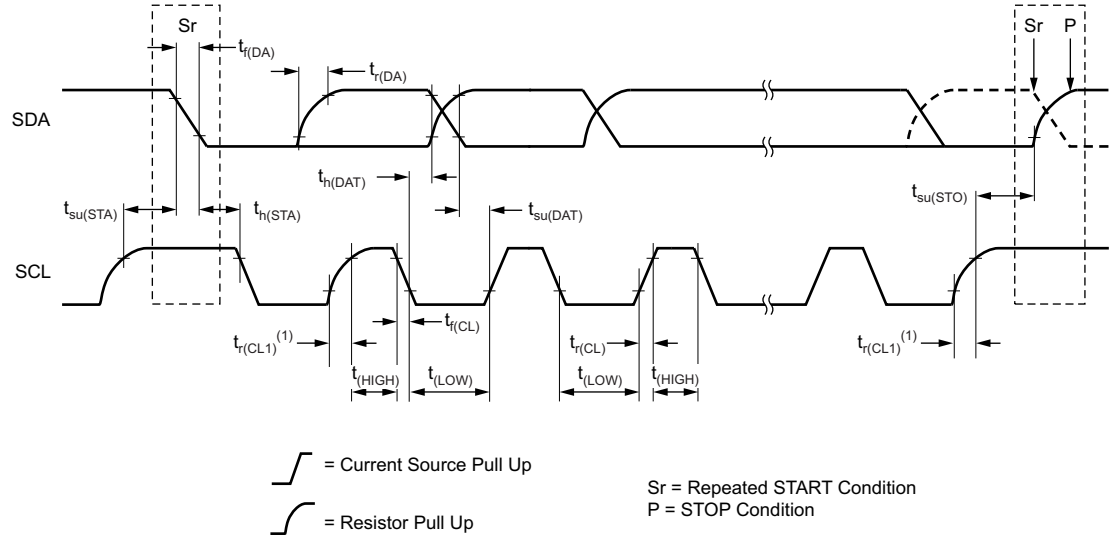


Figure 1. Detailed I/O Timing for Standard and Fast Modes



(1) The First rising edge of the SCL signal after Sr and after each acknowledge bit.

Figure 2. Detailed I/O Timing for High-Speed Mode

6.10 Typical Characteristics

At T_A = –40°C to 125°C, SNSVDD/VREF = 1.6 V to 3 V, I/OVDD = 1.2 V to SNSVDD/VREF, $f_{(ADC)} = f_{(OSC)} / 2$, high-speed mode ($f_{(SCL)}$ = 3.4 MHz), 12-bit mode, and non-continuous AUX measurement, unless otherwise noted.

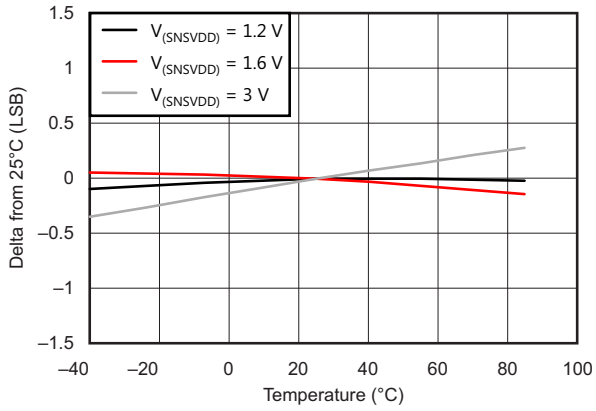


Figure 3. Change in Offset vs Temperature

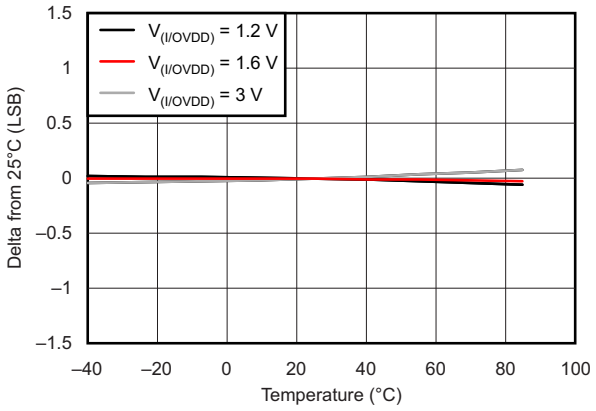
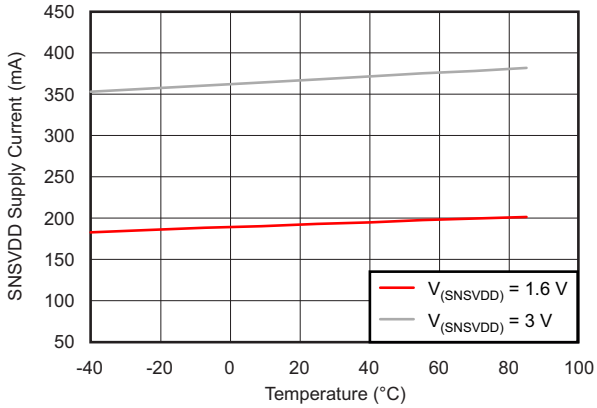
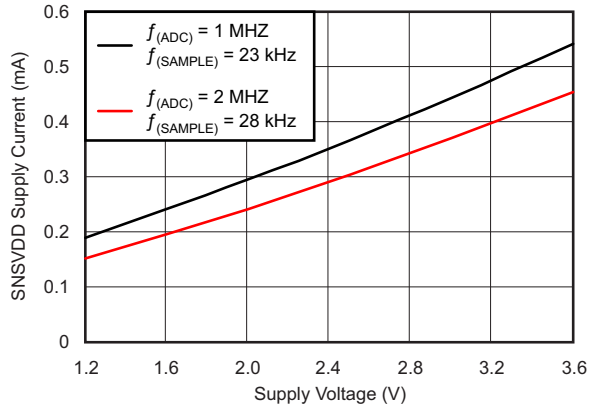


Figure 4. Change in Gain vs Temperature



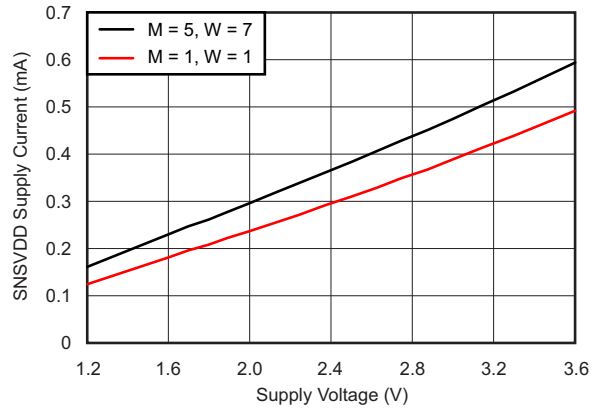
M = 1 W = 1 (See Table 1) $f_{(SAMPLE)}$ = 28 kHz
AUX non-continuous mode

Figure 5. SNSVDD Supply Current vs Temperature



T_A = 25° C

Figure 6. SNSVDD Supply Current vs SNSVDD Supply Voltage



$t_{(PVS)}$, $t_{(PRE)}$, $t_{(SNS)}$ = default values
TSC-initiated mode scan X, Y, and Z at 50SSPS
Touch sensor modeled by: 2 kΩ for X-plane and Y-plane and 1 kΩ for Z (touch resistance, See Figure 14)

Figure 7. Supply Current vs Supply Voltage, T_A = 25° C

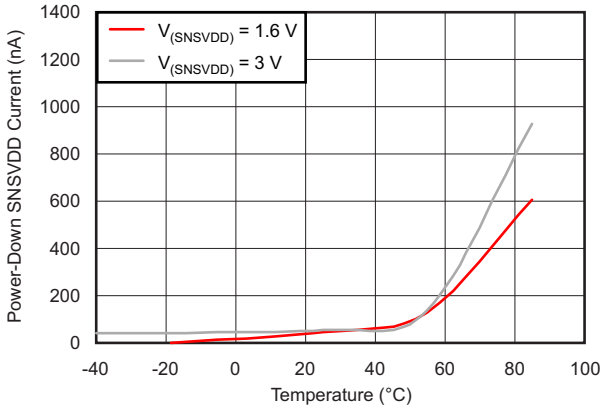
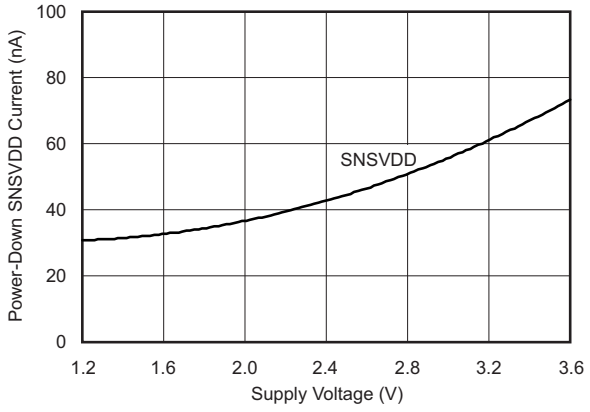


Figure 8. Power-Down Supply Current vs Temperature

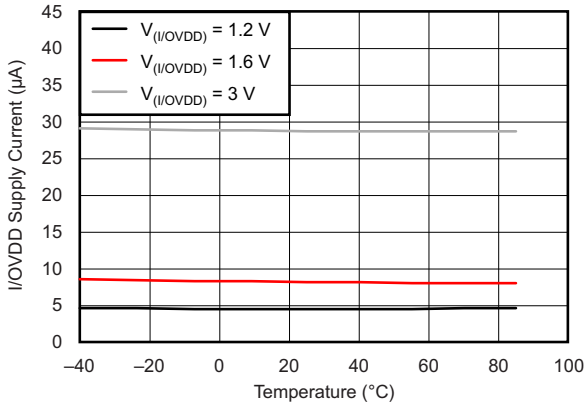
Typical Characteristics (continued)

At T_A = –40°C to 125°C, SNSVDD/VREF = 1.6 V to 3 V, I/OVDD = 1.2 V to SNSVDD/VREF, $f_{(ADC)} = f_{(OSC)} / 2$, high-speed mode ($f_{(SCL)}$ = 3.4 MHz), 12-bit mode, and non-continuous AUX measurement, unless otherwise noted.



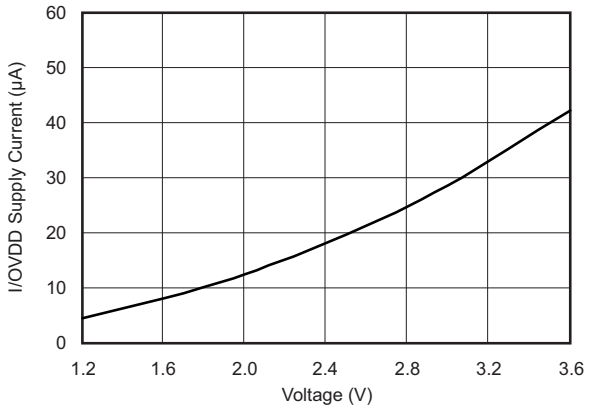
T_A = 25°C

Figure 9. Power-Down Supply Current vs Supply Voltage



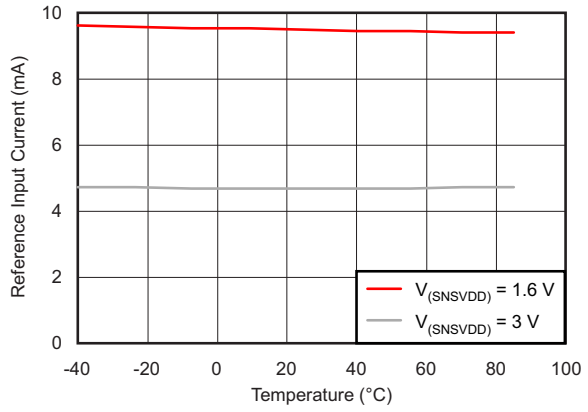
I/OVDD = SNSVDD/VREF

Figure 10. I/OVDD Supply Current vs Temperature



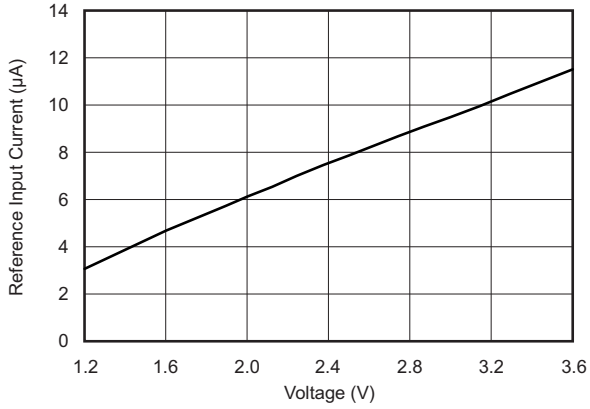
IOVDD = SNSVDD/VREF $f_{(SAMPLE)}$ = 28 kHz

Figure 11. I/OVDD Supply Current vs I/OVDD Supply Voltage



IOVDD = SNSVDD/VREF AUX continuous mode

Figure 12. Reference Input Current vs Temperature



IOVDD = SNSVDD/VREF AUX continuous mode
T_A = 25°C

Figure 13. Reference Input Current vs SNSVDD Supply Voltage

7 Detailed Description

7.1 Overview

The TSC2013-Q1 device is an analog interface circuit for a human-interface touch-screen device. A register-based architecture eases integration with microprocessor-based systems through a standard I^2C bus. Registers and onboard state machines control all peripheral functions. The TSC2013-Q1 features include:

- Very low-power touch-screen controller
- Very small onboard footprint
- Flexible preprocessing which relieves the host from tedious routine tasks and saves resources for more critical tasks
- Ability to work on very low supply voltage
- Minimal connection interface allows easiest isolation and reduces the number of dedicated I/O pins required
- Enhanced ESD protection
- Panel-current sensing
- Miniature device, yet complete; requires no external supporting components

NOTE

Although the TSC2013-Q1 device can use an external reference, the SNSVDD/VREF pin can also be used as the reference.

The TSC2013-Q1 device consists of the following blocks (see the *Functional Block Diagram* section):

- Touch-screen interface
- Auxiliary input (AUX)
- Acquisition-activity preprocessing
- Internal conversion clock
- I^2C interface

Communication with the TSC2013-Q1 device is through an I^2C serial interface. The TSC2013-Q1 device is an I^2C slave device. Therefore, data shifts into or out of the TSC2013-Q1 device under the control of the host microprocessor, which also provides the serial data clock.

Writing to different registers in the TSC2013-Q1 device controls the TSC2013-Q1 device and device functions. The use of a simple command protocol (compatible with I^2C) addresses these registers. This protocol can be an I^2C write-address followed by multiple control bytes, or multiple combinations of control and data bytes for writing into different registers (two bytes each). To read from registers, write an I^2C read-address to the TSC2013-Q1 device, followed by one or multiple sequential reads from the registers.

The host writes the address of the register to be read in control byte 0 with the register address and read-bit (as described in the previous paragraph). The register address serves as a pointer to the register map where the first read starts. This designated register address is static and a write to a register address does not need to occur again unless a new register address has overwritten it or after a TSC2013-Q1 reset (by a software reset or by the $\overline{\text{RESET}}$ pin).

The touch-measurement result goes into the TSC2013-Q1 registers, from which the host may read it at any time. This preprocessing frees up the host in order to allocate resources to more-critical tasks. Two optional signals are also available from the TSC2013-Q1 device to indicate that data are available for the host to read. The $\overline{\text{PINTDAV}}$ pin is a programmable interrupt or status output pin. With the $\overline{\text{PINTDAV}}$ pin programmed as a $\overline{\text{DAV}}$ output, the pin indicates that an ADC conversion has completed and that data are available. With the $\overline{\text{PINTDAV}}$ pin programmed as a $\overline{\text{PENIRQ}}$ output, the pin indicates the detection of a touch on the touch screen. The status register of the TSC2013-Q1 device provides an extended status reading, including the state of the $\overline{\text{DAV}}$ and $\overline{\text{PENIRQ}}$ outputs, without the cost of any dedicated pin. See Figure 14 for a typical application of the TSC2013-Q1 device.

To detect two touches, add an external $R_{(SENSE)}$ resistor as shown in Figure 14. The value of $R_{(SENSE)}$ depends on the touch-panel resistance. The ratio between the lowest touch-panel resistance and $R_{(SENSE)}$ should be approximately 4.5.

Overview (continued)

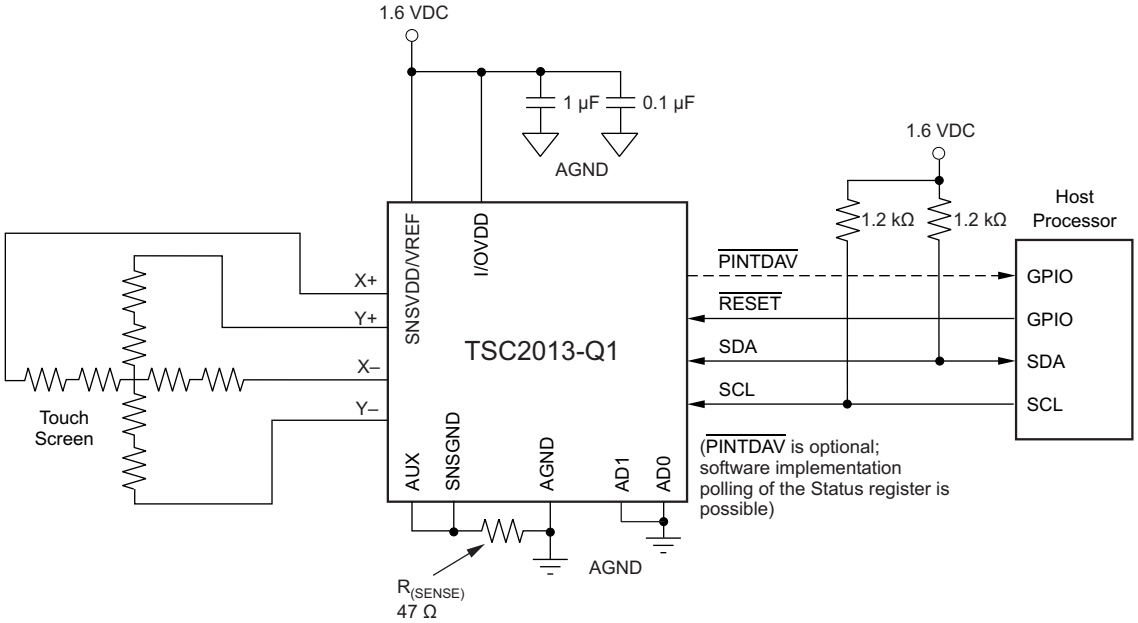
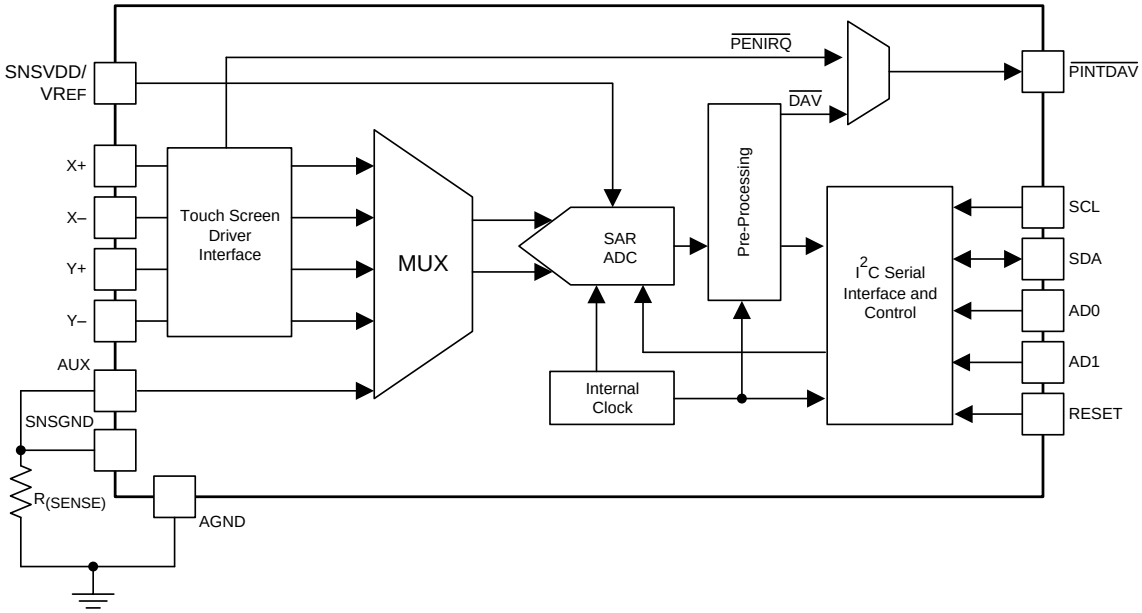


Figure 14. Typical Circuit Configuration

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Touch-Screen Operation

A resistive touch screen operates by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where an input (stylus, pen, or finger) touches the screen. The change in the resistance ratio marks the location on the touch screen.

The TSC2013-Q1 device supports resistive 4-wire configurations as shown in Figure 15. The circuit determines location in two coordinate-pair dimensions, although addition of a third dimension for measuring pressure is possible.

7.3.2 4-Wire Touch Screen Measurements

Figure 15 shows construction of a typical four-wire touch screen. The screen consists of two transparent resistive layers separated by insulating spacers.

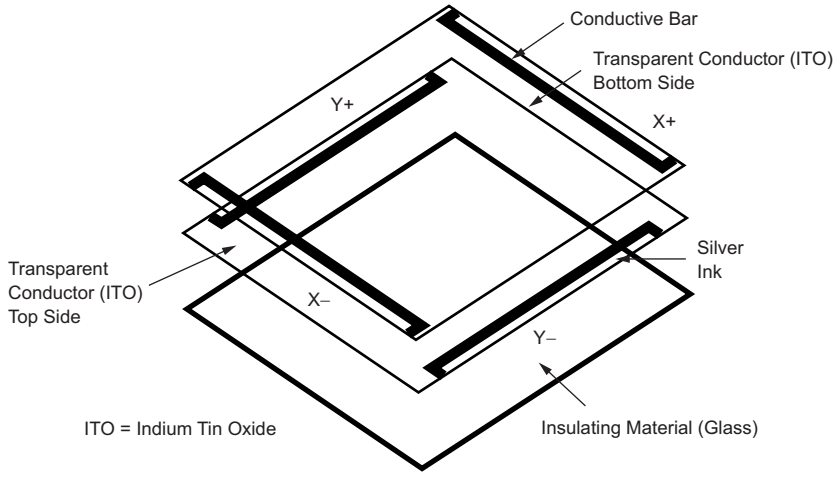


Figure 15. Four-Wire Touch Screen Construction

The four-wire touch-screen panel works by applying a voltage across the vertical or horizontal resistive network.

To determine a touch location, the TSC2013-Q1 device provides a set of eight data measurements (X1, X2, IX, Y1, Y2, IY, Z1, and Z2). Figure 17 through Figure 19 show the internal ADC configurations. Taking an X1 measurement involves activating the X+ and X– drivers and digitizing the voltage at Y+. The $R_{(SENSE)}$ resistor must be connected as shown in Figure 14. The SNSGND and AUX pins connect to one end of $R_{(SENSE)}$, and the other end connects to the AGND pin.

The TSC2013-Q1 device can also measure touch pressure (Z). To determine a pen or finger touch, determination of the pressure of the *touch* is required. Generally, having very high performance for this test is not necessary. Therefore, TI recommends 10-bit resolution mode. Several different ways of performing this measurement are available. The TSC2013-Q1 device supports two methods. The first method requires knowing the X-plate resistance, the measurement of X1, and two additional cross-panel measurements (Z2 and Z1) of the touch screen (see Figure 16). Equation 1 calculates the touch resistance ($R_{(TOUCH)}$).

$$R_{(TOUCH)} = R_{X(PLATE)} \times \frac{X1}{4096} \times \left(\frac{Z2}{Z1} - 1 \right) \quad (1)$$

The second method requires knowing both the X-plate and Y-plate resistance, and the measurement of X1, Y1, and Z1. Equation 2 also calculates the touch resistance.

$$R_{(TOUCH)} = \frac{R_{X(PLATE)}}{4096} \left(\frac{4096}{Z1} - 1 \right) - R_{Y(PLATE)} \times \left(1 - \frac{Y1}{4096} \right) \quad (2)$$

Feature Description (continued)

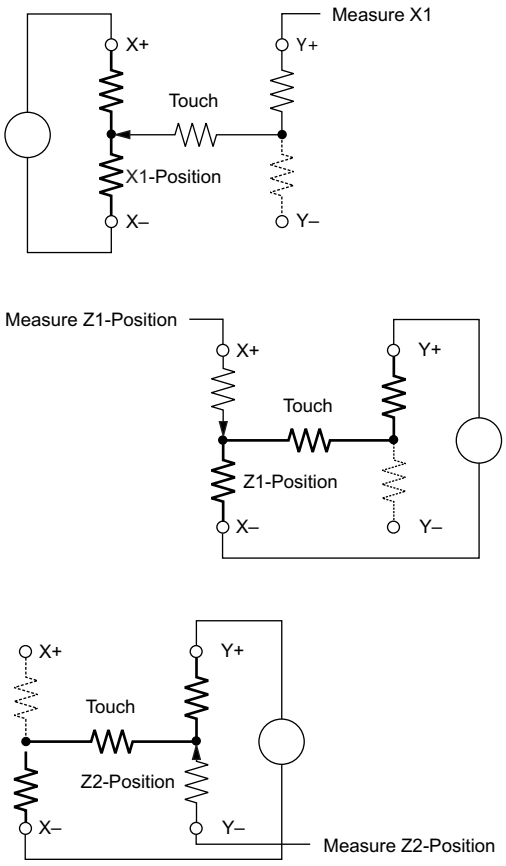


Figure 16. Pressure Measurement

Feature Description (continued)

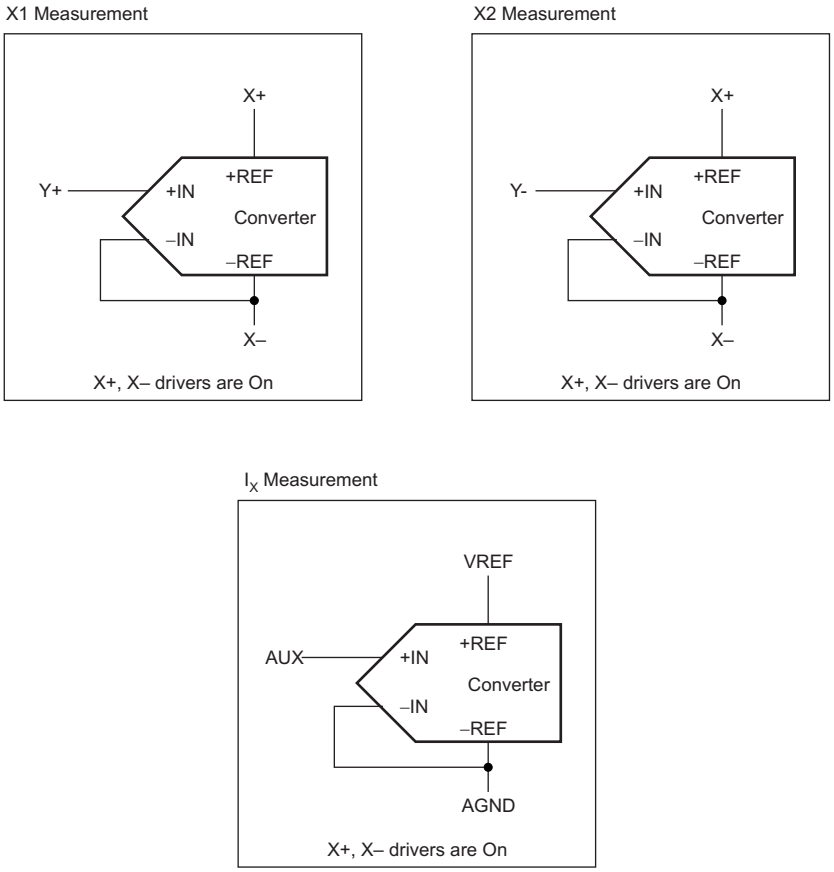


Figure 17. X-Coordinate Differential-Triplet Measurement (X1, X2, IX)

Feature Description (continued)

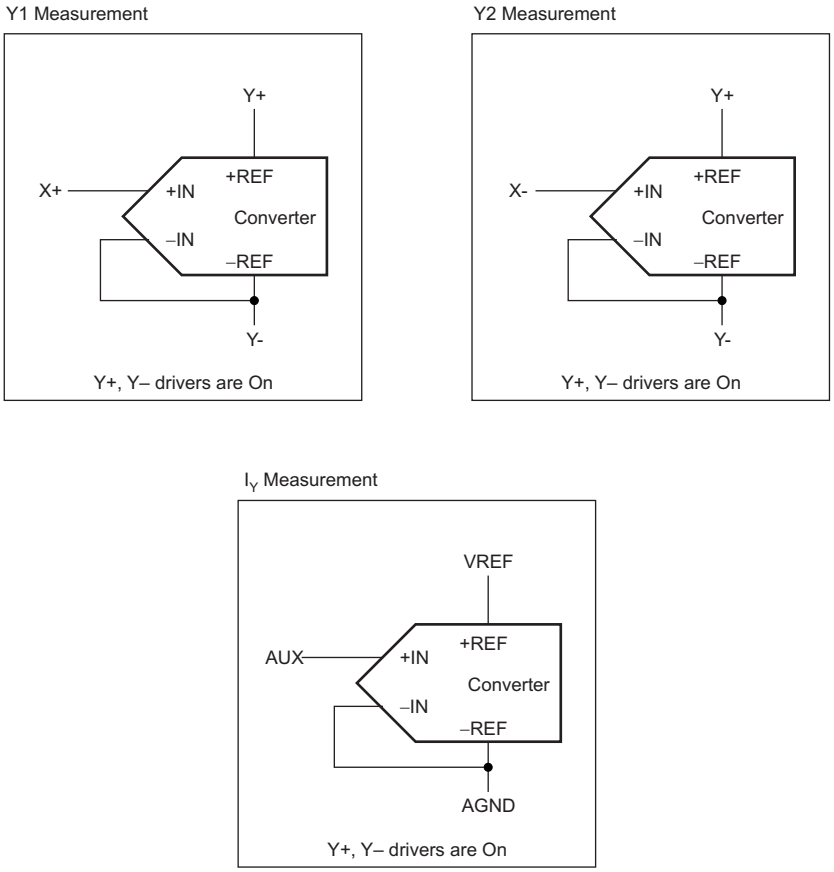


Figure 18. Y-Coordinate-Differential-Triplet Measurement (Y1, Y2, IY)

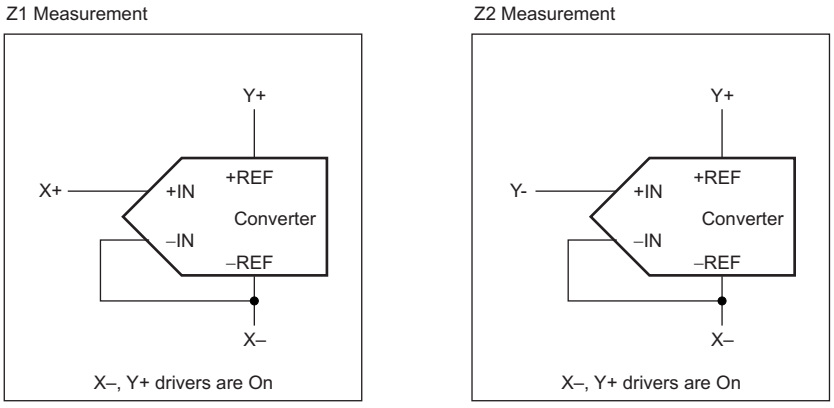


Figure 19. Z-Measurement (Z1, Z2)

When touching or pressing the touch panel with the drivers to the panel turned on, the voltage across the touch panel often overshoots and then slowly settles down (decays) to a stable DC value. This effect is a result of mechanical bouncing caused by vibration of the top-layer sheet of the touch panel when pressing the panel. Without accounting for this settling time, the converted value is in error. Therefore, introducing a delay between the time the driver for a particular measurement is turned on and the time a measurement is made is necessary.

Feature Description (continued)

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (such as noise generated by the LCD panel or back-light circuitry). The value of these capacitors provides a low-pass filter to reduce noise, but causes an additional settling-time requirement when the panel is touched.

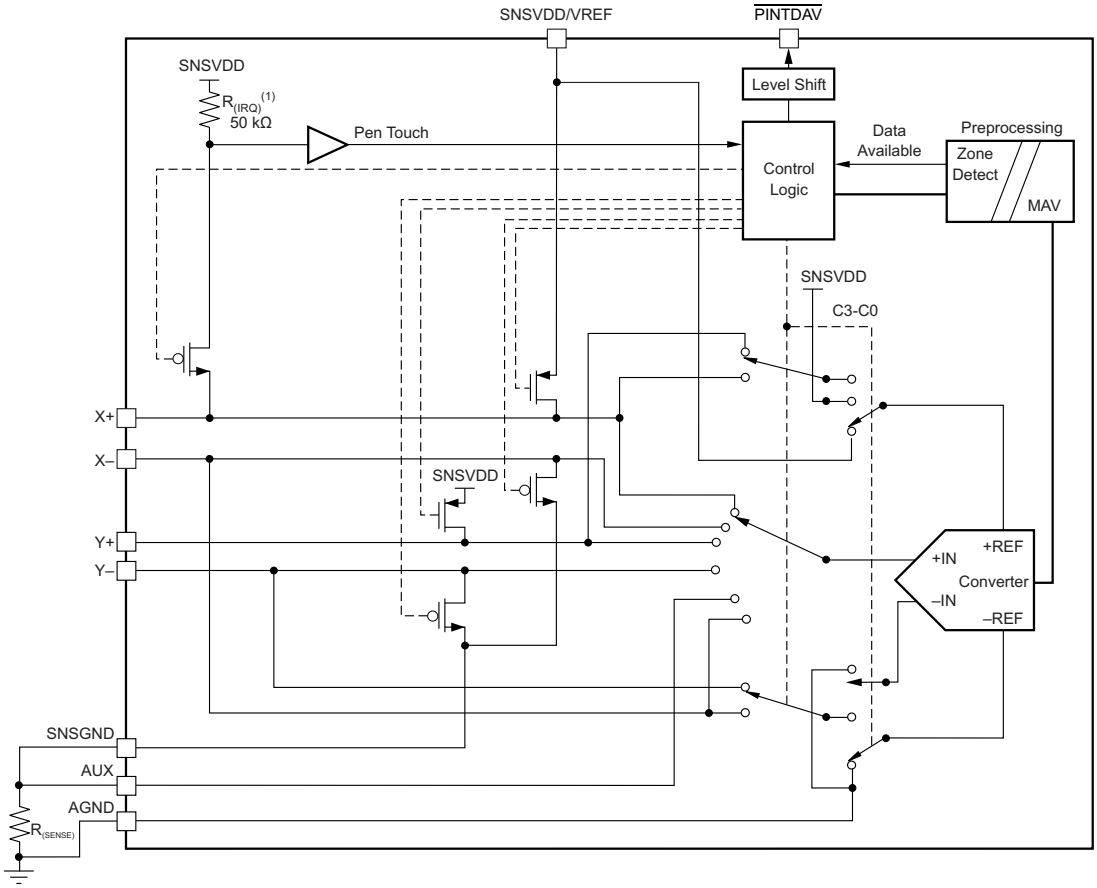
The TSC2013-Q1 device offers several solutions to this problem. A programmable delay time is available that sets the delay between turning the drivers on and making a conversion. The TSC2013-Q1 device uses this delay, referred to as the *panel voltage-stabilization time*, in some of the device modes. In other modes, commands can cause the TSC2013-Q1 device to turn on the drivers only without performing a conversion. Issuing the command to perform a conversion occurs after allowing sufficient stabilization time.

The TSC2013-Q1 touch-screen interface can measure different data sets. Determination of these measurements is possible under three different modes of the ADC:

- TSMode1: conversion controlled by the TSC2013-Q1 device and initiated by the touchscreen controller (TSC)
- TSMode2: conversion controlled by the TSC2013-Q1 device and initiated by the host responding to the $\overline{\text{PENIRQ}}$ signal
- TSMode3: conversion completely controlled by the host processor

7.3.3 Analog-to-Digital Converter

Figure 20 shows the analog inputs of the TSC2013-Q1 device. A multipexer provides the analog inputs (X, Y, and Z touch panel coordinates and auxiliary inputs) to the successive-approximation register (SAR) analog-to-digital converter (ADC). The basis of ADC architecture is capacitive redistribution architecture, which inherently includes a sample-and-hold function.



(1) Untrimmed resistor; see the typical value in the table.

Figure 20. Simplified Diagram of the Analog Input Section

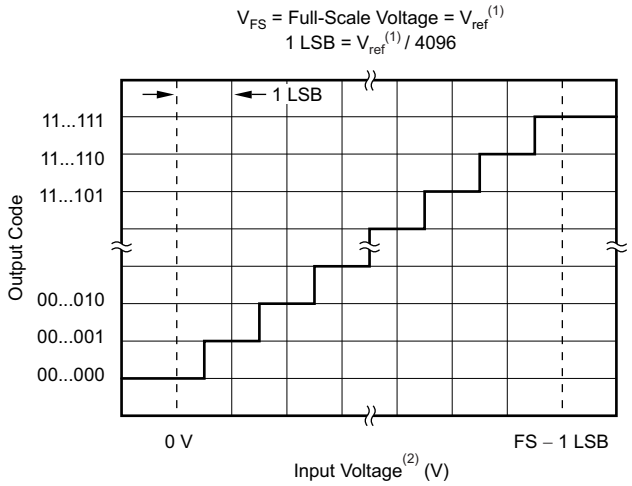
Feature Description (continued)

A unique configuration of low on-resistance switches allows an unselected ADC input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, negating errors caused by the on-resistance of the driver switches is possible.

Two ADC-control registers control the ADC. Several modes of operation are possible, depending on the bits set in the control registers. Programming of channel selection, scan operation, preprocessing, resolution, and conversion rate is through these registers. The following sections outline these modes for each type of analog input. The appropriate result register stores the conversion results.

7.3.3.1 Data Format

The TSC2013-Q1 output data are in straight binary format as shown in Figure 21. Figure 21 shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



(1) Reference voltage at converter: +REF – (–REF). See Figure 20.

(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 20.

Figure 21. Ideal Input Voltages and Output Codes

7.3.3.2 Reference

The TSC2013-Q1 device uses an external voltage reference applied to the SNSVDD/VREF pin. Using the SNSVDD/VREF pin as the reference voltage is possible because the upper reference voltage range is the same as the supply-voltage range.

7.3.3.3 Variable Resolution

The TSC2013-Q1 device provides either 10-bit or 12-bit resolution for the ADC. Lower resolution is often practical for measuring slow-changing signals such as touch pressure. Performing the conversions at lower resolution reduces the amount of time required for the ADC to complete the conversion process which also lowers power consumption.

7.3.3.4 Conversion Clock and Conversion Time

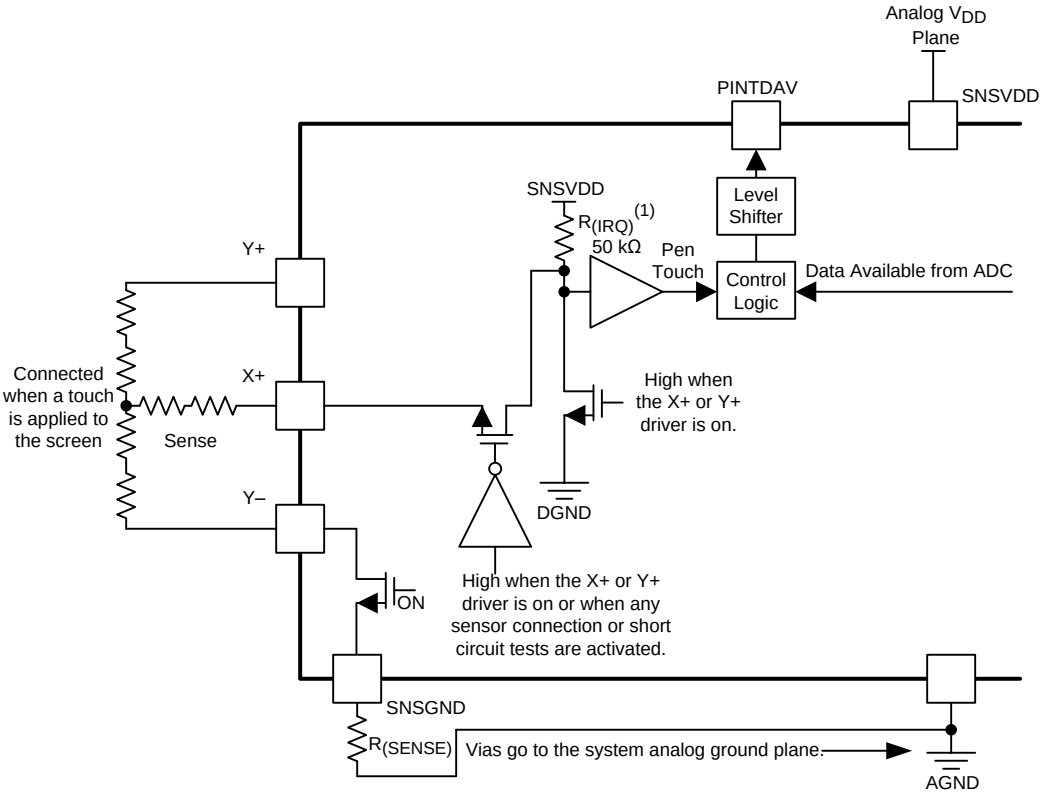
The TSC2013-Q1 device contains an internal clock (oscillator) that drives the internal state machines that perform the many functions of the part. This clock is divided down to provide a conversion clock for the ADC. The setting for the division ratio of this clock is in the ADC control register (see Configuration Register 0 (address = 0) [reset = 4000h for read; 0000h for write]). The ability to change the conversion clock rate allows the user to select the optimal values for resolution, speed, and power dissipation. Using the 4-MHz (oscillator) clock directly as the ADC clock (when the CL[1:0] bit is set to 0) limits the ADC resolution to 10 bits. Using higher resolutions at this speed does not result in more accurate conversions. Twelve-bit resolution requires that the CL bits 1 and 0 are set to 0 and 1, or 1 and 0 (respectively).

Feature Description (continued)

Regardless of the conversion clock speed, the internal clock runs nominally at 3.8 MHz at a 3-V supply (SNSVDD) and slows down to 3.6 MHz at a 1.6-V supply. The conversion time of the TSC2013-Q1 device depends on several functions. The conversion clock speed plays an important role in the time required for a conversion to complete. However, proper sampling of the signal requires a certain number of internal clock cycles. Moreover, additional times (such as the panel voltage-stabilization time), can add significantly to the time it takes to perform a conversion. Conversion time can vary depending on the mode of use of TSC2013-Q1 device. This data sheet makes use of internal and conversion clock cycles throughout as the units used to describe the amount of time that many functions take. Take these times into account when considering the total system design.

7.3.3.5 Touch Detect

The $\overline{\text{PINTDAV}}$ pin can be programmed to generate an interrupt to the host. Figure 22 shows an example for a typical screen-touch situation. While in the power-down mode, the Y– driver is on and connects to GND. The internal pen-touch signal depends on whether or not the X+ input is low. A touch on the panel pulls the X+ input to ground through the touch screen and sets the internal pen-touch output to low because of the detection on the current path through the panel to ground, which initiates an interrupt to the processor. During the measurement cycles for X and Y-position, the device disconnects the X+ input, which eliminates any leakage current from the pullup resistor flowing through the touch screen, thus causing no errors.



(1) Untrimmed resistor; see the typical value in the table.

Figure 22. Example of a Pen-Touch Induced Interrupt via the $\overline{\text{PINTDAV}}$ Pin

Feature Description (continued)

In modes where the TSC2013-Q1 device must detect whether or not a touch remains on the screen (for example, when doing a pen-touch-initiated X, Y, and Z conversion), the TSC2013-Q1 device must reset the drivers to connect the $R_{(IRQ)}$ resistor again. Because of the high value of this pullup resistor, any capacitance on the touch screen inputs causes a long delay time, and may prevent the detection from occurring correctly. To prevent this possible delay, the TSC2013-Q1 device has a circuit that allows *prechargingd* any screen capacitance, so that the pullup resistor must not be the only source for the charging current. The setting for the time allowed for this precharge, as well as the time needed to sense if the screen touch remains, is in the configuration register.

This configuration underscores the need to use the minimum possible capacitor values on the touch-screen inputs. Capacitors can be used to reduce noise, but capacitors with too large a value increase the required precharge and sense times, as well as the panel voltage-stabilization time.

7.3.3.6 Preprocessing

The TSC2013-Q1 device offers an array of powerful preprocessing operations that reduce unnecessary traffic on the bus and reduce the host processor loading. This reduction is especially critical for the serial interface because of the slow bus speed and the high CPU bandwidth required for I^2C communication.

All data-acquisition tasks are looking for specific data that meet certain criteria. Many of these tasks fall into a predefined range, while other tasks may be looking for a value in a noisy environment. If the host processor is to retrieve all these data for processing, the limited bus bandwidth quickly saturates, along with the host processor processing capability. In any case, reserving the host processor for more critical tasks rather than routine work is always necessary.

The preprocessing unit consists of two main functions which result in the combined MAV (median and averaging-value) filter: the median value filter (MVF) and the averaging-value filter (AVF).

7.3.3.6.1 Preprocessing—Median Value Filter and Averaging Value Filter

The first preprocessing function, a combined MAV filter, can operate independently as a median value filter (MVF), an averaging value filter (AVF), and a combined filter (MAV filter).

If the acquired signal source is noisy because of the digital switching circuit, evaluating the data without noise may be necessary. In this case, the median value filter (MVF) operation helps to discard noise. The first action is sorting the array of *N* converted results. The return value is either the middle (median value) of an array of *M* converted results, or the average value of a window size of *W* of converted results:

N = the total number of converted results used by the MAV filter

M = the median value filter size programmed

W = the averaging window size programmed

If M is equal to 1, then N is equal to W. A special case is W equal to 1, which indicates a bypassed MAV filter. Otherwise, if W is greater than 1, averaging is the only function performed on these converted results. In either case, the return value is the averaged value of window size W of converted results.

If M is greater than 1 and W is equal to 1, then N is equal to M, meaning the only operating filter is the median value filter. The return value is the middle position converted result from the array of M converted results.

If M is greater than 1 and W is greater than 1, then N is equal to M. In this case, W is less than M. The return value is the averaged value of middle portion W of converted results out of the array of M converted results. Because the value of W is an odd number in this case, the calculation of the averaging value counts the middle-position converted result twice (averaging a total of W + 1 converted results).

Feature Description (continued)

Table 1. Median Value Filter-Size Selection

M1	M0	MEDIAN VALUE FILTER M =	POSSIBLE AVERAGING WINDOW SIZE W =
0	0	1	1, 4, 8, 16
0	1	3	1
1	0	7	1, 3
1	1	15	1, 3, 7

Table 2. Averaging Value Filter-Size Selection

W1	W0	AVERAGING VALUE FILTER SIZE SELECTION W =	
		M = 1 (Averaging Only)	M > 1
0	0	1	1
0	1	4	3
1	0	8	7
1	1	16	Reserved

The device uses the default MVF setting (median value filter with averaging bypassed) for any invalid MAV filter configuration. For example, if M1, M0, W1, and W0 equals 1, 0, 1, and 0 (respectively), the MAV filter will perform as if it were configured for 1, 0, 0, 0, median filter only with filter size of 7, and no averaging. The only exception is when M is greater than 1 and when W1 and W0 equal 1. Avoid using this reserved setting.

Table 3. Combined MAV Filter Setting

M	W	INTERPRETATION	N =	OUTPUT
= 1	= 1	Bypass both MAF and AVF	W	The converted result
= 1	> 1	Bypass MVF only	W	Average of W converted results
> 1	= 1	Bypass AVF only	M	Median of M converted results
> 1	> 1	M > W	M	Average of middle W of M converted results with the median counted twice

The MAV filter is available for all analog inputs including the touch-screen inputs and the AUX measurement.

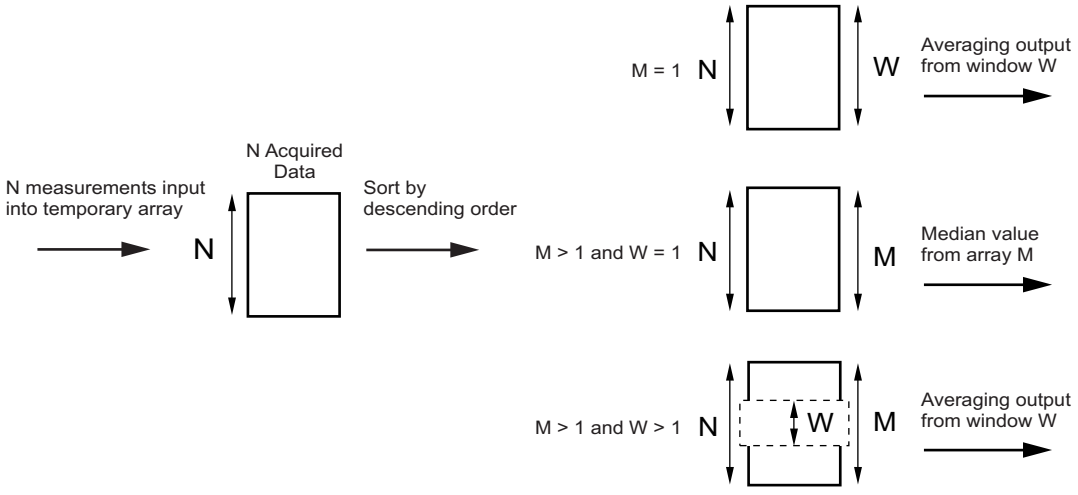


Figure 23. MAV Filter Operation

7.4 Device Functional Modes

7.4.1 Conversion Controlled by TSC2013-Q1 and Initiated by TSC2013-Q1 (TSMode 1)

In TSMode 1, before a pen-touch detection is possible, the TSC2013-Q1 device must be programmed with the PSM bit set to 1 and one of two scan modes:

1. X-triplet, Y-triplet, Z-scan (converter function select bits C[3:0] = control byte 1 D[6:3] = 0000)
2. IX-IY scan (converter function select bits C[3:0] = control byte 1 D[6:3] = 0001).

See Table 7 for more information on the converter function-select bits.

On touching the touch panel, the internal pen-touch signal activates, lowering the $\overline{\text{PINTDAV}}$ output if programmed as $\overline{\text{PENIRQ}}$. The TSC2013-Q1 device then executes the preprogrammed scan function without a host intervention.

7.4.1.1 IX-IY Scan

The TSC2013-Q1 device starts up the internal clock. The device then turns on the Y-drivers, and after a programmed panel voltage-stabilization time, the device powers up the ADC and converts the IY coordinate. With preprocessing selected, several conversions can occur. When data preprocessing is complete, a temporary register stores the IY coordinate result.

If the screen touch remains at this time, the device enables the X-drivers and the process repeats but measures the IX coordinate instead, storing the result in a temporary register.

Figure 24 shows a flowchart for this process. The time required to go through this process depends on the selected resolution, internal conversion clock rate, panel voltage-stabilization time, precharge and sense times, and the selection status of preprocessing. Use Equation 3 to calculate the time required to achieve a complete X and Y coordinate (sample set) reading.

$$t_{(COORDINATE)} = \frac{t_{(OH1)}}{f_{(OSC)}} + 2 \times \left(t_{(PVS)} + t_{(PRE)} + t_{(SNS)} + \frac{t_{d(OH1)}}{f_{(OSC)}} \right) + 2 \times \left(N \times \left[(B+2) \times \frac{f_{(OSC)}}{f_{(ADC)}} + t_{c(OH)} \right] \times \left[\frac{1}{f_{(OSC)}} \right] + \left[\frac{t_{(PPRO)}}{f_{(OSC)}} \right] \right) \quad (3)$$

where

- $t_{(COORDINATE)}$ = time to complete IX and IY coordinate reading
- N = number of measurements for MAV filter input, as given in Table 3 as *N* (For no MAV: M1 = M0 = W1 = W0 = 0)
- $t_{(PVS)}$ = panel voltage stabilization time, as listed in Table 10
- $t_{(PRE)}$ = precharge time, as listed in Table 10
- $t_{(SNS)}$ = sense time, as listed in Table 10
- B = number of bits of resolution
- $f_{(OSC)}$ = TSC onboard OSC clock frequency. See the *Electrical Characteristics* section for supply frequency (SNSVDD)
- $f_{(ADC)}$ = ADC clock frequency, as listed in Table 10
- $t_{(OH1)}$ = overhead time number 1 = 2.5 internal clock cycles
- $t_{d(OH1)}$ = total overhead time for $t_{(PVS)}$, $t_{(PRE)}$, and $t_{(SNS)}$ = 10 internal clock cycles
- $t_{c(OH)}$ = total overhead time for A-to-D conversion = 3 internal clock cycles
- $t_{(PPRO)}$ = preprocessor preprocessing time as listed in Table 4

Table 4. Preprocessing Delay

M =	W =	$t_{(PPRO)}$ =	
		FOR B = 12 BIT	FOR B = 10 BIT
1	1, 4, 8, 16	2	2
3, 7	1	28	24
7	3	31	27
15	1	31	29
15	3	34	32
15	7	38	36

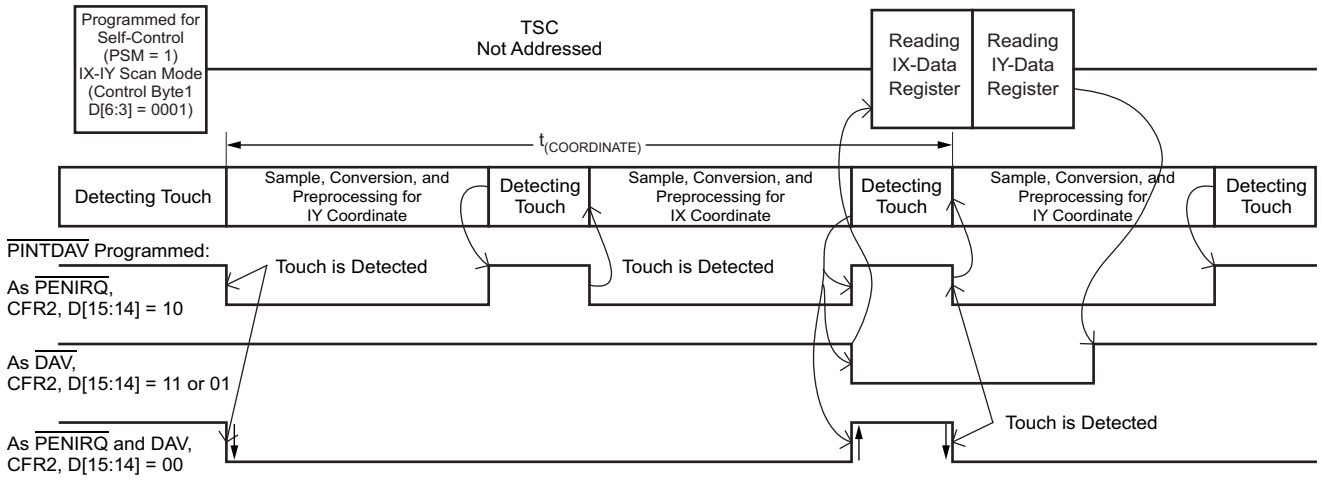


Figure 24. Example of an IX and IY Touch-Screen Scan Using TSMode 1

7.4.1.2 X-Triplet, Y-Triplet, Z-Scan

The TSC2013-Q1 device starts up the internal clock. The device then turns on the Y-drivers, and after a programmed panel voltage-stabilization time, powers up the ADC and converts the Y-triplet. With preprocessing selected, several conversions can occur. When data preprocessing is complete, temporary registers store the Y-triplet results.

If the screen touch remains at this time, the device enables the X-drivers and the process repeats but measures the X-triplet instead, storing the result in temporary registers.

The process continues in the same way, but measures the Z1 and Z2 values instead, storing the results in temporary registers. When the complete sample set of data (X1, X2, IX, Y1, Y2, IY, Z1, and Z2) are available, the device loads the data in the X1, X2, IX, Y1, Y2, IY, Z1, and Z2 registers. Figure 25 shows this process. This process time depends on the previously described settings. Use Equation 4 to calculate the time for a complete X1, X2, IX, Y1, Y2, IY, Z1, and Z2 coordinate reading.

$$t_{(COORDINATE)} = \frac{t_{(OH2)}}{f_{(OSC)}} + 3 \times \left(t_{(PVS)} + t_{(PRE)} + t_{(SNS)} + \frac{t_{d(OH1)}}{f_{(OSC)}} \right) + 8 \times \left(N \times \left[(B+2) \times \frac{f_{(OSC)}}{f_{(ADC)}} + t_{c(OH)} \right] \times \left[\frac{1}{f_{(OSC)}} \right] + \left[\frac{t_{(PPRO)}}{f_{(OSC)}} \right] \right)$$

where

- $t_{(OH2)}$ = overhead time number 2 = 3.5 internal clock cycles (4)

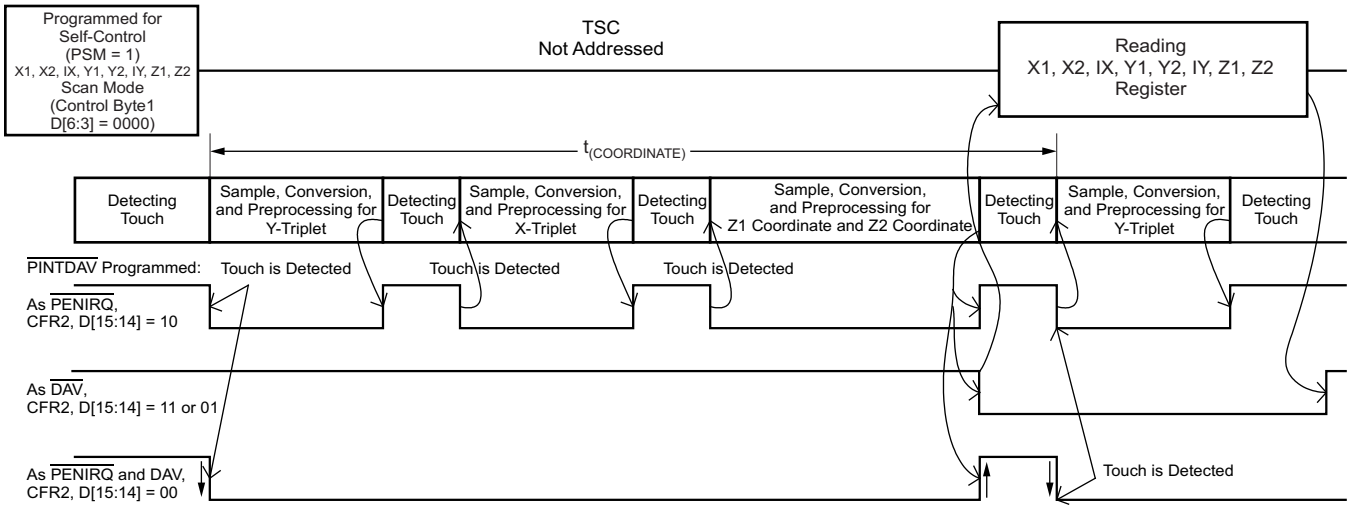


Figure 25. Example of an X-Triplet and Y-Triplet Coordinate Touch-Screen Scan Using TSMode 1

7.4.2 Conversion Controlled by TSC2013-Q1 and Initiated by Host (TSMode 2)

In TSMode 2, the TSC2013-Q1 device detects when a touch of the touch panel occurs and causes the internal pen-touch signal to activate, which lowers the $\overline{\text{PINTDAV}}$ output if programmed as $\overline{\text{PENIRQ}}$. The host recognizes the interrupt request and then writes to the ADC control register to select one of the following two Touch-Screen Scan functions:

1. X-triplet, Y-triplet, Z-scan (converter function select bits C[3:0] = control byte 1 D[6:3] = 0000); or
2. IX-IY scan (converter function select bits C[3:0] = control byte 1 D[6:3] = 0001).

See Table 7 for more information on the converter function-select bits.

The conversion process then proceeds as shown in Figure 26. See the *IX-IY Scan* and *X-Triplet, Y-Triplet, Z-Scan* sections for additional details.

The main difference between this mode and the previous mode is that the host, not the TSC2013-Q1 device, decides when the touch-screen scan begins.

Use **Equation 3** to calculate the time required to convert both IX and IY under host control (not including the time required to send the command over the I^2C bus):

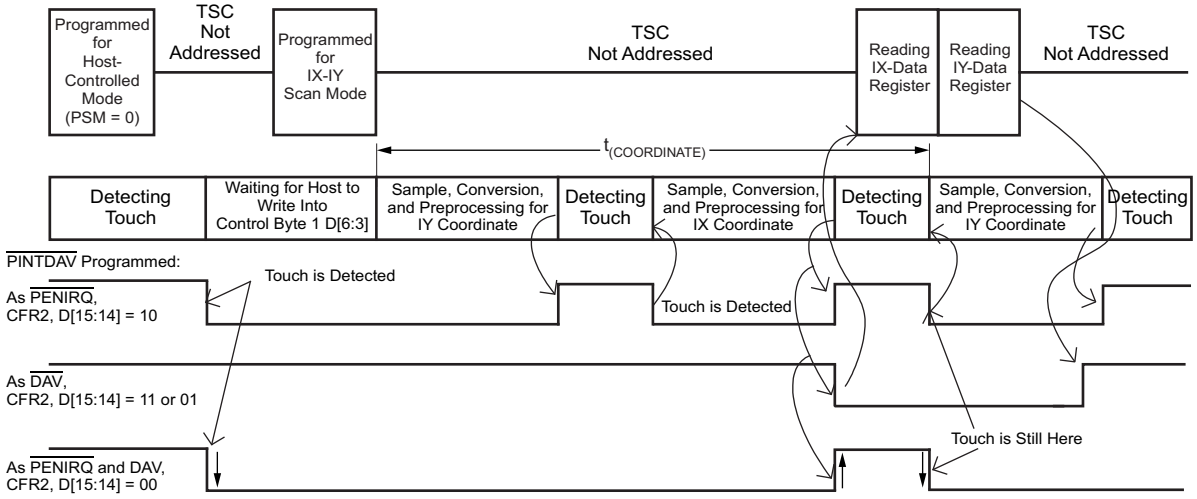


Figure 26. Example of an IX and IY Touch-Screen Scan Using TSMode 2

7.4.3 Conversion Controlled by Host (TSMode 3)

In TSMode 3, the TSC2013-Q1 device detects a touch of the touch panel and causes the internal pen-touch signal to be active, which lowers the $\overline{\text{PINTDAV}}$ output if programmed as $\overline{\text{PENIRQ}}$. The host recognizes the interrupt request. Instead of starting a sequence in the TSC2013-Q1 device, which then reads each coordinate in turn, the host must now control all aspects of the conversion. Generally, on receiving the interrupt request, the host turns on the X drivers.

NOTE

With the drivers turned off, the device detects this condition and turns the driver on before the scan starts. This situation is why the event of *turn on drivers* is shown as optional in Figure 27 and Figure 29.

After waiting for the settling time, the host then addresses the TSC2013-Q1 device again, this time requesting an X-coordinate conversion.

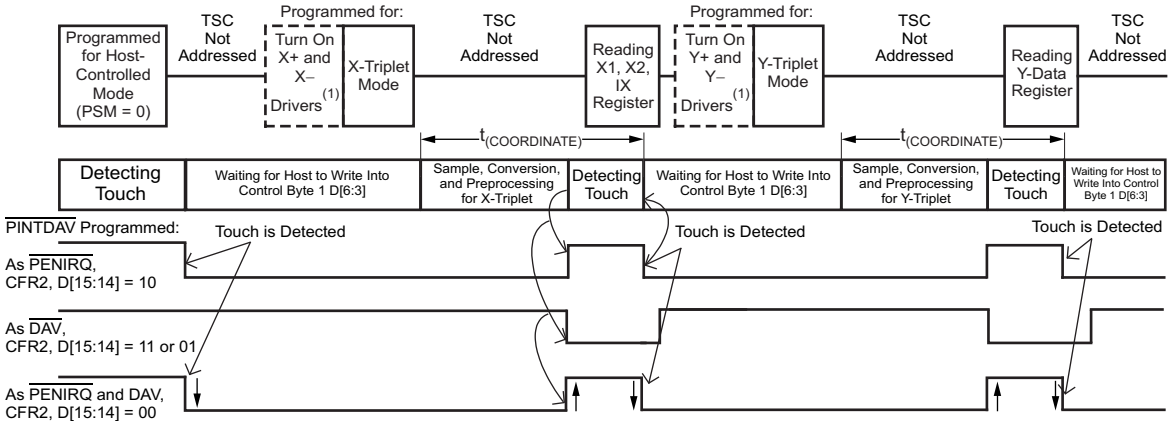
The process then repeats for the Y and Z coordinates. Figure 27 and Figure 29 show this process. Figure 27 shows two consecutive scans on IX and IY. Figure 29 shows a single Z scan.

Use Equation 5 to calculate the time required to convert any single X-triplet or Y-triplet under host control (not including the time required to send the command over the I^2C bus):

$$t_{(COORDINATE)} = \frac{t_{(OH1)}}{f_{(OSC)}} + \left(t_{(PRE)} + t_{(SNS)} + \frac{t_{d(OH2)}}{f_{(OSC)}} \right) + 3N \times \left(\left[(B+2) \times \frac{f_{(OSC)}}{f_{(ADC)}} + t_{c(OH)} \right] \times \left[\frac{1}{f_{(OSC)}} \right] + \left[\frac{t_{(PPRO)}}{f_{(OSC)}} \right] \right) \quad (5)$$

where

- $t_{d(OH2)}$ = total overhead time for $t_{(PRE)}$ and $t_{(SNS)}$ = 6 internal clock cycles



(1) Optional. If not turned on, it will be turned on by the scan mode, when detected.

Figure 27. Example of X-Triplet and Y-Triplet Touch-Screen Scan (Without Panel Stabilization Time) Using TSMode 3

Use Equation 6 to calculate the time required to convert any single X-triplet or Y-triplet under host control (not including the time required to send the command over the I^2C bus):

$$t_{(COORDINATE)} = \frac{t_{(OH1)}}{f_{(OSC)}} + \left(t_{(PVS)} + t_{(PRE)} + t_{(SNS)} + \frac{t_{d(OH2)}}{f_{(OSC)}} \right) + 3N \times \left(\left[(B+2) \times \frac{f_{(OSC)}}{f_{(ADC)}} + t_{c(OH)} \right] \times \left[\frac{1}{f_{(OSC)}} \right] + \left[\frac{t_{(PPRO)}}{f_{(OSC)}} \right] \right) \quad (6)$$

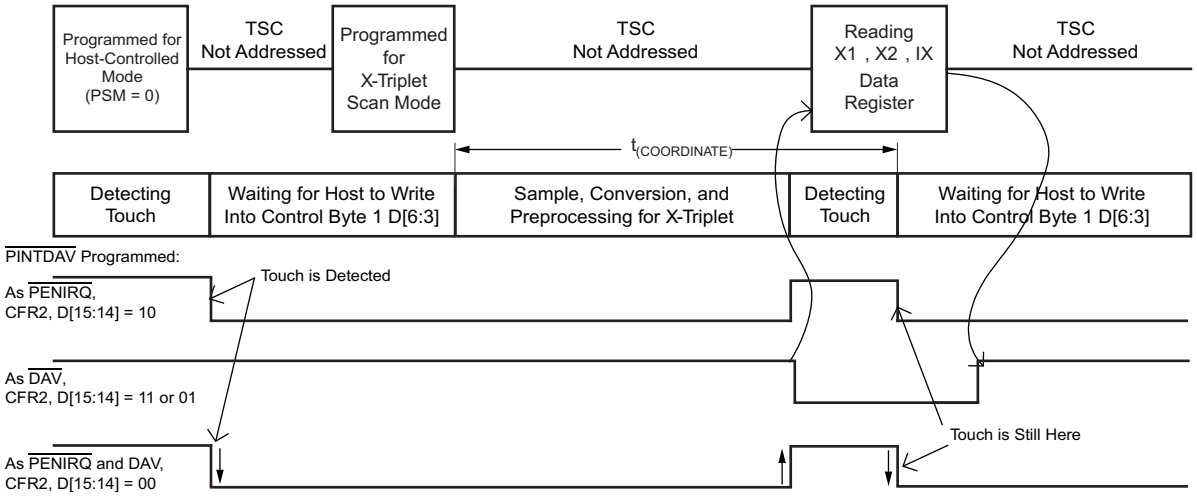
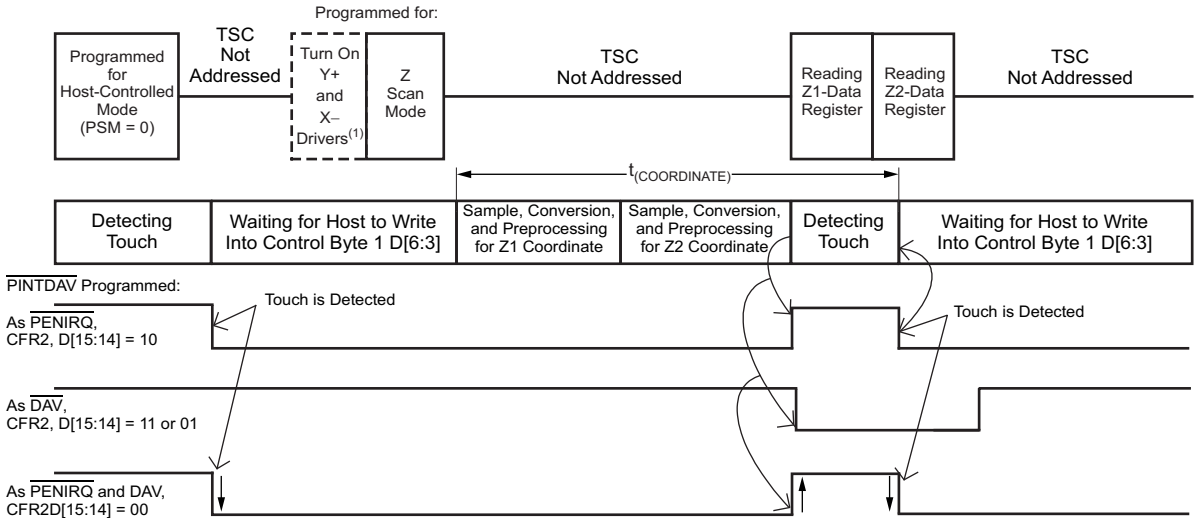


Figure 28. Example of a Single X-Triplet Touch-Screen Scan (With Panel Stabilization Time) Using TSMode 3

Use Equation 7 to calculate the time required to convert any Z1 and Z2 coordinate under host control (not including the time required to send the command over the I²C bus):

$$t_{(COORDINATE)} = \frac{t_{(OH2)}}{f_{(OSC)}} + \left(t_{(PRE)} + t_{(SNS)} + \frac{t_{d(OH2)}}{f_{(OSC)}} \right) + N \times \left(\left[(B+2) \times \frac{f_{(OSC)}}{f_{(ADC)}} + t_{c(OH)} \right] \times \left[\frac{1}{f_{(OSC)}} \right] + \left[\frac{t_{(PPRO)}}{f_{(OSC)}} \right] \right) \quad (7)$$



(1) Optional. If not turned on, it will be turned on by the scan mode, when detected.

Figure 29. Example of Z1 and Z2 Coordinate Touch-Screen Scan (Without Panel Stabilization Time) Using TSMode 3

If the drivers do not turn on prior to programming the touch-screen scan mode, include the panel stabilization time. In this case, use Equation 8 to calculate the time required to convert any single X or Y under host control (not including the time required to send the command over the I²C bus):

$$t_{(COORDINATE)} = \frac{t_{(OH2)}}{f_{(OSC)}} + \left(t_{(PVS)} + t_{(PRE)} + t_{(SNS)} + \frac{t_{d(OH2)}}{f_{(OSC)}} \right) + N \times \left(\left[(B+2) \times \frac{f_{(OSC)}}{f_{(ADC)}} + t_{c(OH)} \right] \times \left[\frac{1}{f_{(OSC)}} \right] + \left[\frac{t_{(PPRO)}}{f_{(OSC)}} \right] \right) \quad (8)$$

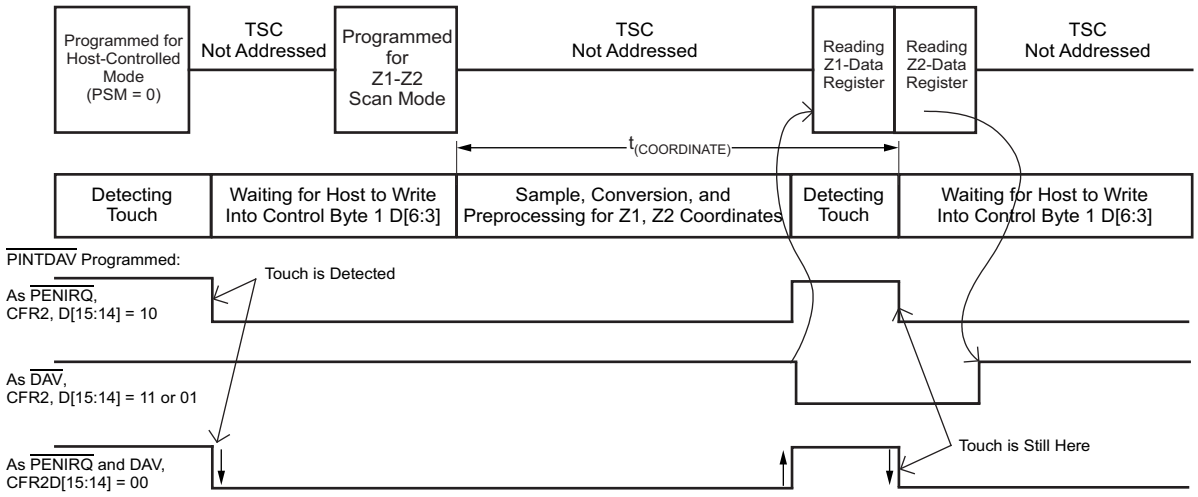


Figure 30. Example of a Z1 and Z2 Coordinate Touch-Screen Scan (With Panel Stabilization Time) Using TSMode 3

7.5 Programming

7.5.1 I²C Interface

The TSC2013-Q1 device supports the I²C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus has the definition of a transmitter, and a device receiving data that of a receiver. The device that controls the message is a *master*. Devices controlled by the master are *slaves*. A master device that generates the serial clock (SCL), controls bus access, and generates the START and STOP conditions must control the bus The TSC2013-Q1 device operates as a slave on the I²C bus. Connections to the bus are through the open-drain I/O lines, SDA and SCL.

The following bus protocol has been defined (see Figure 31):

- A device can initiate data transfer only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, definitions for the following bus conditions follow:

Bus Not Busy Both data and clock lines remain high.

Start Data Transfer A change in the state of the data line, from high to low, while the clock is high, defines a start condition.

Stop Data Transfer A change in the state of the data line, from low to high, while the clock line is high, defines the stop condition.

Data Valid The state of the data line represents valid data, when, after a start condition, the data line is stable for the duration of the high period of the clock signal. One clock pulse occurs per bit of data.

Each data transfer begins with a start condition and terminates with a stop condition. The number of data bytes transferred between start and stop conditions, which the master device determines, is not limited. The information transfers byte-wise, and the receiver acknowledges each byte with a ninth bit.

The I²C bus specifications define a standard mode (100-kHz clock rate), a fast mode (400-kHz clock rate), and a high-speed mode (3.4-MHz clock rate). The TSC2013-Q1 device works in all three modes.

Acknowledge Each receiving device, when addressed, must generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse for association with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Of course, the timing must take into account setup and hold times. A master must signal an end-of-data to the slave by not generating an acknowledge bit on the last byte that clocks out of the slave. In this case, the slave must leave the data line high to enable the master to generate the stop condition.

Figure 31 shows the data-transfer process on the I²C bus. Depending on the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. Data transfer from a master transmitter to a slave receiver.

   The first byte transmitted by the master is the slave address. A number of data bytes occurs next. The slave returns an acknowledge bit after the slave address and each received byte.

2. Data transfer from a slave transmitter to a master receiver.

   The master transmits the first byte, the slave address. The slave then returns an acknowledge bit. Next, the slave transmits a number of data bytes to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, the master returns a not-acknowledge.

The master device generates all of the serial clock pulses and the start and stop conditions. A transfer ends with a stop condition or a repeated start condition. Because a repeated start condition is also the beginning of the next serial transfer, the bus is not released.

Programming (continued)

The TSC2013-Q1 device can operate in the following two modes:

1. Slave receiver mode

   Reception of serial data and clock is through SDA and SCL. After the reception of each byte, the receiver transmits an acknowledge bit. Start and stop conditions designate the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit.

2. Slave transmitter mode

   Reception and handling of the first byte (the slave address) is the same as in the slave receiver mode. However, in this mode the direction bit indicates a reversal of the transfer direction. Serial data transmission on SDA by the TSC2013-Q1 device occurs during input of the serial clock on SCL. Start and stop conditions designate the beginning and end of a serial transfer.

7.5.1.1 I^2C Fast or Standard Mode (F-S Mode)

In I^2C fast or standard (F-S) mode, serial data transfer must meet the timing shown in the timing requirement tables in the *Specifications* section.

In the serial transfer format of F-S mode, the master signals the beginning of a transmission to a slave with a start condition (S), which is a high-to-low transition on the SDA input while SCL is high. When the master has finished communicating with the slave, the master issues a stop condition (P), which is a low-to-high transition on SDA while SCL is high, as shown in Figure 31. The bus is free for another transmission after the occurrence of a stop. Figure 31 shows the complete F-S mode transfer on the I^2C, two-wire serial interface. Transmission of the address byte, control byte, and data byte is between the start and stop conditions. The SDA state can only change while SCL is low, except for the start and stop conditions. Data transmission is in 8-bit words. Nine clock cycles are necessary to transfer the data into or out of the device (8-bit word plus acknowledge bit).

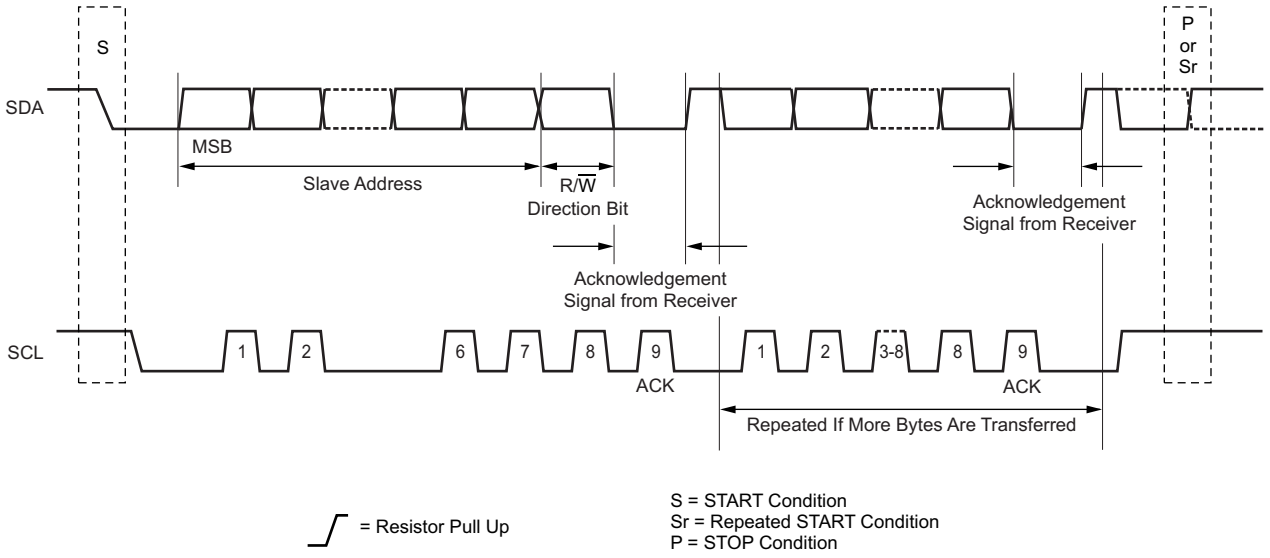


Figure 31. Complete Fast or Standard-Mode Transfer

Programming (continued)

7.5.1.2 I²C High-Speed Mode (Hs Mode)

Serial data transfer format in high-speed (Hs) mode meets the fast or standard (F-S) mode I²C bus specification. Hs mode can only commence after the following conditions (all of which are in F-S mode) exist:

1. Start condition (S)
2. 8-bit master code (0000 1xxx)
3. Not-acknowledge bit (N)

Figure 32 shows this sequence in more detail. Hs-mode master codes are reserved 8-bit codes used only for triggering Hs mode. Do not use these codes for slave addressing or any other purpose. The master code indicates to other devices that an Hs-mode transfer is about to begin and the connected devices must meet the Hs mode specification. Because no device can acknowledge the master code, a not-acknowledge bit (N) follows the master code.

After the not-acknowledge bit (N) and SCL achieve a high level, the master switches to Hs-mode and enables (at time $t_{(H)}$; shown in Figure 32) the current-source pullup circuit for SCL. Because other devices can delay the serial transfer before $t_{(H)}$ by stretching the LOW period of SCL, the master enables the current-source pullup circuit when all devices have released SCL and SCL has reached a high level, thus speeding up the last part of the rise time of the SCL.

The master then sends a repeated start condition (Sr) followed by a 7-bit slave address with an R/$\overline{W}$ bit address, and receives an acknowledge bit (A) from the selected slave. After a repeated start (Sr) condition and after each acknowledge bit (A) or not-acknowledge bit (N), the master disables the current-source pullup circuit. This disabling enables other devices to delay the serial transfer by stretching the low period of SCL. The master re-enables the current-source pullup circuit again when all devices have released, and SCL reaches a high level, which speeds up the last part of the SCL signal rise time.

Data transfer continues in Hs mode after the next repeated start (Sr), and only switches back to F-S mode after a stop condition (P). To reduce the overhead of the master code, the master can link to a number of Hs mode transfers, separated by repeated start conditions (Sr).

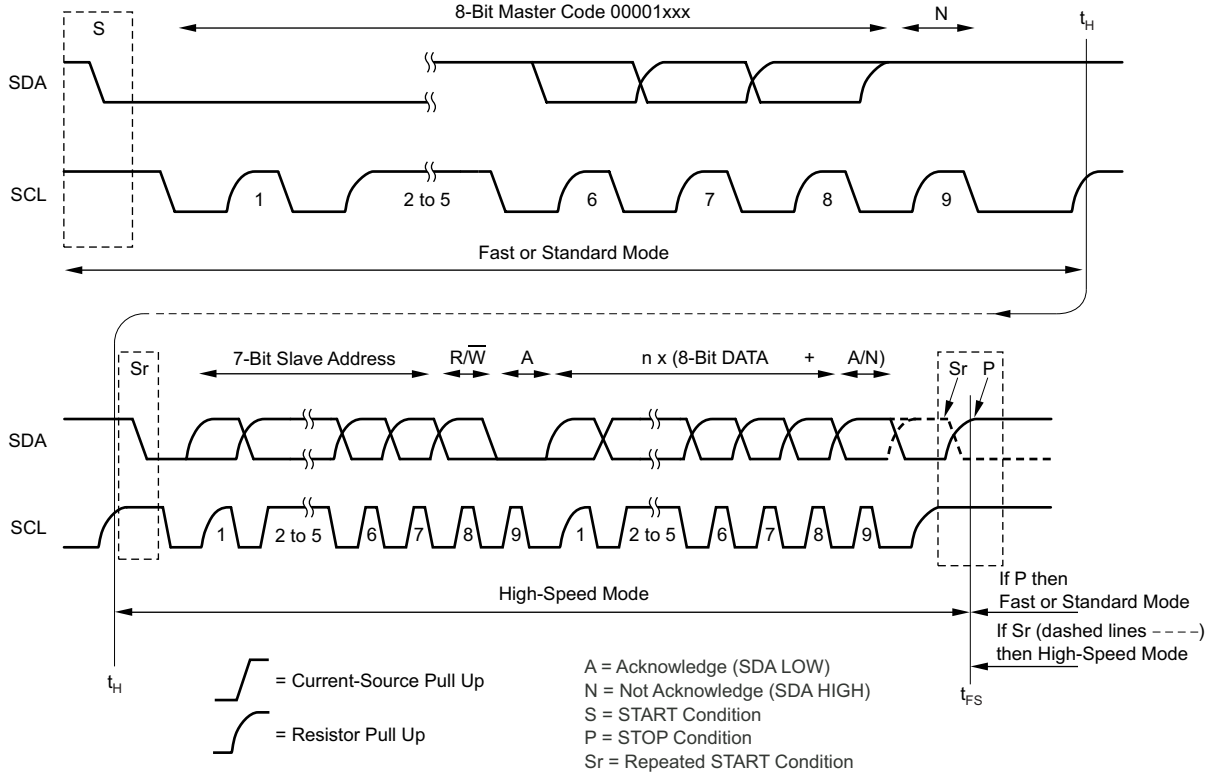


Figure 32. Complete High-Speed Mode Transfer

Programming (continued)

7.5.2 Digital Interface

7.5.2.1 Address Byte

The TSC2013-Q1 device has a 7-bit slave address word. The factory presets the first five bits (MSBs) of the slave address to comply with the I^2C standard for ADCs; the setting is always 1 0010. The logic state of the address input pins (AD1 through AD0) determines the two LSBs of the device address to activate communication. Therefore, one bus can accommodate a maximum of four devices with the same preset code at one time.

The device only reads the AD1 through AD0 address inputs during a power-up of the device, and the pin connections should be to a digital supply (I/OVDD) or digital ground (DGND). The TSC2013-Q1 latches the slave address on the falling edge of SCL after reception of the R/$\overline{W}$ bit by the slave.

The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. Setting the bit to 1 selects a read operation. Setting the bit to 0 selects a write operation. Following the start condition, the TSC2013-Q1 device monitors the SDA bus, checking the transmitted device-type identifier. On receiving the 1 0010 code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Table 5. I^2C Slave Address Byte

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	0	0	1	0	AD1	AD0	R/$\overline{W}$

R/$\overline{W}$ (D0)

1: I^2C master read from TSC (I^2C read addressing).

0: I^2C master write to TSC (I^2C write addressing).

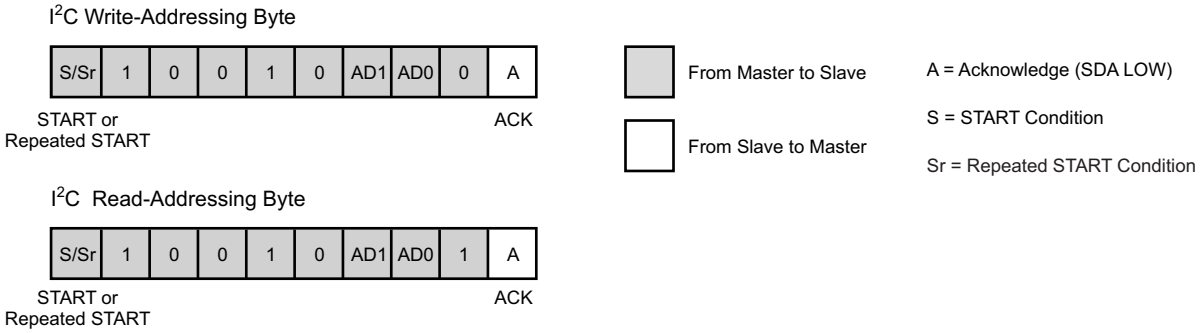


Figure 33. I^2C Bus Addressing (Slave-Address Byte Format)

7.5.3 Control Byte

Table 6. Control Byte Format: Start a Conversion and Mode Setting, D7 = 1

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1 (Control Byte 1)	C3	C2	C1	C0	RM	SWRST	STS

Control Byte ID (D7)

1: Control Byte 1 (start conversion and channel select and conversion-related configuration).

0: Control Byte 0 (read/write data registers and non-conversion-related controls).

C[3:0] (D6:D3)

Converter function select bits

These bits select the input for conversion, and the converter function to be executed. Table 7 lists the possible converter functions.

RM (D2)

Resolution select

If RM = 1, the conversion-result resolution is 12-bit; otherwise, the resolution is 10-bit. This bit is the same RM bit shown in CFR0.

0: 10-bit

1: 12-bit

SWRST (D1)

Software reset. This bit is self-clearing.

1: Reset all register values to default

STS (D0)

Stop bit for all converter functions. This bit is self-clearing.

On writing a 1 to this register, this bit aborts the converter function currently running in the TSC2013-Q1. An automatic write of 0 to this register occurs when the abort has completed. Setting this bit to 1 can only stop converter functions; it does not reset any data, status, or configuration registers. This bit is the same STS bit shown in CFR0, but reading can only be through the CFR0 register.

Write 0: Normal operation

Write 1: Stop converter functions and power down

Table 7. Converter Function Select

C3	C2	C1	C0	FUNCTION
0	0	0	0	Touch-Screen Scan function: X triplet, Y triplet, Z1, and Z2 coordinates converted and the results returned to X1, X2, IX, Y1, Y2, IY, Z1, and Z2 data registers. Scan continues until either lifting of the pen or sending of a stop bit.
0	0	0	1	Touch-Screen Scan function: IX and IY coordinates converted and the results returned to IX and IY data registers. Scan continues until either lifting of the pen or sending of a stop bit.
0	0	1	0	Touch screen function: X triplet converted and the results returned to X1, X2, IX data register.
0	0	1	1	Touch screen function: Y triplet converted and the results returned to Y1, Y2, IY data register.
0	1	0	0	Touch screen function: Z1 and Z2 coordinates converted and the results returned to Z1 and Z2 data registers.
0	1	0	1	Auxiliary input converted and the results returned to the AUX data register.
0	1	1	0	Touch screen function: IX converted and result returned to IX data register.
0	1	1	1	Touch screen function: IY converted and result returned to IY data register.
1	0	0	0	Auxiliary input conversion occurs ***continuously*** and the results returned to the AUX data register.
1	0	0	1	RESERVED
1	0	1	0	RESERVED
1	0	1	1	RESERVED (1)
1	1	0	0	RESERVED
1	1	0	1	X+, X– drivers activated
1	1	1	0	Y+, Y– drivers activated
1	1	1	1	Y+, X– drivers activated

(1) Any condition caused by this command can be cleared by setting the STS bit to 1.

Table 8. Control Byte Format: Start a Conversion and Mode Setting D7 = 0

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
0 (Control Byte 0)	A3	A2	A1	A0	Reserved (Write 0)	PND0	R/$\overline{W}$

Control byte ID (D7)

1: Control byte 1—start conversion, channel select, and conversion-related configuration

0: Control byte 0—read/write data registers and non-conversion-related controls

A[3:0] (D6:D3) Register address bits as detailed in Table 9

RESERVED (D2) Set a 0 in this bit for normal operation

PND0 (D1)

Power-not-down control

1: ADC biasing circuitry is always on between conversions but shuts down after the converter function stops

0: ADC biasing circuitry shuts down either between conversions or after the converter function stops. Example power savings for the following condition is approximately 5%: AUX conversion, continuous mode, median filter = 15, averaging filter = 7, $f_{(ADC)}$ = 2 MHz.

R/$\overline{W}$ (D0)

TSC internal-register data-flow control

1: Set the starting address of the TSC internal registers for a register read (see Figure 34)

0: Write to TSC internal registers

7.5.3.1 Touch-Screen Scan Function for XYZ or XY

These scan functions (C3–C0 = 0000 or 0001) can collaborate with the PSM bit that defines the control mode of converter functions. With the PSM bit set to 1, TI recommends issuing these scan-function select commands before detection of a pen touch in order to allow the TSC2013-Q1 device to initiate and control the scan processes immediately after detection of the screen touched. Without issuing these functions before detection of a pen touch, the TSC2013-Q1 waits for the host to write these functions before starting a scan process. If PSM stays as 1 after a TSC-initiated scan function is complete, the host is not required to write these function-select bits again for each of the following pen touches after the detected touch. In the host-controlled converter function mode (PSM = 0), the host must send these functions select bits repeatedly for each scan function after a detected pen touch.

NOTE

The update of the data registers may occur while a host reading is in progress. Using the sequential read cycle (see Figure 35) prevents the TSC from updating registers while a host reading is in progress. To ensure a correct reading of the XYZ or XY coordinates, use the sequential read cycle to read the coordinates after the scan.

Table 9. Internal Register Map

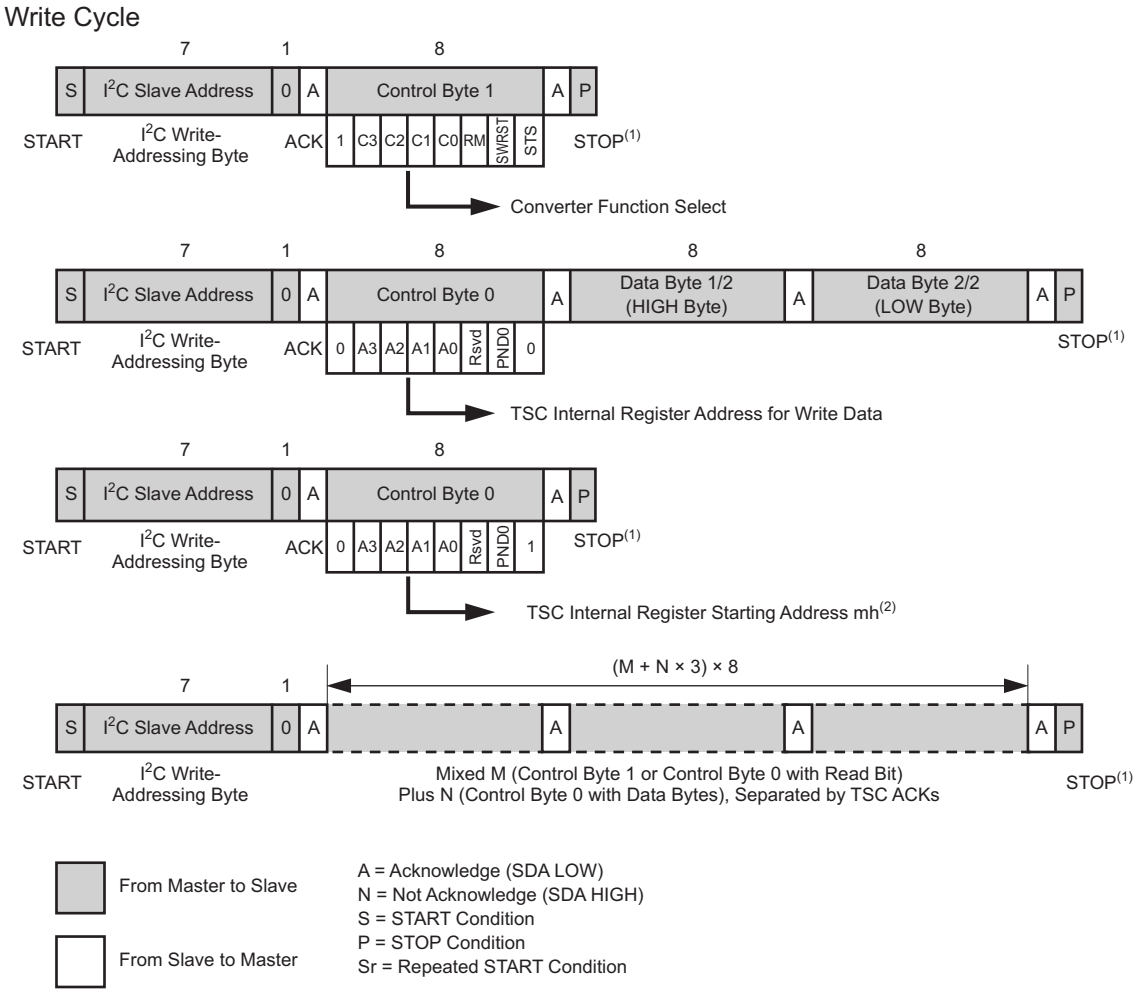
REGISTER ADDRESS				REGISTER CONTENT	READ/WRITE
A3	A2	A1	A0		
0	0	0	0	X1 measurement result	R
0	0	0	1	X2 measurement result	R
0	0	1	0	Y1 measurement result	R
0	0	1	1	Y2 measurement result	R
0	1	0	0	I_X measurement result	R
0	1	0	1	I_Y measurement result	R
0	1	1	0	Z1 measurement result	R
0	1	1	1	Z2 measurement result	R
1	0	0	0	Status	R
1	0	0	1	AUX measurement result	R
1	0	1	0	RESERVED	
1	0	1	1	RESERVED	
1	1	0	0	CFR0	R/W
1	1	0	1	CFR1	R/W
1	1	1	0	CFR2	R/W
1	1	1	1	Converter function select status	R

R/$\overline{W}$ is the register read and write control. A 1 indicates that the value of the internal register address bits A3–A0 is stored internally as the starting address for a register read (see Figure 34). The content of the addressed register is sent to SDA by using I^2C read addressing (see Figure 35 and Figure 36). A0 indicates that the data following control byte 0 on SDA are written into the internal register addressed by bits A3–A0 (see Figure 34).

7.5.4 Start a Write Cycle

A write cycle begins when the master issues the slave address to the TSC2013-Q1 device. The slave address consists of seven address bits and a write bit (R/$\overline{W}$ = 0; see Table 6).On receipt of the eighth bit, if the address matches the AD1 through AD0 address input pin setting, the TSC2013-Q1 device issues an acknowledge bit by pulling SDA low for one additional clock cycle (ACK = 0); see Figure 33.

When the master receives the acknowledge bit from the TSC2013-Q1 device, the master writes the input control byte to the slave (see Table 6). After the control byte is received by the slave, the slave issues another acknowledge bit by pulling SDA low for one clock cycle (ACK = 0). The master then ends the write cycle by issuing a STOP or repeated START condition; see Figure 34.



(1) In order to start the next sequence, a stop condition must be followed by a start condition. If no stop is used, then a repeated start (Sr) must be used. Also note that if a stop condition is issued in high-speed mode, the mode reverts to the previous mode which is either fast or standard mode.

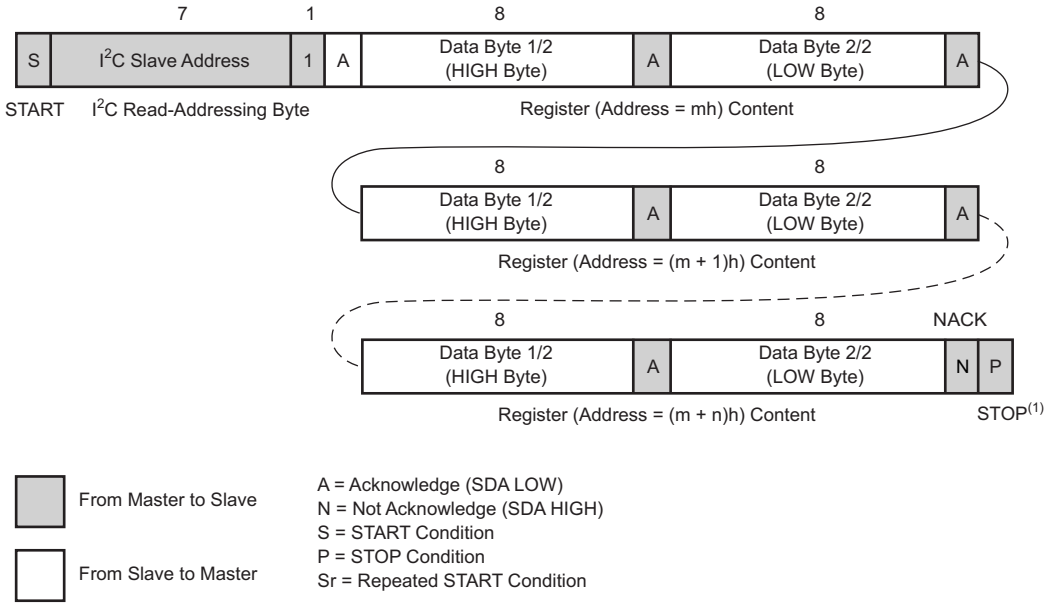
(2) mh is a hexadecimal number.

Figure 34. Write Cycle

7.5.5 Register Access

Data access begins with the master issuing a START (or repeated START) condition followed by the 7-bit address and a read bit (R/$\overline{W}$ = 1; see Table 6). On receipt of the eighth bit has been received and an address match, the slave issues an acknowledge by pulling SDA low for one clock cycle (ACK = 0). The first byte of serial data then follows. After the slave has sent the first byte, it then releases the SDA line for the master to issue an acknowledge (ACK = 0). The slave issues the second byte of serial data on receiving the acknowledgment from the master (D7–D0), followed by a not-acknowledge bit (ACK = 1) from the master to indicate receipt of the last data byte has been received. The master then issues a STOP condition (P) or repeated START (Sr), which ends the read cycle, as shown in Figure 35 and Figure 36. If the master issues a not-acknowledge (ACK = 1) after receipt of the first data byte, the master must then issue a stop condition (P) to reset the registers. If the master is not ready to receive the second data byte, it should issue the acknowledge (ACK = 0), or the master should stretch the clock. On restart of the clock, the master can receive the second byte of data.

Read Cycle: Sequential, from Register Address mh(2) to (m + n)h(3)

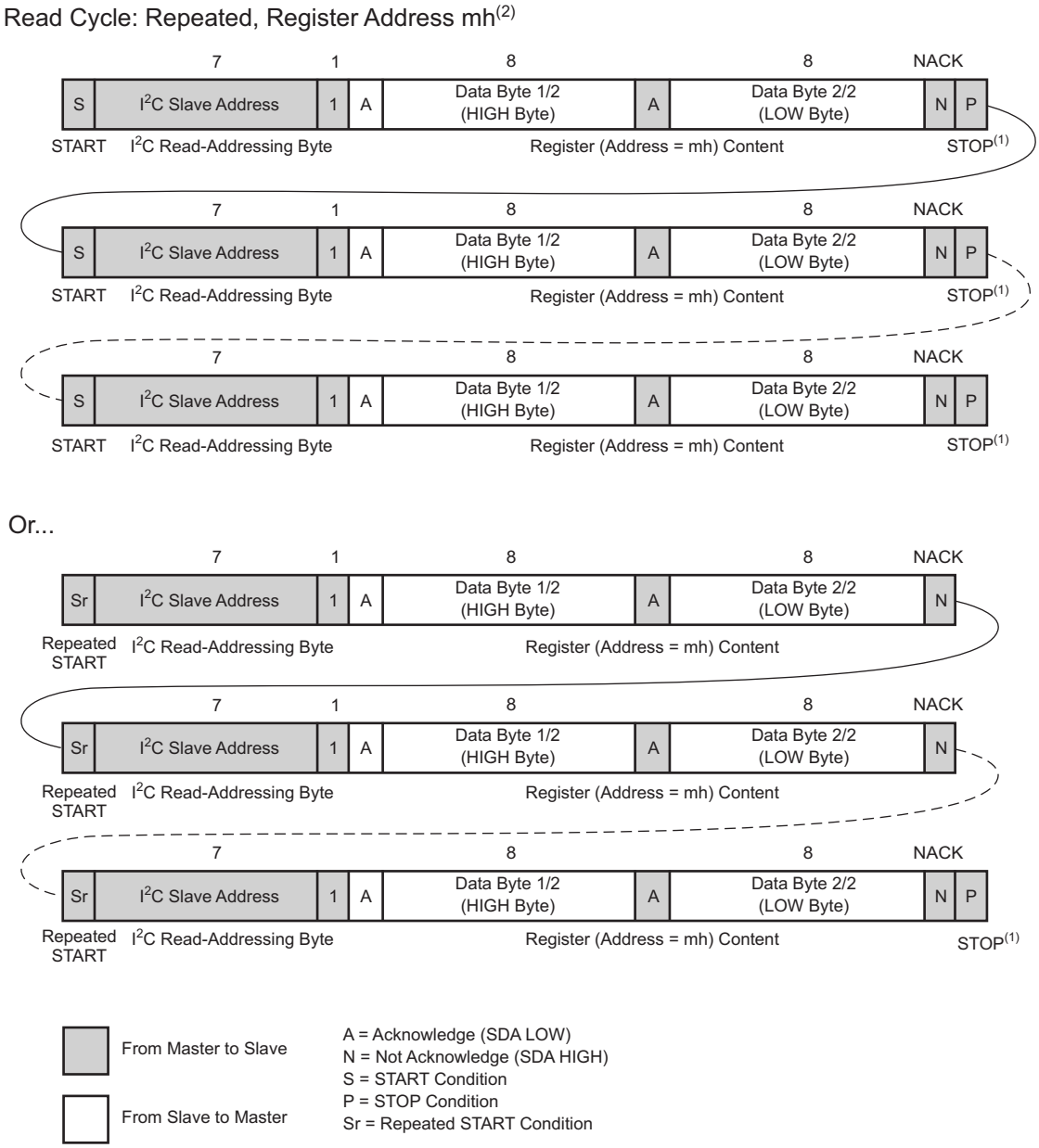


(1) In order to start the next sequence, a Stop condition must be followed by a start condition. If no stop is used, then a repeated start must be used. Also note that if a stop condition is issued in high-speed mode, the mode reverts to the previous mode which is either fast or standard mode.

(2) mh is a hexadecimal number.

(3) If (m+n)h is greater than Fh, then (m + n)h is modulo 16.

Figure 35. Sequential Read Cycle



(1) In order to start the next sequence, a Stop condition must be followed by a start condition. If no stop is used, then a repeated start must be used. Also note that if a stop condition is issued in high-speed mode, the mode reverts to the previous mode which is either fast or standard mode.

(2) mh is a hexadecimal number.

Figure 36. Repeated Read Cycle

7.5.6 Communication Protocol

All control of the TSC2013-Q1 is through registers. Reading and writing to these registers are accomplished by the use of Control Byte 0, which includes a 4-bit address plus one read-write TSC register-control bit. The data registers defined in Table 9 are all 16-bit, right-adjusted.

NOTE

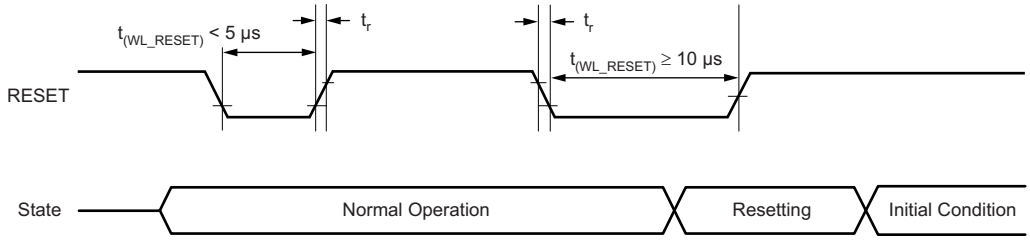
Except for some configuration registers and the status register that are full 16-bit registers, the rest of the value registers are 12-bit (or 10-bit) data preceded by four (or six) zeros.

See the *Configuration and Status Registers* section for the register field descriptions.

7.5.7 Register Reset

The TSC2013-Q1 device can be reset in one of three ways. First, at power-on, a power-good signal generates a prolonged reset pulse internally to all registers.

Second, an external pin, $\overline{\text{RESET}}$, is available to perform a system reset or allow other peripherals (such as a display) to reset the device if the pulse meets the timing requirement (at least 10 µs in duration). Any $\overline{\text{RESET}}$ pulse less than 5 µs is rejected. To accommodate the timing drift between devices because of process variation, a $\overline{\text{RESET}}$ pulse duration between 5 µs and 10 µs falls into the gray area that is unrecognized, giving an undetermined result; avoid this situation. See Figure 37 for details. A good reset pulse must be low for at least 10 µs. An internal spike filter is available to reject spikes up to 20 ns wide.



NOTE: See the timing requirement tables in the *Specifications* section for more information.

Figure 37. External Reset Timing

Third, a software reset is activated by writing a 1 to CB1.1 (bit 1 of control byte 1). Note that this reset is not self-clearing, so the user must write a 0 to remove the software reset.

A reset clears all registers and loads default values. A power-on reset and external (hardware) reset take precedence over a software reset. If the user does not clear a software reset, either a power-on reset or an external (hardware) reset clears it.

7.6 Register Maps

The TSC2013-Q1 device has several 16-bit registers that allow control of the device, as well as providing a location to store results from the TSC2013-Q1 device until read out by the host microprocessor. shows the memory map.

Register Content and Reset Values(1)

A3-A0 (HEX)	REGISTER NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	RESET VALUE (HEX)
0	X1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
1	X2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
2	Y1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
3	Y2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
4	IX	T(2)	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
5	IY	T(2)	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
6	Z1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
7	Z2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
8	Status	DAVX	DAVY	DAVZ1	DAVZ2	DAVAUX	0	0	0	RESET	0	0	0	0	PDST	0	0	0004
9	AUX	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
A	RSVD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
B	RSVD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
C	CFR0	PSM	STS	RM	CL1	CL0	PV2	PV1	PV0	PR2	PR1	PR0	SN2	SN1	SN0	DTW	LSM	4000
D	CFR1	0	0	0	0	0	0	0	0	0	0	0	0	0	BTD2	BTD1	BTD0	0000
E	CFR2	PINTS1	PINTS0	M1	M0	W1	W0	0	0	0	0	0	MAVE X TRIPLET	MAVE Y TRIPLET	MAVE Z	MAVE AUX	0	0000
F	CFN	CFN15	CFN14	CFN13	0	0	0	0	CFN8	CFN7	R6	R5	R4	R3	R2	R1	R0	0000

(1) For all combination bits, do not use the pattern marked as *RSVD* (reserved). The default pattern is read back after reset.
(2) Use of the D15 bit only occurs during a single IX or single IY conversion command.
T = 0: No touch detected during conversion
T = 1: Touch detected during conversion

7.6.1 Configuration and Status Registers

7.6.1.1 Configuration Register 0

7.6.1.1.1 Configuration Register 0 (address = 0) [reset = 4000h for read; 0000h for write]

Figure 38. Configuration Register 0

D15	D14	D13	D12	D11	D10	D9	D8
PSM	STS	RM	CL[1:0]		PV[2:0]		
R/W-Reset	R/W-	R/W-	R/W-		R/W-		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PR[2:0]			SN[2:0]			DTW	LSM
R/W-			R/W-			R/W-	R/W-

Table 10. Configuration Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
D15	PSM	R/W	0	**Pen status or control mode. This bit is the MSB.** Reading this bit allows the host to determine if a touch of the screen has occurred. Writing to this bit selects the mode used to control the flow of converter functions that are either initiated and/or controlled by host or under control of the TSC2013-Q1 responding to a pen touch. When reading, the PSM bit indicates if the pen is down or not. When writing to this register, this bit determines if the TSC2013-Q1 or the host controls the converter functions. The default state is the host-controlled converter function mode (0). The other state (1) is the TSC-initiated scan function mode that must only collaborate with C3–C0 = 0000 or 0001 in order to allow the TSC2013-Q1 to initiate and control the scan function for XYZ or XY when a on detection of a pen touch. 0 (R): No screen touch detected 1 (R): Screen touch detected 0 (W): Converter functions initiated and/or controlled by host 1 (W): Converter functions initiated and controlled by the TSC2013-Q1
D14	STS	R/W	1 for R 0 for W	**ADC status** When reading, this bit indicates if the converter is busy or not busy. Continuous scans or conversions can be stopped by writing a 1 to this bit, immediately aborting the running converter function (even if the pen is still down) and causing the ADC to power down. The default state for write is 0 (normal operation), and the default state for read is 1 (converter is not busy). Note that the same bit can be written through Control Byte 1 (bit 0). This bit is self-clearing. 0 (R): Converter is busy 1 (R): Converter is not busy 0 (W): Normal operation 1 (W): Stop converter function and power down
D13	RM	R/W	0	**Resolution control** This bit specifies the ADC resolution. See for a description of these bits. This bit is the same whether reading or writing, and defaults to 0. Note that one cn write the same bit through Control Byte 1. 0: 10-bit resolution. Default after power up and reset 1: 12-bit resolution

Table 10. Configuration Register 0 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
D12-D11	CL[1:0]	R/W	0	Conversion-clock control These two bits specify CL bits that specify the clock rate that the ADC uses to perform conversion. CL1 = 0, CL0 = 0: $f_{(ADC)} = f_{(OSC)}$ / 1, referred to as the 4-MHz ADC clock rate, 10-bit resolution only CL1 = 0, CL0 = 1: $f_{(ADC)} = f_{(OSC)}$ / 2, referred to as the 2-MHz ADC clock rate CL1 = 1, CL0 = 0: $f_{(ADC)} = f_{(OSC)}$ / 4, referred to as the 1-MHz ADC clock rate CL1 = 1, CL0 = 1: $f_{(ADC)} = f_{(OSC)}$ / 4, referred to as the 1-MHz ADC clock rate
D10-D8	PV[2:0]	R/W	0	**Panel-voltage stabilization-time control** These bits specify a delay time from the moment of touch-screen drivers enabling to the time of voltage sampling and the start of a conversion. These bits allow the user to adjust the appropriate settling time for the touch panel and external capacitances. See for settings of these bits. The default state is 000, indicating a 0-µs stabilization time ($t_{(PVS)}$). These bits are the same whether reading or writing. PV2 = 0, PV1 = 0, PV0 = 0: 0 µs PV2 = 0, PV1 = 0, PV0 = 1: 100 µs PV2 = 0, PV1 = 1, PV0 = 0: 500 µs PV2 = 0, PV1 = 1, PV0 = 1: 1 ms PV2 = 1, PV1 = 0, PV0 = 0: 5 ms PV2 = 1, PV1 = 0, PV0 = 1: 10 ms PV2 = 1, PV1 = 1, PV0 = 0: 50 ms PV2 = 1, PV1 = 1, PV0 = 1: 100 ms
D7-D5	PR[2:0]	R/W	0	**Precharge time selection** These bits set the amount of time allowed for precharging any pin capacitance on the touch screen prior to sensing whether a pen touch is in progress. The following lists the precharge time ($t_{(PRE)}$) PR2 = 0, PR1 = 0, PR0 = 0: 20 µs PR2 = 0, PR1 = 0, PR0 = 1: 84 µs PR2 = 0, PR1 = 1, PR0 = 0: 276 µs PR2 = 0, PR1 = 1, PR0 = 1: 340 µs PR2 = 1, PR1 = 0, PR0 = 0: 1.044 ms PR2 = 1, PR1 = 0, PR0 = 1: 1.108 ms PR2 = 1, PR1 = 1, PR0 = 0: 1.3 ms PR2 = 1, PR1 = 1, PR0 = 1: 1.364 ms
D4-D2	SN[2:0]	R/W	0	**Sense-time selection** These bits set the amount of time the TSC2013-Q1 device waits after converting a coordinate to sense whether a screen touched is in progress. SNS2 = 0, SNS1 = 0, SNS0 = 0: 32 µs SNS2 = 0, SNS1 = 0, SNS0 = 1: 96 µs SNS2 = 0, SNS1 = 1, SNS0 = 0: 544 µs SNS2 = 0, SNS1 = 1, SNS0 = 1: 608 µs SNS2 = 1, SNS1 = 0, SNS0 = 0: 2.08 ms SNS2 = 1, SNS1 = 0, SNS0 = 1: 2.144 ms SNS2 = 1, SNS1 = 1, SNS0 = 0: 2.592 ms SNS2 = 1, SNS1 = 1, SNS0 = 1: 2.656 ms

Table 10. Configuration Register 0 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
D1	DTW	R/W	0	**Detection of pen touch in wait (patent pending)** Writing a 1 to this bit enables pen-touch detection in the background while waiting for the host to issue the converter function in host-initiated and -controlled modes. This background detection allows the TSC2013-Q1 to pull $\overline{\text{PINTDAV}}$ high to indicate no pen touch detected while waiting for the host to issue the converter function. If the host polls a high state at $\overline{\text{PINTDAV}}$ before the transmission of the convert function, the host can abort the issuance of the convert function and stay in the polling $\overline{\text{PINTDAV}}$ mode until the detection of the next pen touch.
D0	LSM	R/W	0	**Longer sampling mode. This bit is the LSB.** With this bit set to 1, an extra 500 ns of sampling time is added to the normal sampling cycles of each conversion. This additional time is represented as approximately two internal oscillator clock cycles.

7.6.1.2 Configuration Register 1 (address = Dh) [reset = 0000h]

Configuration register 1 (CFR1) defines the connection test-bit modes configuration and batch-delay selection.

Figure 39. Configuration Register 1

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
W-0							
D7	D6	D5	D4	D3	D2	D1	D0
RESERVED					BTD[2:0]		
W-0					R/W-0		

Table 11. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
D15-D3	RESERVED	W	0	
D2-D0	BTD[2:0]	R/W	0	**Batch time-delay mode** These are the selection bits that specify the delay before the triggering of a sample or conversion scan cycle. When it is set, Batch time-delay mode uses a set of timers to trigger a sequence of sample-and-conversion events automatically. The mode works for both TSC-initiated scans (XYZ or XY) and host-initiated scans (XYZ or XY). Configure a TSC-initiated scan (XYZ or XY) by setting the PSM bit in CFR0 to 1 and C[3:0] in control byte 1 to 0000 or 0001. In the case of a TSC-initiated scan (XYZ or XY), the sequence begins with the TSC responding to a pen touch. After the first processed sample set completes during the batch delay, the scan enters a wait mode until the end of the batch delay. If detection of a pen touch persists at that moment, the scan continues to process the next sample set, along with a resumption of the batch delay. The selected batch delay during the time of the detected pen touch regulates the throughput of the processed sample sets (shown in as sample sets per second, or SSPS). One can configure a TSC-initiated scan (XYZ or XY) by setting the PSM bit in CFR0 to 1 and C[3:0] in control byte 1 to 0000 or 0001. Note that the throughput of the processed sample set also depends on the settings of stabilization, precharge, and sense times, and the total number of samples to be processed per coordinates. If the accrual time of these factors exceeds the batch delay time, the accrual time dominates. Batch delay time starts when the pen touch initiates the scan function that converts coordinates. One can configure a host-initiated scan (XYZ or XY) by setting the PSM bit in CFR0 to 0 and C[3:0] in control byte 1 to 0000 or 0001. For the host-initiated scan (XYZ or XY), the host must set TSC internal register C[3:0] in control byte 1 to 0000 or 0001 initially after a pen-touch detection; see . After engagement of the scan (XYZ or XY), the selected batch-delay timer regulates the throughput of the processed sample sets, as long as the initial detected touch is uninterrupted.

Table 11. Configuration Register 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Throughput for TSC-initiated or host-initiated scan, XYZ OR XY: BTD2 = 0, BTD1 = 0, BTD0 = 0, t_d = 0: Normal operation throughput depends on settings BTD2 = 0, BTD1 = 0, BTD0 = 1, t_d = 1: 1000 SSPS BTD2 = 0, BTD1 = 1, BTD0 = 0, t_d = 2: 500 SSPS BTD2 = 0, BTD1 = 1, BTD0 = 1, t_d = 4: 250 SSPS BTD2 = 1, BTD1 = 0, BTD0 = 0, t_d = 10: 100 SSPS BTD2 = 1, BTD1 = 0, BTD0 = 1, t_d = 20: 50 SSPS BTD2 = 1, BTD1 = 1, BTD0 = 0, t_d = 40: 25 SSPS BTD2 = 1, BTD1 = 1, BTD0 = 1, t_d = 100: 10 SSPS For example, if stabilization time, precharge time, and sense time are selected as 100 µs, 84 µs, and 96 µs, respectively, and the batch delay time is 2 ms, then the scan function enters wait mode after the first processed sample set until the 2 ms of batch-delay time expires. When the scan function starts to process the second sample set (if a touch is still present on the screen), the batch delay restarts at 2 ms (in this example). This procedure remains regulated by 2 ms until the pen touch is undetected or a stop bit or any reset form stops the scan function.

7.6.1.3 Configuration Register 2 (address = Eh) [reset = 0000h]

Configuration register 2 (CFR2) defines the preprocessor configuration.

Figure 40. Configuration Register 2

D15	D14	D13	D12	D11	D10	D9	D8
PINTS1	PINTS0	M[1:0]		W[1:0]		RESERVED	
R/W-0	R/W-0	R/W-00		R/W-00		W-0	
D7	D6	D5	D4	D3	D2	D1	D0
RESERVED			MAVE X TRIPLET	MAVE Y TRIPLET	MAVE Z	MAVE AUX	RESERVED
W-0			R/W-0000	R/W-0000	R/W-0000	R/W-0000	W-0

Table 12. Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
D15	PINTS1	R/W	0	This bit controls the output format of the $\overline{\text{PINTDAV}}$ pin. With this bit set to 0, the output format is the AND-form of internal signals of $\overline{\text{PENIRQ}}$ and DAV). With this bit set to 1, $\overline{\text{PINTDAV}}$ outputs $\overline{\text{PENIRQ}}$ only. $\overline{\text{PINTDAV}}$ PIN OUTPUT = 0: AND combination of $\overline{\text{PENIRQ}}$ (active-low) and DAV (active-high). 0: Data available, $\overline{\text{DAV}}$ (active-low). 1: Interrupt, $\overline{\text{PENIRQ}}$ (active-low) generated by pen-touch. 1: Data available, $\overline{\text{DAV}}$ (active-low).
D14	PINTS0	R/W	0	This bit selects the output on the $\overline{\text{PINTDAV}}$ pin. With this bit set to 0, the output format of $\overline{\text{PINTDAV}}$ depends on the selection made on the PINTS1 bit. With this bit set to 1, $\overline{\text{PINTDAV}}$ outputs the internal signal of $\overline{\text{DAV}}$. $\overline{\text{PINTDAV}}$ PIN OUTPUT = 0: AND combination of $\overline{\text{PENIRQ}}$ (active-low) and DAV (active-high). 1: Data available, $\overline{\text{DAV}}$ (active-low). 0: Interrupt, $\overline{\text{PENIRQ}}$ (active-low) generated by pen-touch. 1: Data available, $\overline{\text{DAV}}$ (active-low).
D13-D12	M[1:0]	R/W	00	Preprocessing MAV filter control Note that when the MAV filter is processing data, the STS bit and the corresponding DAV bits in the status register indicate that the converter is busy until all conversions necessary for the preprocessing are complete. The default state for these bits is 0000, which bypasses the preprocessor. These bits are the same whether reading or writing.
D11-D10	W[1:0]	R/W	00	Preprocessing MAV filter control Note that when the MAV filter is processing data, the STS bit and the corresponding DAV bits in the status register indicate that the converter is busy until all conversions necessary for the preprocessing are complete. The default state for these bits is 0000, which bypasses the preprocessor. These bits are the same whether reading or writing.
D9-D5	RESERVED	W	0	
D4-D1	MAVE	R/W	0000	MAV-filter function-enable bit When any bit is set to 1, the MAV filter setup is applied to the corresponding measurement.
D0	RESERVED	W	0	

7.6.1.4 Converter-Function Select Register (address = Fh) [reset = 0000h]

The converter-function select (CFN) register reflects the converter function select status.

Figure 41. Converter-Function Select Register

D15	D14	D13	D12	D11	D10	D9	D8
CFN[15:13]			RESERVED				CFN[8:0]
R-0			R-0				R-0
D7	D6	D5	D4	D3	D2	D1	D0
CFN[8:0]							
R-0							

Table 13. Converter-Function Select Register Field Descriptions

Bit	Field	Type	Reset	Description
D15-D13	CFN[15:13]	R	0	Touch-screen driver status These bits represent the current status of the turned-on touch-screen drivers. The device sets CFN13 to 1 with both X+ and X– drivers turned on, CFN14 to 1 with both Y+ and Y– drivers turned on, and CFN15 to 1 with Y+ and X– drivers turned on. Otherwise, the device sets these bits to 0. The device resets these bits to 000b whenever the converter function is complete, stopped by the STS bit, or reset (by a hardware reset from the RESET pin or a software reset from SWRST bit in control byte 1).
D12-D9	RESERVED	R	0	
D8-D0	CFN[8:0]	R	0	Converter function-select status. These bits represent the converter function currently running, which is set in bits C3–C0 of control byte 1. When the CFNx bit shows 1, where x is the decimal value of converter function-select bits C3–C0, it is an indication that the converter function set in bits C3–C0 is running. For example, when CFN2 shows 1, it indicates the converter function set in bits C3-C0 (0010) is running. Reset of the CFNx bits to 0000h occurs whenever the converter function is complete, stopped by STS bit, or reset (by the hardware reset from the RESET pin or the software reset from SWRST bit in Control Byte 1). However, if the TSC sets the PSM bit in the CFR0 register to 1 to initiate the scan-function mode, reset of the CFN0 or CFN1 does not occur when the corresponding converter function is complete, because there is no pen touch. This event allows the TSC2013-Q1 to initiate the scan process (corresponding to CFN0 or CFN1 set to 1) immediately on detection of the next pen touch.

7.6.1.5 Status Register (address = 8h) [reset = 0004h]

The Status Register provides information about the TSC2013-Q1 status.

Figure 42. Status Register

D15	D14	D13	D12	D11	D10	D9	D8
DAV Due X TRIPLET	DAV Due Y TRIPLET	DAV Due Z1	DAV Due Z2	DAV Due AUX	RESERVED		
R-0					R-0		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESET Flag	RESERVED				PDST	RESERVED	
R-0	R-0				R-1	R-0	

Table 14. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
D15-D11	DAV	R	0	Data available bits These five bits mirror the operation of the internal signals of DAV. On storing any processed data in data registers, the DAV bit (D15 to D11) corresponding to the data type is set to 1. The bIt stays at 1 until the registers updated to the host has read out the processed data. If the user submits a single I_X or single I_Y conversion command, bit D15 or D14 (respectively) shows data availability. In this case, only data register I_X or I_Y receives an update. 0: No new processed data are available. 1: Processed data are available. This bit remains at 1 until the host has read out all updated registers.
D10-D8	RESERVED	R	0	
D7	RESET	R	0	Interpretation of the RESET flag bits: 0: Device was reset since the last status poll (hardware or software reset). 1: Device reset has not occurred since the last status poll.
D6-D3	RESERVED	R	0	
D2	PDST	R	1	Power-down status This bit reflects the setting of the PND0 bit in Control Byte 0. When this bit shows 0, it indicates ADC bias circuitry power is still on after each conversion and before the next sampling; otherwise, it indicates ADC bias circuitry power is down after each conversion and before the next sampling. However, power is down between conversion sets. Because this status bit is in synchrony with the internal clock, it does not reflect the setting of the PND0 bit until detection of a pen touch is detected or initiation of a converter function.
D1-D0	RESERVED	R	0	

7.6.2 Data Registers

The data registers of the TSC2013-Q1 hold data results from conversions. All of these registers default to 0000h on reset.

7.6.2.1 X1, X2, IX, Y1, Y2, IY, Z1, Z2, and AUX registers (offset = see) [reset = see]

The results of all ADC conversions are placed in the appropriate data registers, as described in Table 9. The data format of the result word (R) of these registers is right-justified, as shown in .

Figure 43. X1, X2, IX, Y1, Y2, IY, Z1, Z2, and AUX Registers

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED				R11(1)	R10(1)	R9	R8
R-0				R-0	R-0	R-0	R-0
D7	D6	D5	D4	D3	D2	D1	D0
R7	R6	R5	R4	R3	R2	R1	R0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

(1) R11 and R10 are 0 in 10-bit mode.

Table 15. X1, X2, IX, Y1, Y2, IY, Z1, Z2, and AUX Register Field Descriptions

Bit	Field	Type	Reset	Description
D15-D12	RESERVED	R	0	Use of the D15 bit only occurs during a single IX or single IY conversion command (see). T = 0: No touch detected during conversion T = 1: Touch detected during conversion
D11-D0	R[11:0]	R	0	12-bit data

8 Application and Implementation

8.1 Application Information

8.1.1 Auxiliary Measurement

The TSC2013-Q1 device can measure the voltage from the auxiliary input (AUX). Applications for the AUX can include external temperature sensing, ambient light monitoring for controlling backlighting, or sensing the current drawn from batteries. Two converter functions can be used for the measurement of the AUX:

1. Non-continuous AUX measurement as shown in Figure 44 (converter function select bits C[3:0] = control byte 1 D[6:3] = 0101)
2. Continuous AUX measurement as shown in Figure 45 (converter function select bits C[3:0] = control byte 1 D[6:3] = 1000)

   See Table 7 for more information on the converter function select bits.

Use Equation 9 to calculate the time required to make a non-continuous auxiliary measurement.

$$t_{(COORDINATE)} = \frac{t_{(OH3)}}{f_{(OSC)}} + N \times \left((B+2) \times \frac{f_{(OSC)}}{f_{(ADC)}} + t_{c(OH)} \right) \times \left(\frac{1}{f_{(OSC)}} \right) + \left(\frac{t_{(PPRO)}}{f_{(OSC)}} \right) \quad (9)$$

where

- $t_{(OH3)}$ = overhead time number 3 = 3.5 internal clock cycles.

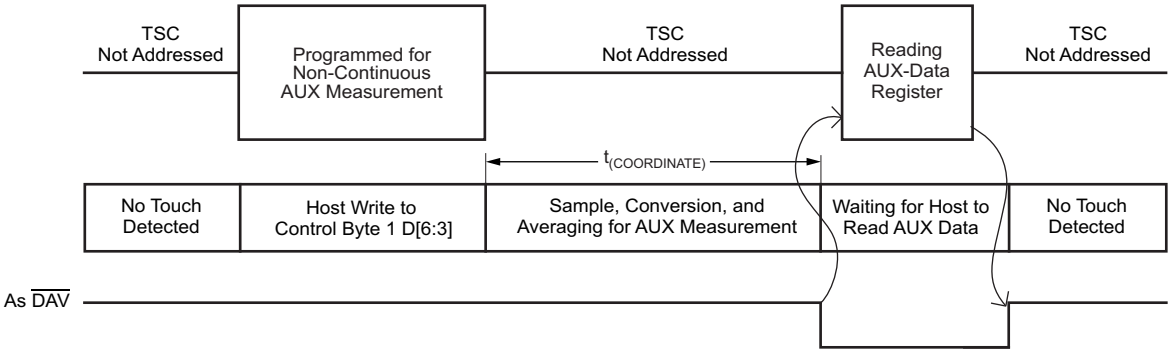


Figure 44. Non-Touch Screen, Non-Continuous AUX Measurement

Use Equation 9 to calculate the time required to make a continuous auxiliary measurement.

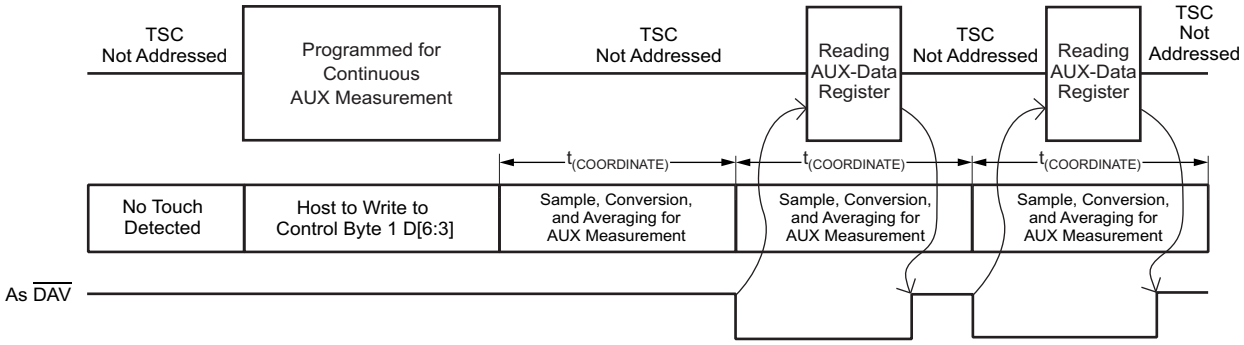


Figure 45. Non-Touch Screen, Continuous AUX Measurement

8.1.2 Single IX or Single IY Measurement

Figure 46 shows the sequence for a single IX or single IY measurement.

Application Information (continued)

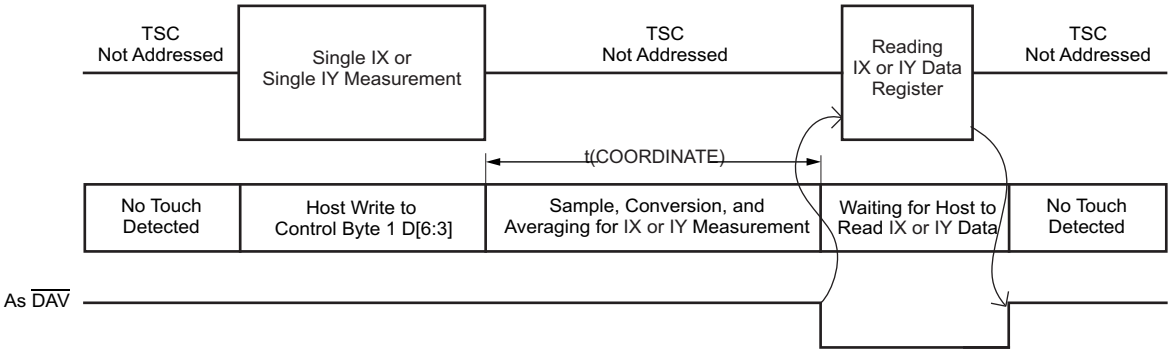


Figure 46. Touch Screen, Single IX or IY Measurement

8.2 Typical Application

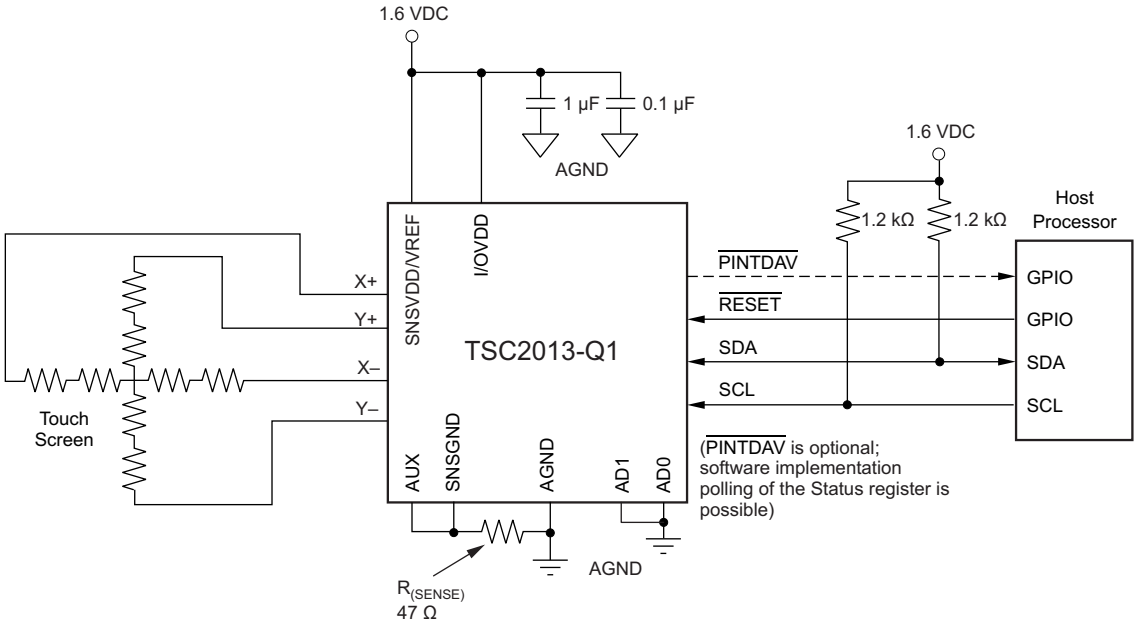


Figure 47. Typical Application Diagram

8.2.1 Design Requirements

The system-level requirements for this design include:

- Normal 4-wire resistive touch screen with low activation force (from center area down to 0.1 to 0.3 N) to enable smooth dual-touch operation.
- The $R_{(SENSE)}$ resistor value is the lowest panel resistance (X or Y layer) which is approximately 4.5. This resistor value provides the best dynamic range for dual-touch separation.
- To achieve the best possible SNR, select the highest operating voltage of the TSC2013-Q1 device that is compatible with the system.

8.2.2 Detailed Design Procedure

Resistive dual touch using TSC2013-Q1 device is based on the principle of measuring resistance changes between X and Y panel. The resistive touch screen has two ITO layers which are located apart from each other. When the user uses a single-finger touch, only a minor parallel connection occurs between these two layers.

Typical Application (continued)

During a dual-finger touch when the finger touches are located on different areas of the screen, parallel connection is much higher which results in a reduction in panel resistance. Because the TSC2013-Q1 device measures both X and Y-layer panel resistance, the finger touch distance can be easily calculated from the resistance change. This calculation is achieved by using one external resistor the is connected internally in series with the measured X-Y panel.

Use the following methods to enable the dual-touch function of the TSC2013-Q1 device:

- Measure all four nodes and use those measurements to calculate center point of the finger touch.
- Use the measurements of the four nodes to correctly place the touch positions to the correct quadrants.
- Measure the two-layer panel resistance by using a single external resistor that is connected internally in series with measured panel layer. A change in resistance is interpreted as a change in finger distance.

All calculations are performed by the host-side processor. The TSC2013-Q1 device provides only data.

The following sections describe the design procedure in detail.

8.2.2.1 Power-On-Reset and Reset Consideration

The TSC2013-Q1 device can be rest to the default working state in one of three ways. These resets are: power-on reset (see the *Power-On Reset* section), hardware reset (see the *Hardware Reset* section), and software reset (see the *Software Reset* section).

The requirements for ensuring a proper TSC2013-Q1 power-on reset (POR) are very stringent and can be very hard to meet in many applications. To workaround this issue, users should apply a proper hardware or software reset, instead of or in addition to the POR.

8.2.2.1.1 Power-On Reset

Based on design principles and extensive tests with TSC2013-Q1 device, the power of the device must meet a specific on-off timing and sequence to ensure the POR is implemented during each TSC2013-Q1 power on. This specific timing and sequence also ensures that a lockup is prevented.

During the device power on, the POR brings the TSC2013-Q1 device into a known default working state by initializing the internal state machine, data and control registers, and the condition of the output pins. Without the POR, the TSC2013-Q1 device can power on in a random state and can cause the $\overline{\text{PINTDAV}}$ pin to respond incorrectly.

The TSC2013-Q1 POR circuit was designed to not consume power during normal operation. The power-down current is kept as low as possible (0.8-µA maximum power-down supply current).

This POR circuit in TSC2013-Q1 device requires specific power-up and power-down ramps and sequences.

Figure 48 shows and Table 16 lists the recommended power-off times, on-ramp, and off-ramp specifications.

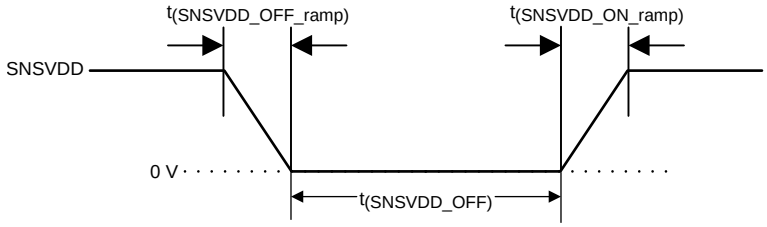


Figure 48. POR Sequence

Table 16. Requested POR Timings

TEMPERATURE RANGE	MINIMAL $t_{(SNSVDD\_OFF\_ramp)}$	MINIMAL $t_{(SNSVDD\_ON\_ramp)}$	MINIMAL $t_{(SNSVDD\_OFF)}$ (1)
–40°C to –21°C	12 kV/s	12 kV/s	1.2 s
–20°C to 85°C	2 kV/s	12 kV/s	200 ms

(1) $t_{(SNSVDD\_OFF)}$ time begins when the SNSVDD pin voltage reaches and stays at 0 V.

8.2.2.1.2 Requesting a Minimal $t_{(SNSVDD\_OFF)}$ Time

The POR circuit of the TSC2013-Q1 device contains a capacitor that is charged when the device powers up which generates an internal reset signal. This capacitor is discharged after the TSC2013-Q1 supply is switched off. The TSC2013-Q1 device is designed for low-power operation, therefore the POR requires time to charge and discharge the capacitor, especially under cold temperatures (less than –20°C). If the SNSVDD off time is not sufficient, the device can lock up. Only a power recycle can resolve this lockup condition.

8.2.2.1.3 Requesting a Minimal $t_{(SNSVDD\_OFF\_ramp)}$ and $t_{(SNSVDD\_ON\_ramp)}$ Ramp

To ensure proper initialization of the TSC2013-Q1 device, the device must reach a certain voltage before the internal POR signal is released. If the power supply on the ramp is too slow the device can power up in a random state which can cause a lock up.

The capacitor inside the POR circuit must be discharged through the SNSVDD pin. To support a proper discharge when the TSC2013-Q1 supply is switched off, TI recommends to provide a low resistance path on the SNSVDD pin.

8.2.2.1.4 Hardware Reset

The hardware reset pin, $\overline{\text{RESET}}$, is available to perform a system reset which resets the device if the pulse width meets the timing requirement (at least 10-µs wide and the SNSVDD/VREF or I/OVDD pin is greater than or equal to 1.6 V). Any reset pulse less than 5 µs is rejected. To accommodate the timing drift between devices because of process variation, a reset pulse width between 5 µs and 10 µs is not recognized and the result is undetermined. This situation should be avoided. A good reset pulse must be low for at least 10 µs (SNSVDD/VREF or I/OVDD pin is greater than or equal to 1.6 V). An internal spike filter rejects spikes up to 20 ns wide. See Figure 37 for the hardware reset timing diagram.

8.2.2.1.5 Software Reset

During normal operation a software reset can be sent by the host processor to the device by setting the SWRST bit (D1) to 1 in the control byte 1 (see *Table 6*).

8.2.2.2 Power Up Considerations

8.2.2.2.1 Power-Off Cycles During Normal Operation

The TSC2013-Q1 device is a low-power device and therefore switching the TSC2013-Q1 device off during normal operation is not needed nor recommended.

Every power cycle (power on → power off → power on) must meet the requirements described in the *Power-On Reset* section. If requirements cannot be met, TI recommends to issue a hardware reset after every power cycle.

8.2.2.2.2 Supply Glitches During Normal Operation

A TSC2013-Q1 SNSVDD or IOVDD power glitch during normal operation can cause a lockup condition. Therefore ensure that the system is able to either recycle the power in the system following the requirements described in the *Power-On Reset* section or issue a hardware reset as described in the *Hardware Reset* section.

8.2.2.2.3 TSC2013-Q1 Digital Pins

In many applications, users use the same power supply for both the TSC2013-Q1 analog and digital supplies. The SNSVDD supply is connected with the I/OVDD supply. Under such cases, the logic high status on the TSC2013-Q1 digital pins before power-up become a concern when performing a proper POR.

Table 17 lists the digital I/O pins of the TSC2013-Q1 device.

Table 17. TSC2013-Q1 Digital Pin List

TSC2013-Q1 PINS	DESCRIPTION
$\overline{\text{PINTDAV}}$	Digital Output. Data available or the pen-detect interrupt (PENIRQ), depending on setting. Pin polarity is active-low.
$\overline{\text{RESET}}$	Digital input. External hardware reset input (active-low).
SCL	Open drain and collector. Serial clock
SDA	Open drain and collector. Serial data I/O
A0	Digital input. I^2C bus TSC address input bit 0
A1	Digital input. I^2C bus TSC address input bit 1

Every TSC2013-Q1 pin is well protected against ESD strikes. The TSC2013-Q1 $\overline{\text{RESET}}$, A0, and A1 pins have the same protection as the SDA and SCL pins. This protection allows the $\overline{\text{RESET}}$, A0, and A1 pins to be pulled high before the device powers on without activating an internal ESD diode and without causing a power up of the TSC2013-Q1.

The output pin, $\overline{\text{PINTDAV}}$, is a digital output pin. The host processor must define the $\overline{\text{PINTDAV}}$ pin as an input to the host processor without any pullup-pulldown feature. In some cases the default of the host processor is an output with an enabled pullup-pulldown feature but the host-processor firmware changes this definition at a later point to an input. If the TSC2013-Q1 device is not powered up, a power up can also occur through the ESD cells as shown in by the red line in Figure 49. This power up is considered a *false* power up. A false power up cannot ensure a proper power supply to the device or a proper POR.

In case the TSC2013-Q1 device is powered up, both the device and drive processor drive different levels on the same line resulting in high power consumption.

The TSC2013-Q1 $\overline{\text{PINTDAV}}$ pin should be connected to the correct pin on the host processor to avoid bus conflicts and illegal powering up of the TSC2013-Q1 device.

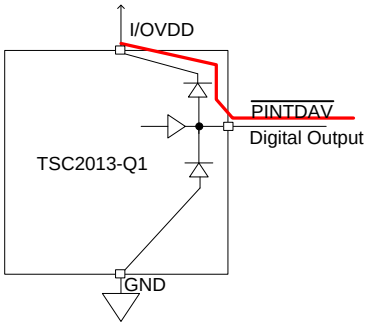


Figure 49. Internal ESD Protection Diodes at the TSC2013-Q1 $\overline{\text{PINTDAV}}$ Pin

8.2.2.2.4 Suggested Hardware Reset During Power-On

The suggested sequence during power up is the following:

- Keep $\overline{\text{RESET}}$ pin low
- Wait for the supplies to settle
- Wait for at least 10µs before releasing the $\overline{\text{RESET}}$ pin

Figure 50 shows the suggested waveform.

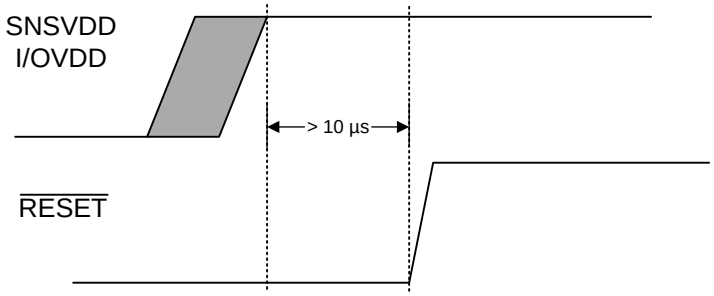


Figure 50. Suggested $\overline{\text{RESET}}$ Waveform During Power-On

8.2.2.3 Device Timing Setup and Use

The TSC2013-Q1 device is a register-based touch-screen controller (TSC). This section describes the setup and use of the programable timings available in the TSC2013-Q1 device.

Figure 52 through Figure 56 in the *Application Curves* were generated to show the principal. The TSC2013-Q1 X triplet contains X1, X2, and IX conversions. The TSC2013-Q1 Y triplet contains Y1, Y2, and IY conversions. The TSC2013-Q1 Z measurement contains Z1 and Z2 conversions.

8.2.2.3.1 Touch-Panel Driving Power

On a resistive touch-screen system, the driving current of the touch panel, provided by the TSC device through the analog interface, has the highest impact on the power consumption in the touch screen system. This touch-panel power consumption is decided by the resistance of the touch panel and the TSC power-supply (SNSVDD) voltage. Figure 51 shows this relationship. The touch screen is driven by the TSC from the SNSVDD supply and the resistance of the panel determines the peak drive current.

Figure 51 only shows the ideal TSC driving condition where the internal resistance of the TSC is ignored because the resistance is small (5 to 6 Ω) compared to the resistance of the touch panel (100s to 1000s Ω). Therefore the actual power consumption should be a little less than that shown in Figure 51.

A user can reduce power consumption in three ways:

- Using touch screens with higher resistance
- Using a low-power supply, SNSVDD, to the TSC
- Reducing the driver on-time or the on-off ratio of the driver

Touch panels with higher resistance are likely to cause more noise and longer settling time which limits the options for users.

The TSC20013-Q1 device is designed with a power supply, SNSVDD, range of 1.6 V to 3.6 V.

Reducing the driver on-time involves setting various touch-screen timings and delays. lists the relevant parameters concerning these timings and delays. The following sections describe the functions and effects of these timings and delays. See the *Register Maps* section for the timing settings of the configuration registers.

8.2.2.3.2 ADC Clock Effects

A TSC2013-Q1 device contains a nominal 4-MHz internal clock that is used to drive the state machines inside the device which performs the many functions. This clock is divided down to provide a clock to run the SAR ADC (analog-to-digital converter). If the 4-MHz clock is used directly (divided by 1), the ADC is limited to a 10-bit resolution, then using higher resolutions at this speed does not result in accurate conversions. The 12-bit resolution requires that the conversion clock run at either 2 MHz (divided by 2) or 1 MHz (divided by 4). The division ratio for the ADC clock is set in the configuration register 0 (CFR0), by setting the CL1 and CL0 bits (see Table 6).

The ability to change the conversion clock rate allows the user to select the optimal value for the ADC resolution, speed, and power dissipation. Higher clock frequency results in faster touch-data converting speed and shorter touch-driver on-time which usually result in lower SNSVDD power consumption. Figure 52 and Figure 53 show examples of the ADC clock effect on the analog interface traffic (X+, X–, Y+, and Y– lines). In these figures, a TSC drives the touch panel to acquire the X, Y, Z1, and Z2 coordinates and three samples-per-coordinate.

Figure 52 shows an analog interface with the clock frequency set to 2 MHz. Figure 53 shows an analog interface with the clock frequency set to 1-MHz. In Figure 52 and Figure 53, other than the ADC clock frequency difference, all other settings are completely identical with the following values: PVS equal to 0 µs, PR equal to 20 µs, and SN equal to 32 µs (see the *Panel Voltage Stabilization Time* section for more information on these timers).

The ADC clock frequency determines the length of the TSC acquisition time and TSC driver on-time. The faster the ADC clock, the shorter the driver on-time. For example, sampling 3 Y data with an ADC clock value of 2 MHz (see Figure 52) uses only about half of the time compared to sampling the data with an ADC clock value of 1 MHz (see Figure 53).

Use Equation 10 to calculate the analog power-supply current, $I_{(SNSVDD)}$.

$$I_{(SNSVDD)} = f\left(V_{(SNSVDD)}\right) + \left(\frac{V_{(SNSVDD)}}{R}\right) \times \left(\frac{SSPS \times S \times B}{f_{(OSC)}}\right) \quad (10)$$

where

- $f(V_{(SNSVDD)})$ is a function of $V_{(SNSVDD)}$
- $V_{(SNSVDD)}$ is the SNSVDD voltage (in V)
- R is the average resistance of the touch panel (in Ω)
- SSPS is sample sets-per-second, which indicates how many sets of touch data is received by the host within a second
- S is the number of data in a set of samples
- B is the TSC resolution, either 10 bit or 12 bit
- $f_{(OSC)}$ is ADC clock frequency, which can be 4, 2, or 1 MHz

Equation 10 includes two parts: the internal circuitry power consumption or $f(V_{(SNSVDD)})$ and the current to drive the external resistive-touch panel which is calculated using Equation 11.

$$I_{(TOUCH–PANEL)} = \left(\frac{V_{(SNSVDD)}}{R}\right) \times \left(\frac{SSPS \times S \times B}{f_{(OSC)}}\right) \quad (11)$$

A concern for using the faster ADC clock is because of the settling time or transients of the analog interface. The higher clock frequency can reduce the accuracy of the data in those cases where the TSC begins the data acquisitions before the analog interface lines reach the stable voltages. Therefore, adding some delays on the analog interface in order to wait for the interface to become stable before an ADC begins working might be necessary. These delays can include the panel voltage-stabilization time, the precharge time of the pins, the sense time (see the *Panel Voltage Stabilization Time* section), or a combination.

8.2.2.4 Panel Voltage Stabilization Time

The panel voltage-stabilization time, $t_{d(PVS)}$, specifies a delay time from the moment the touch screen drivers are enabled to the time the voltage is sampled and a conversion is started. These bits allow the user to adjust the appropriate settling time for the touch panel based on the external capacitances at the analog interface lines.

Figure 54 shows examples where with $t_{d(PVS)}$ is 0 µs (no PVS delay), 100 µs, and 500 µs. In the examples, the TSC uses the sets of 4 × 3 = 12 data which are 3 X, 3 Y, 3 Z1, and 3 Z2. The TSC2013-Q1 device always performs the Y coordinate first when it was set to X-Y or X-Y-Z scan mode. The sequence for receiving a set of samples in Figure 54 is as follows:

1. The TSC adds driver power to Y+ (SNSVDD) and Y– (AGND), waits $t_{d(PVS)}$ µs, and acquires 3 Y data
2. The TSC adds driver power to X+ (SNSVDD) and X– (AGND), waits $t_{d(PVS)}$ µs, and acquires 3 X data
3. The TSC adds driver power to Y+ (SNSVDD) and X– (AGND), waits $t_{d(PVS)}$ µs, and acquires 3 Z1 and 3 Z2 data

The PVS delay consumes power because a driver is on during the PVS delay. Use Equation 12 to calculate the power.

$$P = \left(\frac{V_{(SNSVDD)}}{R} \right) \times SSPS \times t_{d(PVS)} \times 3 \quad (12)$$

where

- 3 indicates that the X, Y, and Z drivers are on

Based on Equation 10, use Equation 13 to calculate a complete expression of the analog power consumption for X-Y-Z 3-dimension coordinates.

$$P = f\left(V_{(SNSVDD)}\right) + \left(\frac{V_{(SNSVDD)}}{R} \times SSPS \times \left[\frac{S \times B}{F} + 3 \times t_{d(PVS)} \right] \right) \quad (13)$$

Use Equation 14 to calculate the power consumption for X-Y 2-dimension touch data.

$$P = f\left(V_{(SNSVDD)}\right) + \left(\frac{V_{(SNSVDD)}}{R} \times SSPS \times \left[\frac{S \times B}{F} + 2 \times t_{d(PVS)} \right] \right) \quad (14)$$

where

- 2 indicates that the X and Y drivers are on

8.2.2.5 Precharge and Sense Time

Unlike the ADC clock frequency (bits CL1 to CL0) and panel voltage-stabilization time (bits PV2 to PV0), the other two TSC timings in the CFR0 register (see Table 6) affect the bus shape and traffic speed but do not effect power consumption of the analog interface.

As shown in Figure 54, some added time or delays occur between samples of two coordinates such as after sampling Y and before the X driver turns on. This added time or delay is the precharge time (bits PR2 to PR0) and sense time (bits SN2 to SN0).

The precharge time sets the amount of time allowed for precharging any pin capacitance on the touch screen during TSC ADC conversions as shown in Figure 55.

The sense time sets the amount of delay for the TSC device to wait between two coordinates during TSC ADC conversions as shown in Figure 56.

If a pressure remains on the touch panel, the TSC devices can automatically and continuously acquire touch data. As many as several-thousand SSPS of touch data can be driven on, sampled, converted, and processed. For a typical application, however, users usually need only 100 to 500 SSPS of touch data because of the control and response limits of a human. To save power, users often do not want the system to acquire any unnecessary data.

The SSPS of a TSC can be reduced in several ways, including:

- Using the batch delay to add waiting time between the sets of touch data
- Inserting delays, such as PR and SN (but not PVS), to slow down the coordinate samples within a set because PR and SN do not consume power

See Table 6 for the bit locations and for the selectable time ranges.

8.2.2.6 Single-Touch Operation

The TSC2013-Q1 device can also be used only for single-touch operation. By measuring all 4-wire nodes (X+, X–, Y+, Y–) more-precise touch accuracy can be achieved compared to normal resistive TSCs.

TI advises to calculate the center point of the touch by using both node values. Equation 15 shows an example.

$$X = 0.5 \times ([X+] - [X-]) + (X+) \quad (15)$$

This same calculation method is used on dual-touch middle-point calculation.

8.2.3 Application Curves

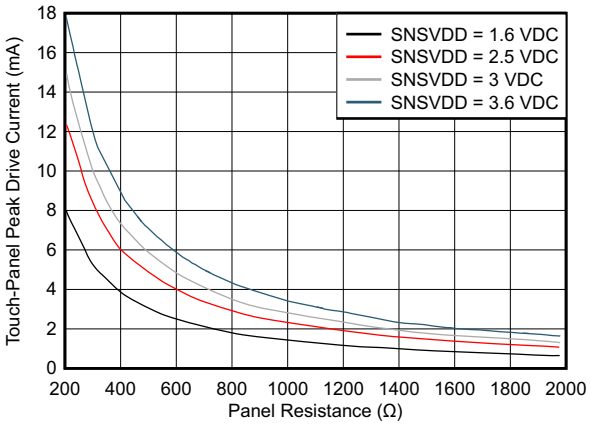


Figure 51. Touch Panel Power Consumption

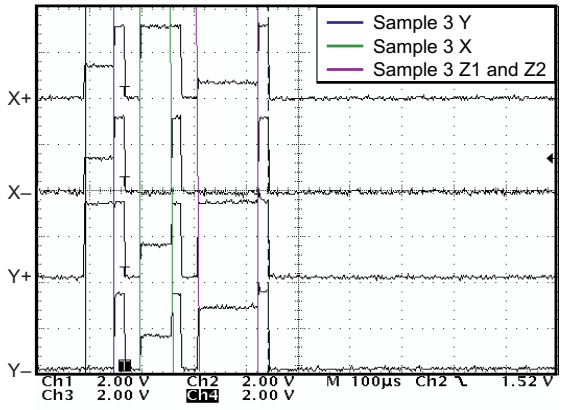


Figure 52. Analog Interface Under ADC Clock = 2 MHz

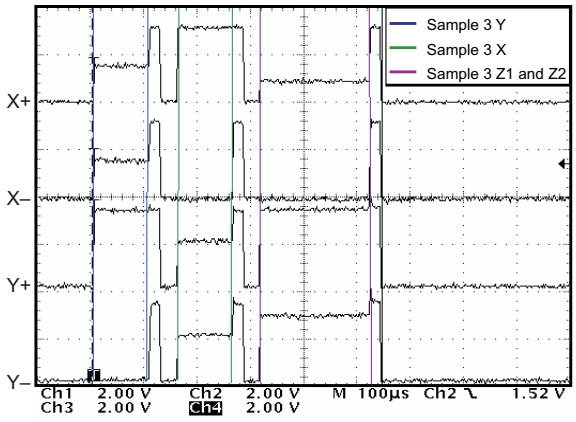


Figure 53. Analog Interface Under ADC Clock = 1 MHz

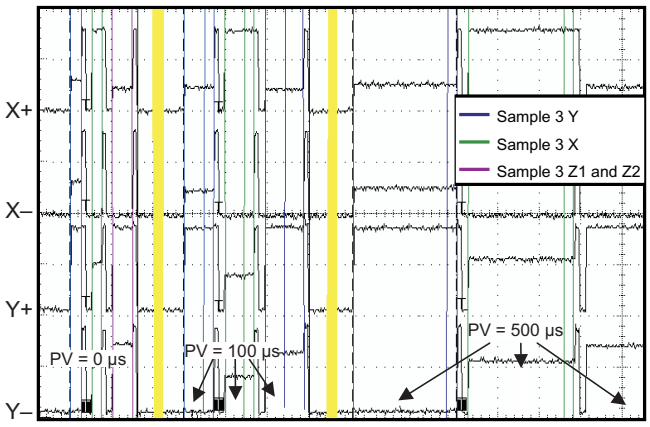


Figure 54. Panel Voltage Stabilization 0 µs, 100 µs, and 500 µs

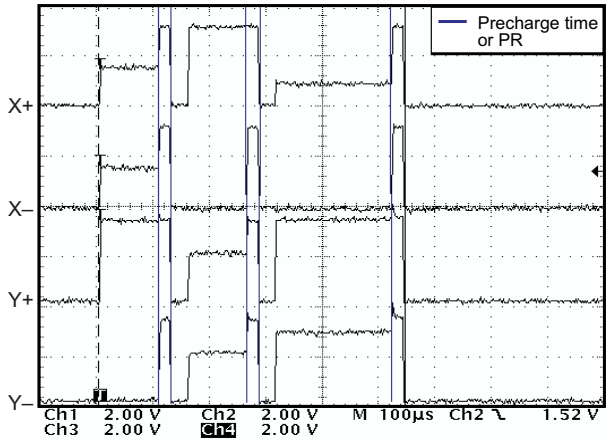


Figure 55. Precharge Time on TSC Analog Interface Lines

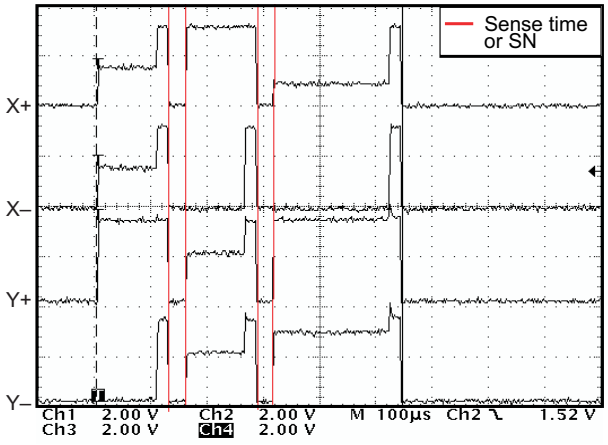


Figure 56. Sense Time on TSC Analog Interface Lines

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 1.6 V and 3.6 V. Power to the TSC2013-Q1 device should be clean and well-bypassed. Add a 0.1-µF ceramic bypass capacitor between (SNSVDD and AGND) or (I/OVDD and AGND).

10 Layout

10.1 Layout Guidelines

The following layout suggestions should obtain optimum performance from the TSC2013-Q1 device. However, many portable applications have conflicting requirements for power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low-power. This situation would mean less bypassing for the converter power and less concern regarding grounding. Still, each application is unique, so review the following suggestions carefully.

For optimum performance, take care with the physical layout of the TSC2013-Q1 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, and ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCL input.

With this in mind, power to the TSC2013-Q1 device should be clean and well-bypassed. Add a 0.1-µF ceramic bypass capacitor between (SNSVDD and AGND) or (I/OVDD and AGND). The circuit also requires a 0.1-µF decoupling capacitor between SNSVDD/VREF and AGND. Place these capacitors as close to the device as possible. The circuit may also require a 1-µF to 10-µF capacitor if the impedance of the connection between SNSVDD/VREF and the power supply is high. Short I/OVDD to the same supply plane as SNSVDD/VREF. Short both SNSVDD/VREF and I/OVDD to the analog power-supply plane.

The ADC architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input, which is of particular concern when the reference input is tied to the power supply for auxiliary input. Any noise and ripple from the supply appears directly in the digital results. While high-frequency noise can be filtered out by the built-in MAV filter, voltage variation as a result of line frequency (50 Hz or 60 Hz) can be difficult to remove. Avoid any active trace going under the analog pins listed in the table without shielding them by a ground or power plane.

Connect the AGND pin to a clean ground point. In many cases, this connection will be the *analog* ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery-connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, take care with the connection between the converter and the touch screen. Because resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch-screen applications (for example, applications that require a backlit LCD panel). This electromagnetic interference (EMI) noise can coupled through the LCD panel to the touch screen and cause flickering of the converted ADC data. On can do several things to reduce this error, such as using a touch screen with a bottom-side metal layer connected to ground, which couples the majority of noise to ground. Another way to filter out this type of noise is by using the TSC2013-Q1 built-in MAV filter (see the section). Filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires longer panel voltage stabilization times, and also increases precharge and sense times for the $\overline{\text{PINTDAV}}$ circuitry of the TSC2013-Q1 device. The resistor value varies depending on the touch-screen sensor used. The internal 50-kΩ pullup resistor ($R_{(IRQ)}$) may be adequate for most sensors.

10.2 Layout Example

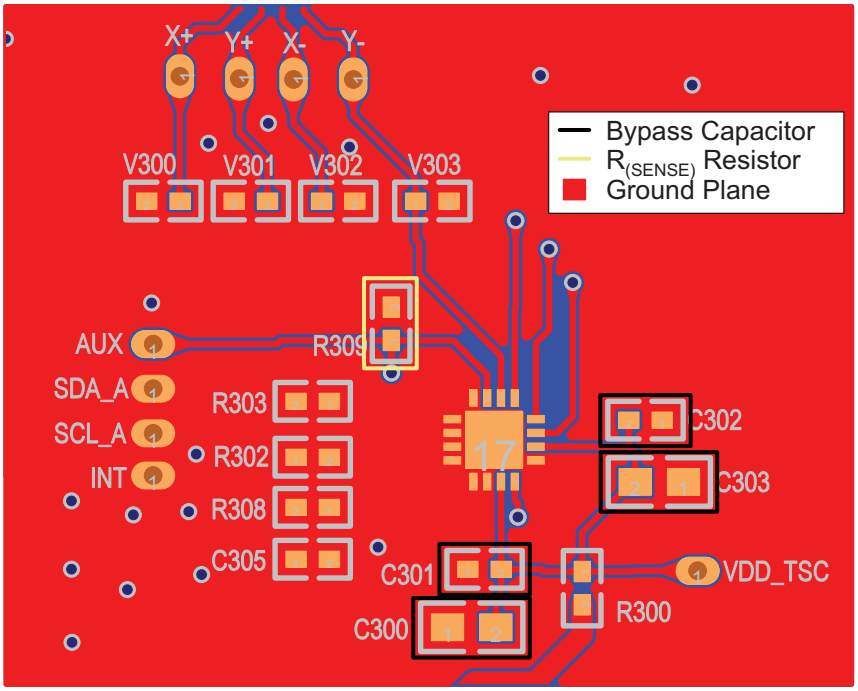


Figure 57. TSC2013-Q1 Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSC2013QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	TS2013Q	Samples
TSC2013QRSARQ1	ACTIVE	QFN	RSA	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSC 2013Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

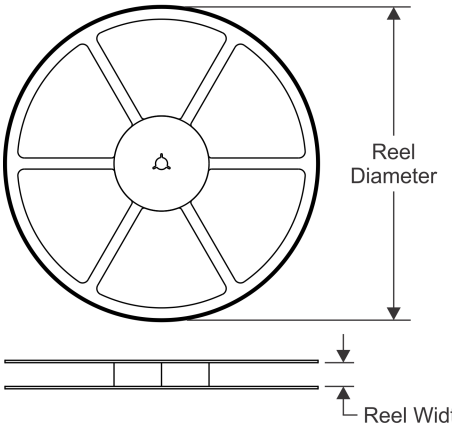
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

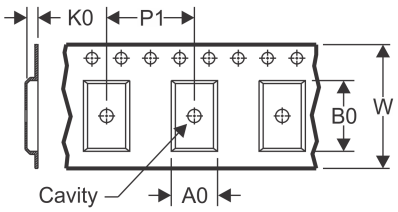
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

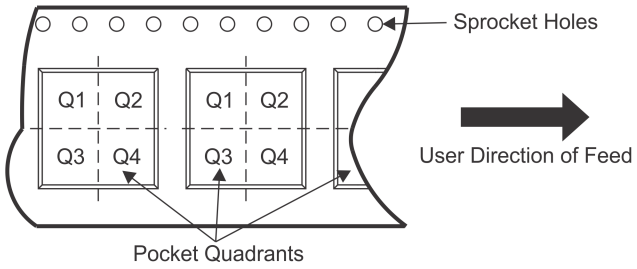


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

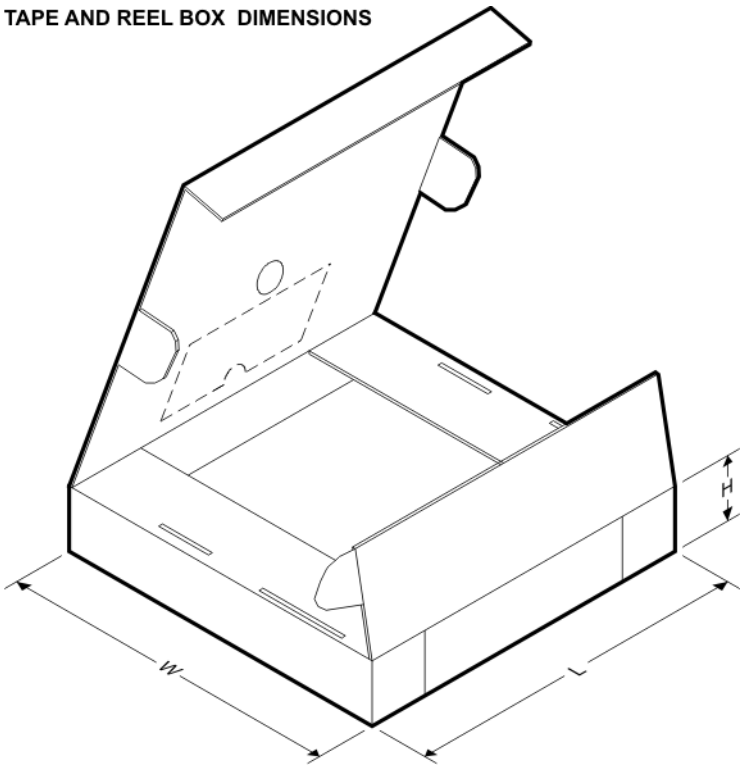
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2013QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSC2013QRSARQ1	QFN	RSA	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

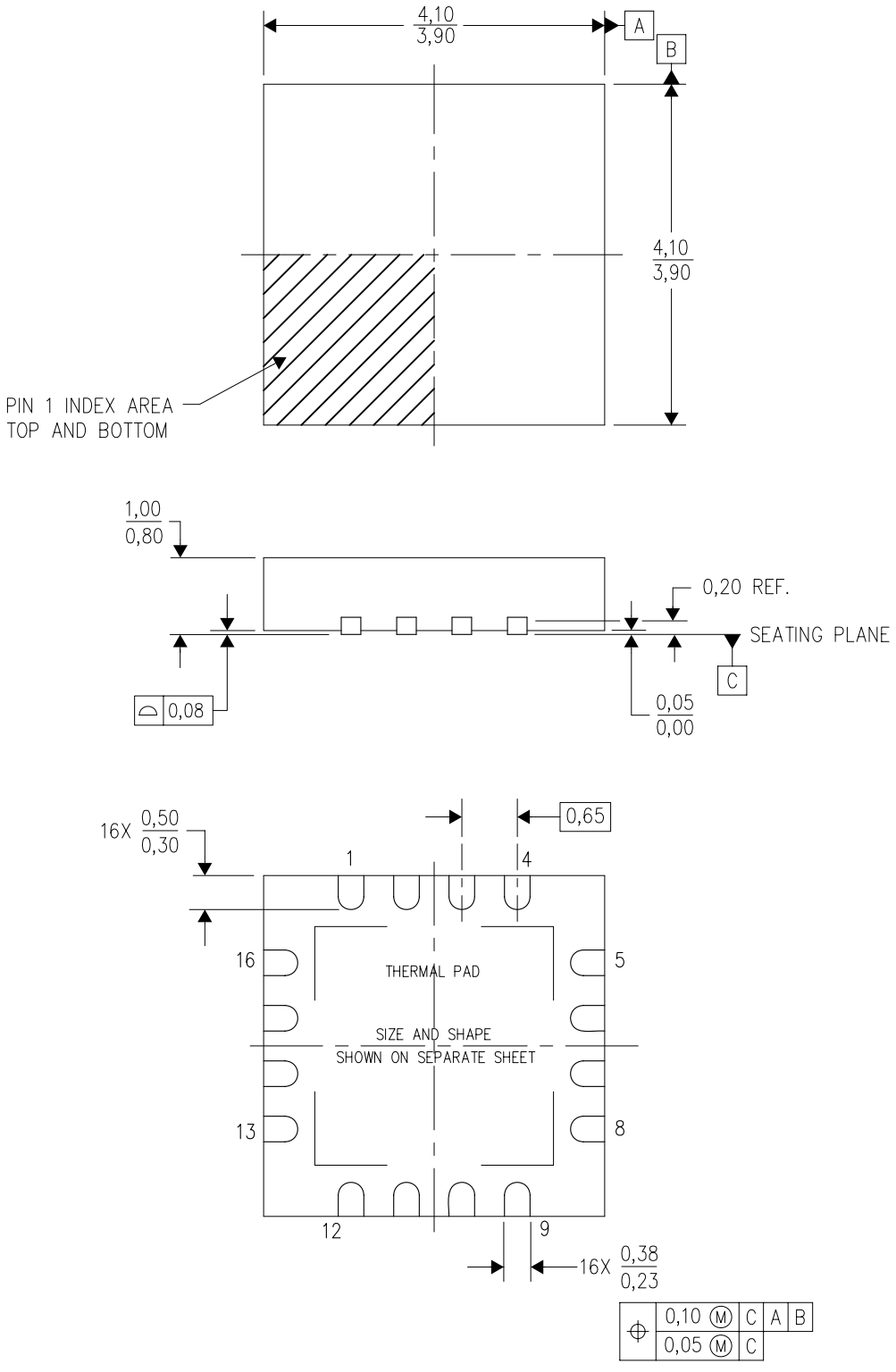
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2013QPWRQ1	TSSOP	PW	16	2000	350.0	350.0	43.0
TSC2013QRSARQ1	QFN	RSA	16	2500	367.0	367.0	35.0

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

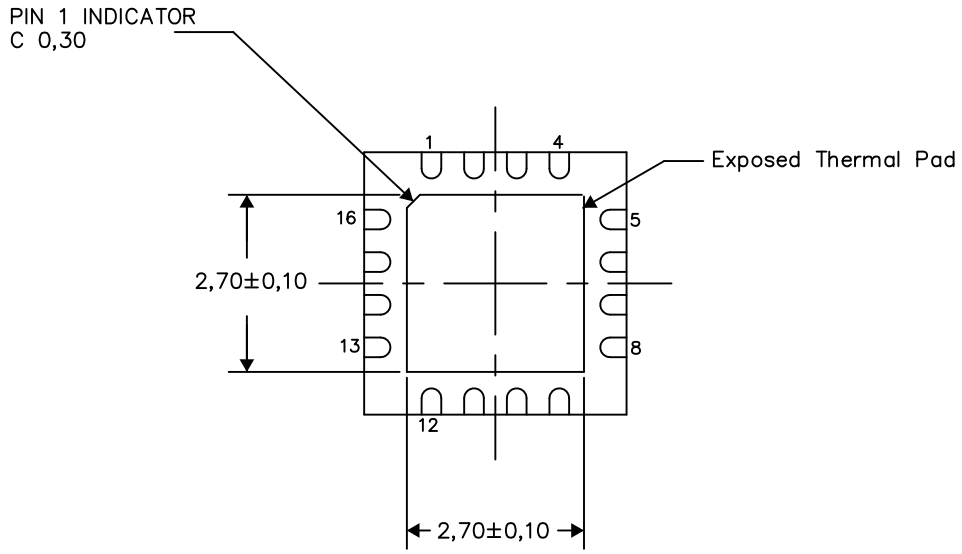
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



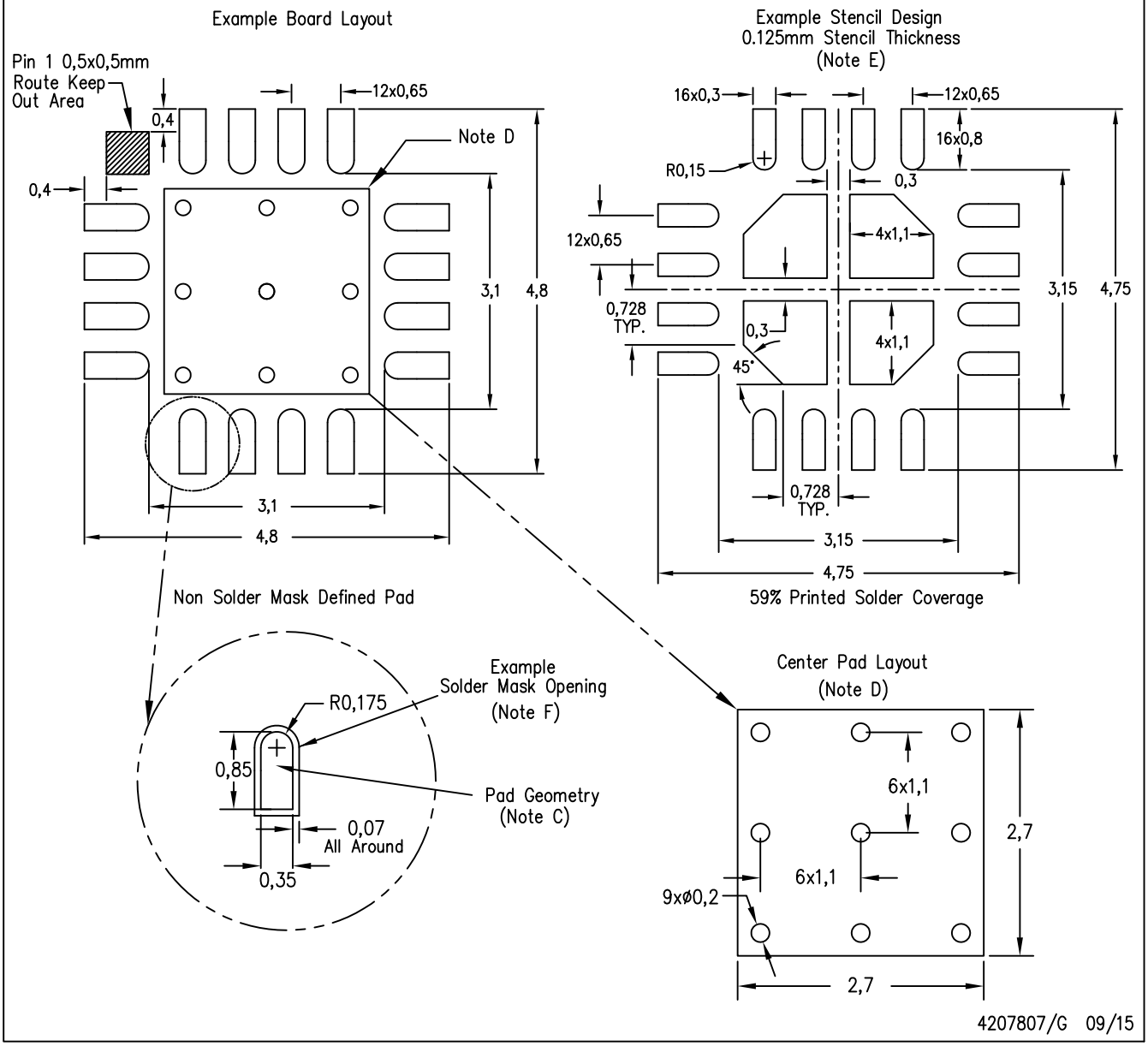
Bottom View

Exposed Thermal Pad Dimensions

4206364–2/0 09/15

NOTES:
A. All linear dimensions are in millimeters

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



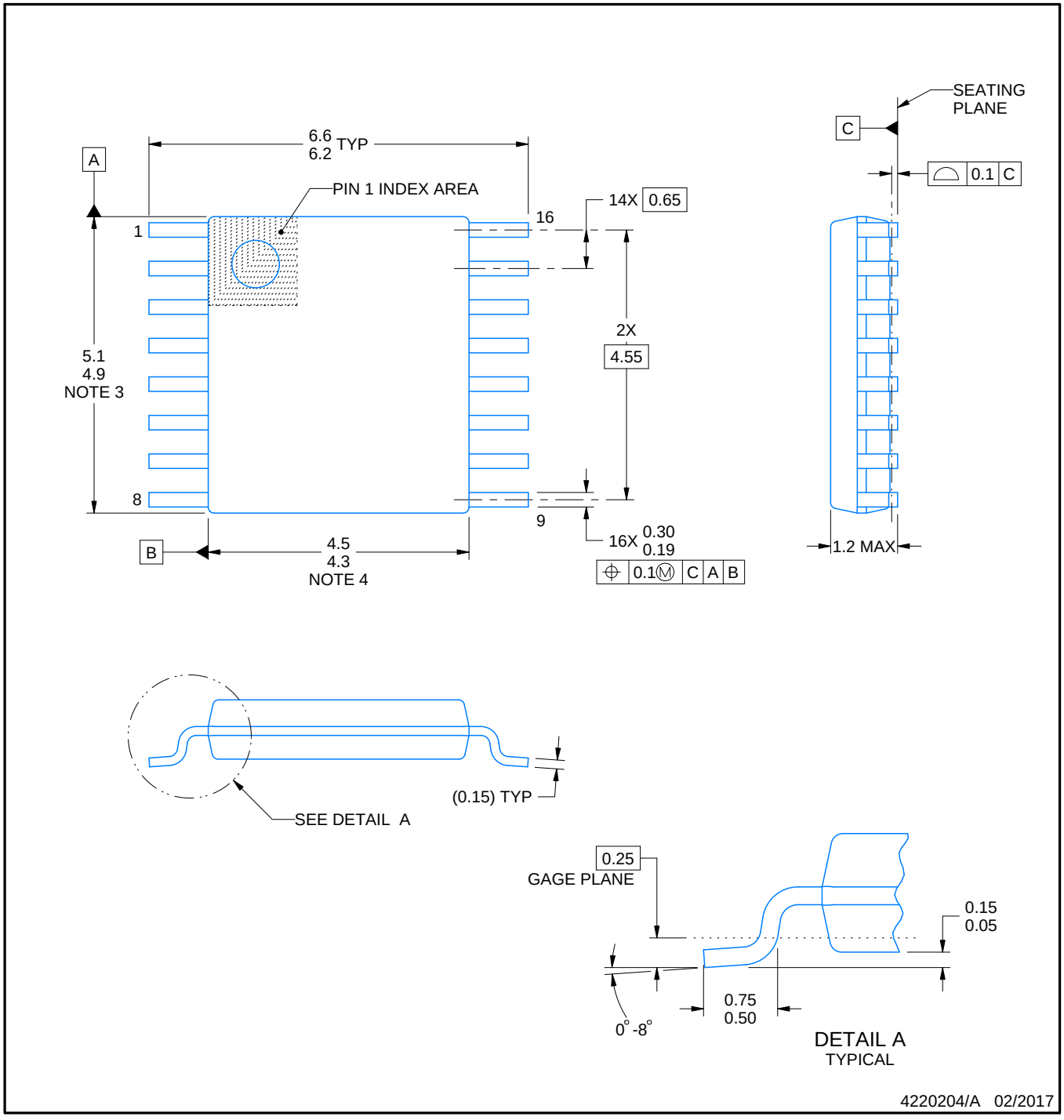
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

PACKAGE OUTLINE

PW0016A

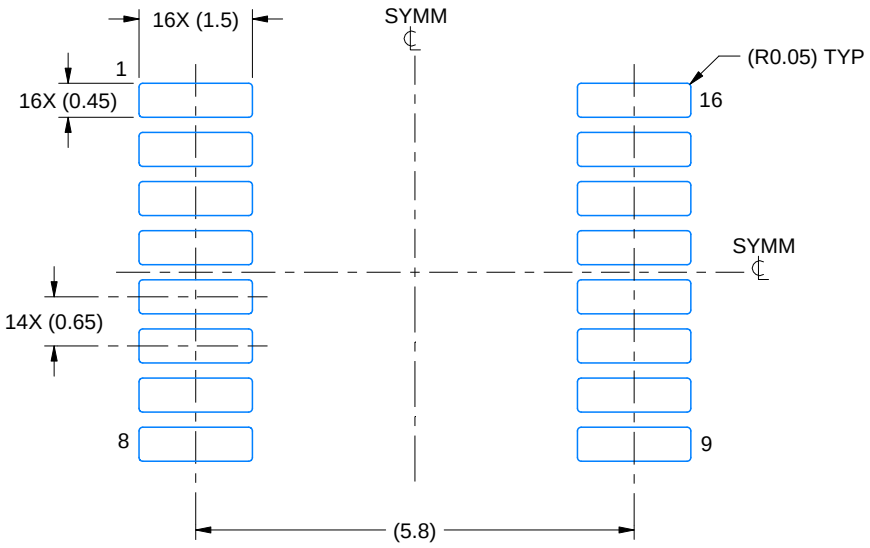
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

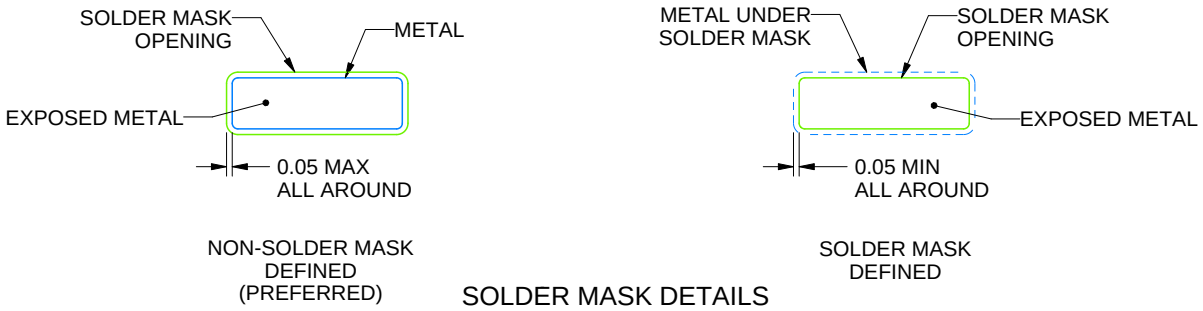


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

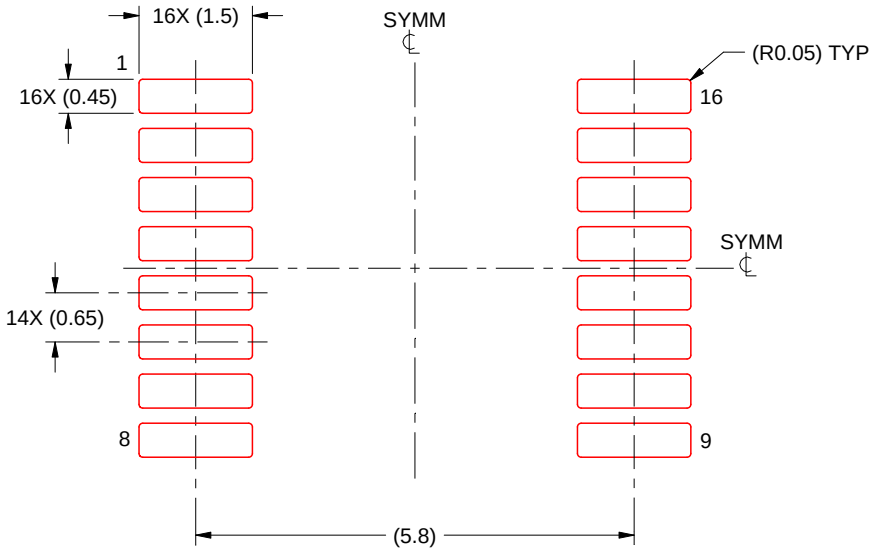


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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