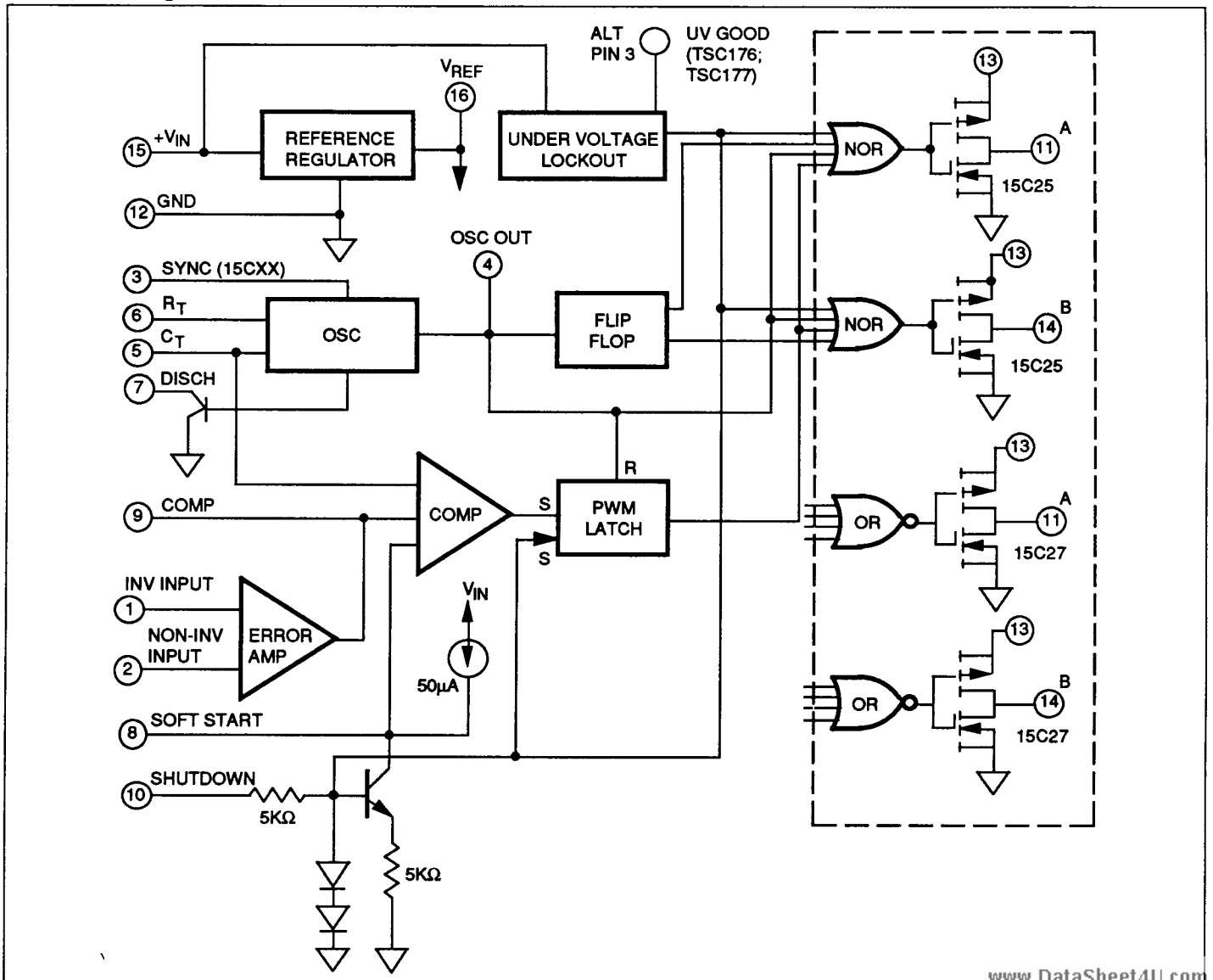


## BICMOS PWM CONTROLLERS

### Features

- High Voltage .....35V Input
- Low Power BICMOS Construction
- Low Supply Current .....1.0mA Typ
- Latch Up Immunity .....> 500 mA on Outputs
- Above and Below Rail Input Protection.....±5V
- High Output Drive .....500 mA Peak
- Fast Rise/Fall Time .....50 nS @ 1000pF
- High Frequency Operation .....Up To 700kHz
- Tri-state R, Pin For Easy Parallel Operation
- UV Hysteresis Guaranteed
- Shutdown Pin Available
- Double Ended
- Soft Start, With Small Cap
- Low Prop Delay Shutdown to Output .....140nS Typ
- 2KV ESD Protection

### Functional Diagram



TSC176  
TSC15C25A  
TSC25C25A  
TSC35C25A

TSC177  
TSC15C27A  
TSC25C27A  
TSC35C27A

### General Description

The TSC35C25A/35C27A family of PWM controllers are CMOS implementations of the industry standard voltage mode ICs.

As well as offering power consumption 10 times less than the industry standard this family offers improved output drive, latch proof operation, input protection 5 volts below the negative rail and improved propagation delay.

Unlike first generation CMOS PWM ICs, this family of devices can be operate from two separate power supplies, one for the output stage and one for the control section. This allows "bootstrap" operation of the IC. The CMOS output stage allows the output voltage swing to come within 25mV of either rail.

A tri-state feature has been added to systems requiring multiple power supplies. When R<sub>T</sub> pin is pulled to +5V, the IC can be driven by an external pulse, allowing external control of frequency and dead time. Use this for master/slave or parallel/redundant configurations. Low 10μA sync current makes this easy.

Other improved features are tightened hysteresis and UV start up points that are specified over temperature, and low input bias currents on all inputs making these devices especially useful for high voltage supplies. An internal 35 volt zener diode on the input is available as a clamp for those applications where external clamps are not available.

To use these PWM in place of older bipolar versions it should be noted that the oscillator ramp is 3V, not 4V, and that a different RC is required. Also the voltage reference is 4V, not 5V.

### Ordering Information

Part No	Configuration	Pkg./Temperature
TSC35C25ACOE	Non-Inverting	16-Pin SOIC (wide) 0 to 70°C
TSC35C25ACPE	Non-Inverting	16-Pin Plastic DIP 0 to 70°C
TSC35C25ACL P	Non-Inverting	20-Pin Plastic LCC 0 to +70°C
TSC35C27ACOE	Inverting	16-Pin SOIC (wide) 0 to 70°C
TSC35C27ACPE	Inverting	16-Pin Plastic DIP 0 to 70°C
TSC35C27ACL P	Inverting	20-Pin Plastic LCC 0 to 70°C

### Ordering Information

Part No.	Configuration	Pkg./Temperature
TSC15C25AMJ	Non-Inverting	16-Pin CerDIP -55 to +125°C
TSC15C25AMNP	Non-Inverting	20-Pin LCC -55 to +125°C
TSC15C27AMJE	Inverting	16-Pin CerDIP -55 to +125°C
TSC15C27AMNP	Inverting	20-Pin LCC 16-pin -55 to +125°C
TSC176COE	UV Pin, Non-Inverting	16-Pin SOIC (wide) 0 to +70°C
TSC176CPE	UV Pin, Non-Inverting	16-Pin Plastic DIP 0 to 70°C
TSC176EOE	UV Pin, Non-Inverting	16-Pin SOIC (wide) -40 to +85°C
TSC176EPE	UV Pin, Non-Inverting	16-Pin Plastic DIP -40 to +85°C
TSC176MJE	UV Pin, Non-Inverting	16-Pin CerDIP -55 to +125°C
TSC177COE	UV Pin, Inverting	16-Pin SOIC (wide) 0 to 70°C
TSC177CPE	UV Pin, Inverting	16-Pin Plastic DIP 0 to +70°C
TSC177EOE	UV Pin, Inverting	16-Pin SOIC (wide) -40 to +85°C
TSC177EPE	UV Pin, Inverting	16-Pin Plastic DIP -40 to +85°C
TSC177MJE	UV Pin, Inverting	16-Pin CerDIP -55 to +125°C
TSC25C25AE OE	Non-Inverting	16-Pin SOIC (wide) -40 to +85°C
TSC25C25AEPE	Non-Inverting	16-Pin Plastic DIP -40 to +85°C
TSC25C25AEJE	Non-Inverting	16-Pin CerDIP -40 to +85°C
TSC25C27AE OE	Inverting	16-Pin SOIC (wide) -40 to +85°C
TSC25C27AEPE	Inverting	16-Pin Plastic DIP -40 to +85°C
TSC25C27AEJE	Inverting	16-Pin CerDIP -40 to +85°C

## PRELIMINARY INFORMATION

TSC176  
TSC15C25A  
TSC25C25A  
TSC35C25A

TSC177  
TSC15C27A  
TSC25C27A  
TSC35C27A

Electrical Characteristics:  $V_+ = 16V$ ,  $T_{AMP} = 25^\circ C$ ,  $R_T = 5K\Omega$ ,  $R_D = 100\Omega$ ,  $C_T = 1000pF$  (See test circuit)

PARAMETER	NOTES 1, 2	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Reference Section</b>						
Output Voltage		@ 1mA	3.95	4	4.05	V
Line Regulation	*	$V_{IN} = 8$ to 18V		5	10	mV
Load Regulation	*	$I_L = 1$ to 20mA		4	20	mV
Temperature Stability		Oper Temp Range		20	50	mV
Total Variation		Line, Load, Temp	3.85	4	4.15	V
Long Term Stability		$T_J = 125^\circ C$		1	10	mV/1KHrs
Short Circuit Current		$V_{REF} = 0$		50	100	mA
Output Noise		$10Hz \leq f \leq 10KHz$		40	200	$\mu VRMS$
Output Impedance		10Hz (See Graph)	0.2	0.25	0.5	$\Omega$
<b>Oscillator</b>						
Initial Accuracy	*	@ 95KHz		$\pm 2$	$\pm 3$	%
Voltage Stability		$V_{IN} = 8$ to 16V		0.5	1	%
Temperature Stability		Oper Temp Range		$\pm 3$	$\pm 6$	%
Charge Current Range	+	$R_T = 3K\Omega$ to 300K $\Omega$	100:1			
Max Cap Reset Transistor		$R_{DS(ON)} = 0\Omega$	40	47	75	$\Omega$
Osc Output Amplitude		$f = 100KHz$ , $R_L = 1M\Omega$	5.9	6	6.1	V
Osc Output Min Width	*	$R_D = 27\Omega$	130	160	230	nS
Sync Threshold		$R_T$ pin tied to +6V, $C_T$ pin at GND	0.8	1.3	1.6	V
Sync Input Current		Sync Voltage = 3.5V			10	$\mu A$
Min Sync Pulse Width	+	Sync Voltage = 5V	190	200	230	nS
Max Osc Freq	*	$R_T = 1K$ , $C_T = 200pF$ , $R_{DIS} = 20\Omega$	790	810	840	KHz
<b>Error Amplifier (<math>V_{CN} = 2.5V</math>)</b>						
Input Offset Voltage				5	15	mV
Input Bias Current	*			0.2	0.5	$\mu A$
Input Offset Current	*			100	500	pA
DC Open Loop Gain	*	$R_L = 100K\Omega$	80	90		db
Gain Bandwidth Product		$A_V = 0db$	0.7	0.9	1.2	MHz
Output Low Level	*	$R_L = 100K\Omega$ (N Channel)		0.01	0.05	V
Output High Level		$R_L = 100K\Omega$ (NPN)	5	5.4		V
CMRR		$V_{CN} = 0.5$ to 4.7V	60	75		db
Supply Voltage Rejection	*	$V_{IN} = 8$ to 18V	90	100	120	db
<b>PWM Comparator</b>						
Min Duty Cycle					0	%
Max Duty Cycle		$f = 100KHz$	45	49		%
Input Threshold		Zero Duty Cycle		0.6		V
Input Threshold		Max Duty Cycle	3	3.3	3.6	V
Input Bias Current	*			0.05	0.1	$\mu A$
<b>Soft Start Section</b>						
Soft Start Current	*	$V_{SHUTDOWN} = 0V$	38	46	55	$\mu A$
Soft Start Voltage		$V_{SHUTDOWN} = 2V$	0.2	0.25	0.5	V
Shutdown Input Current	*	$V_{SHUTDOWN} = 2.5V$		0.5	1	$\mu A$
Min Shutdown Pulse Width	+	$V_{SHUTDOWN} = 5V$	45	50		nS
Shutdown Delay	*	$V_{SHUTDOWN} = 5V$	130	140	170	nS

# BICMOS PWM CONTROLLERS

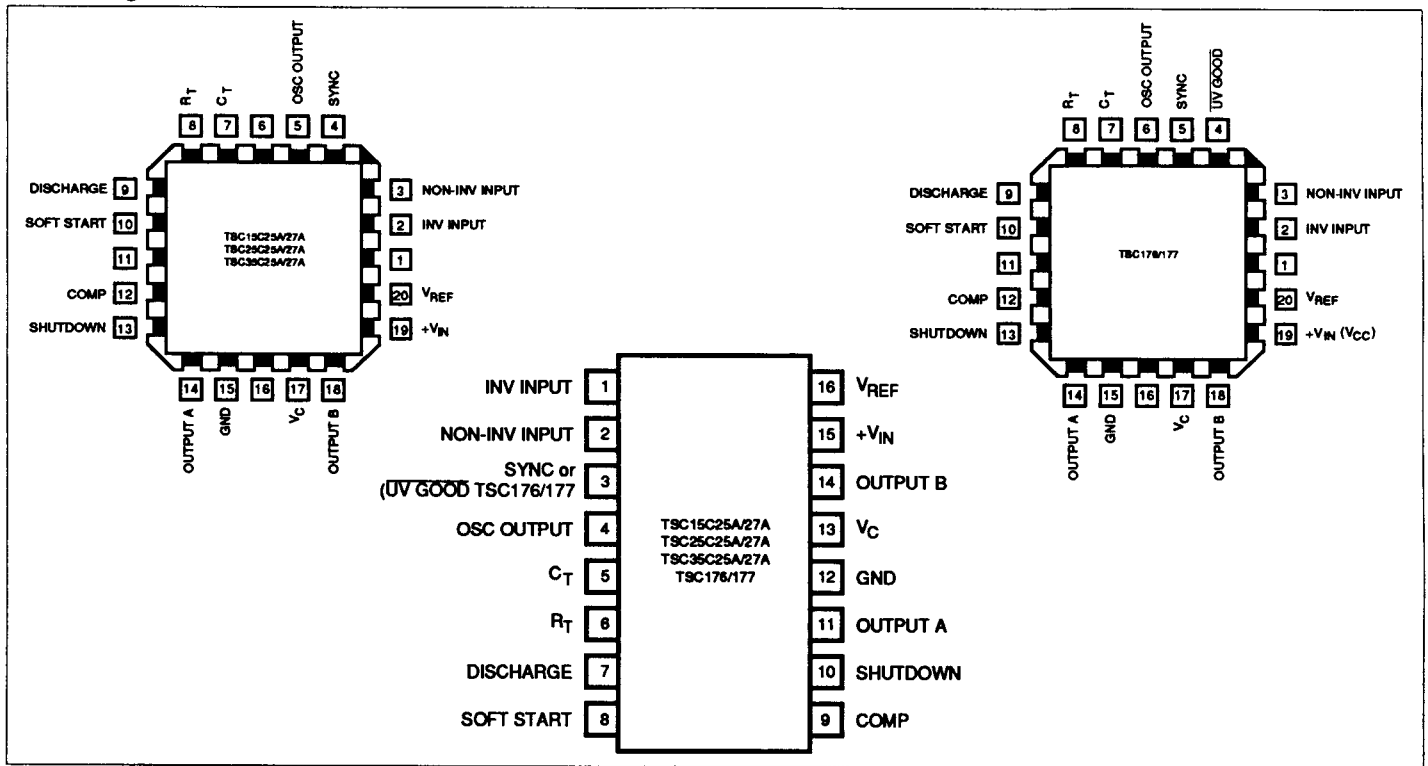
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**TSC35C25A**

**TSC177**  
**TSC15C27A**  
**TSC25C27A**  
**TSC35C27A**

PARAMETER	NOTES 1, 2	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Output Drivers (each output)</b>						
Output Low Level		$R_{DS(ON)}$		17	22	$\Omega$
Output High Level		$R_{DS(ON)}$		10	15	$\Omega$
Rise Time		$C_L = 1KpF$	50	100	150	nS
Fall Time		$C_L = 1KpF$	50	100	150	nS
<b>Power Supply</b>						
Supply Current		$f = 100KHz$ (See Test Circuit)		1	1.8	mA
UV Lockout		Pins 8 and 9 to $V_{REF}$	6.65	6.85	7.05	V
UV Lockout Hysteresis			0.3	0.65	0.8	V

**NOTES:** 1. \*Improved specification.  
 2. +Added specification.

## Pin Configurations



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