DATA SHEET

HIGH-FIDELITY HEADPHONE AMPLIFIER

TSDP1xx

DESCRIPTION

The TSDP1xx is a Cap less Direct Connect™ Ground-Referenced Output Headphone amplifier with independent left/right volume and GPIO control. It provides high quality audio fidelity with SNR of 105dB and output power of 180mW per channel. The differential inputs allow for flexible input configuration that maximizes noise rejection for best in class CMRR.

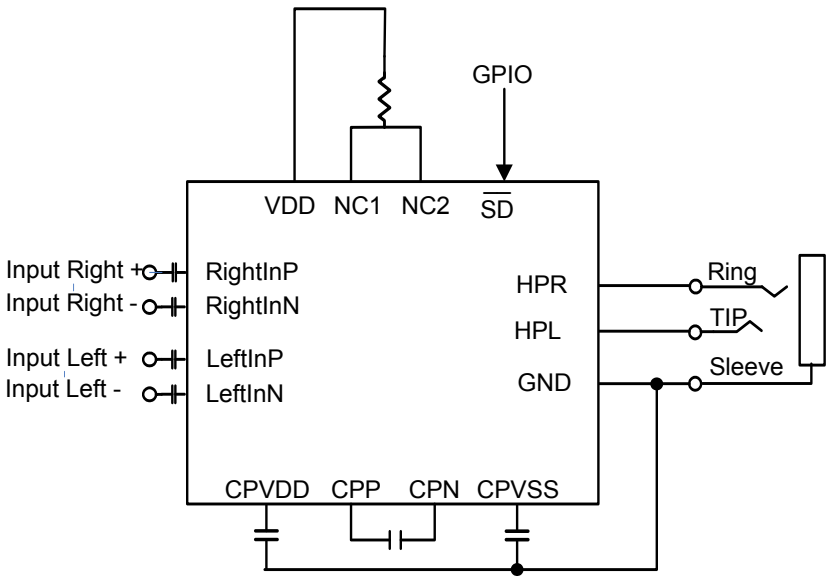
TARGET APPLICATIONS

- **Tablets**
- **Mobile Phones**
- **Stereo Audio Headsets**
- **Notebook Computers**
- **High Fidelity Audio Applications**

FEATURES

- **The Class H TSDP1xx Capless DirectConnect™ Feature**
  - Eliminates Large Output DC Blocking Capacitors
  - Reduces Board Area
  - Reduces Component Height and Cost
  - Full Bass Response Without Attenuation
  - No Pop on start-up or power-down
  - SNR of 105dB
  - Reduced BOM Cost
  - Class H reduces power consumption by as much as 45% at typical listening levels
  - Low Quiescent Current
  - 180mW Per Channel into 16Ω
  - Charge-pump allows for true ground centered outputs
- **Independent Left/Right Volume and Mute Control**
- **Power Supply Voltage Range: 2.5 V to 5.5 V**
- **High Power Supply Rejection Ratio (>100 dB PSRR)**
- **Differential Inputs for Maximum Noise Rejection Ratio (90 dB CMRR)**
- **Optional register controlled High-Impedance Outputs When Disabled**
- **GPIO Control for Hardware Shutdown**
- **Advanced Finer Control via Register control**
- **20 Pin, 4 mm x 4 mm QFN RoHS Package**

FUNCTIONAL DIAGRAM



1. PRODUCT OVERVIEW

The TSDP1xx stereo Class H Capless DirectConnect™ headphone amplifier is optimally designed for portable applications. The GPIO control allows the device to be put in a low power shutdown mode. The TSDP1xx is a high fidelity amplifier with SNR of 104dB. With a PSRR greater than 90dB. The TSDP1xx can be connected directly to a battery without compromising the listening experience. The output noise of 6.3μVrms (typical *A-weighted*) provides a minimal noise background during periods of silence. Configurable differential inputs and high CMRR allow for maximum noise rejection in the noisy mobile environment.TSDP1xx is available in a 4x4mm QFN package. The TSDP1xx stereo headphone DirectConnect™ architecture eliminates the large output coupling capacitors typically required for single-supply headphone drivers. The device consists of two 210mW Class AB headphone drivers, supply controlled with Class H charge-pump, shutdown control, and comprehensive click-and-pop suppression circuitry. The charge pump uses VREG to create a positive supply (CPVDD) and inverts VREG to create a negative supply (CPVSS). The headphone drivers operate from these bipolar supplies with their outputs biased around GND. The drivers have almost twice the supply range compared to other 3V/5V single-supply drivers, increasing the available output power. Additionally, by being biased around physical GND, the typical power-on pops and clicks are eliminated.

The benefit of this GND bias is that the driver outputs do not have the typical VDD/2 DC component. The large DC-blocking capacitors are unnecessary, thus improving frequency response while conserving board space and system cost. Each channel has independent left/right, software controlled gain and mute, this makes it possible to optimize power savings and click-and-pop suppression in mixed-mode operation, mono/stereo click-and-pop suppression that eliminates audible transients on startup and shutdown. Additionally, the TSDP1xxfeatures thermal overload and short-circuit protection.

2. DETAILED BLOCK DIAGRAMS

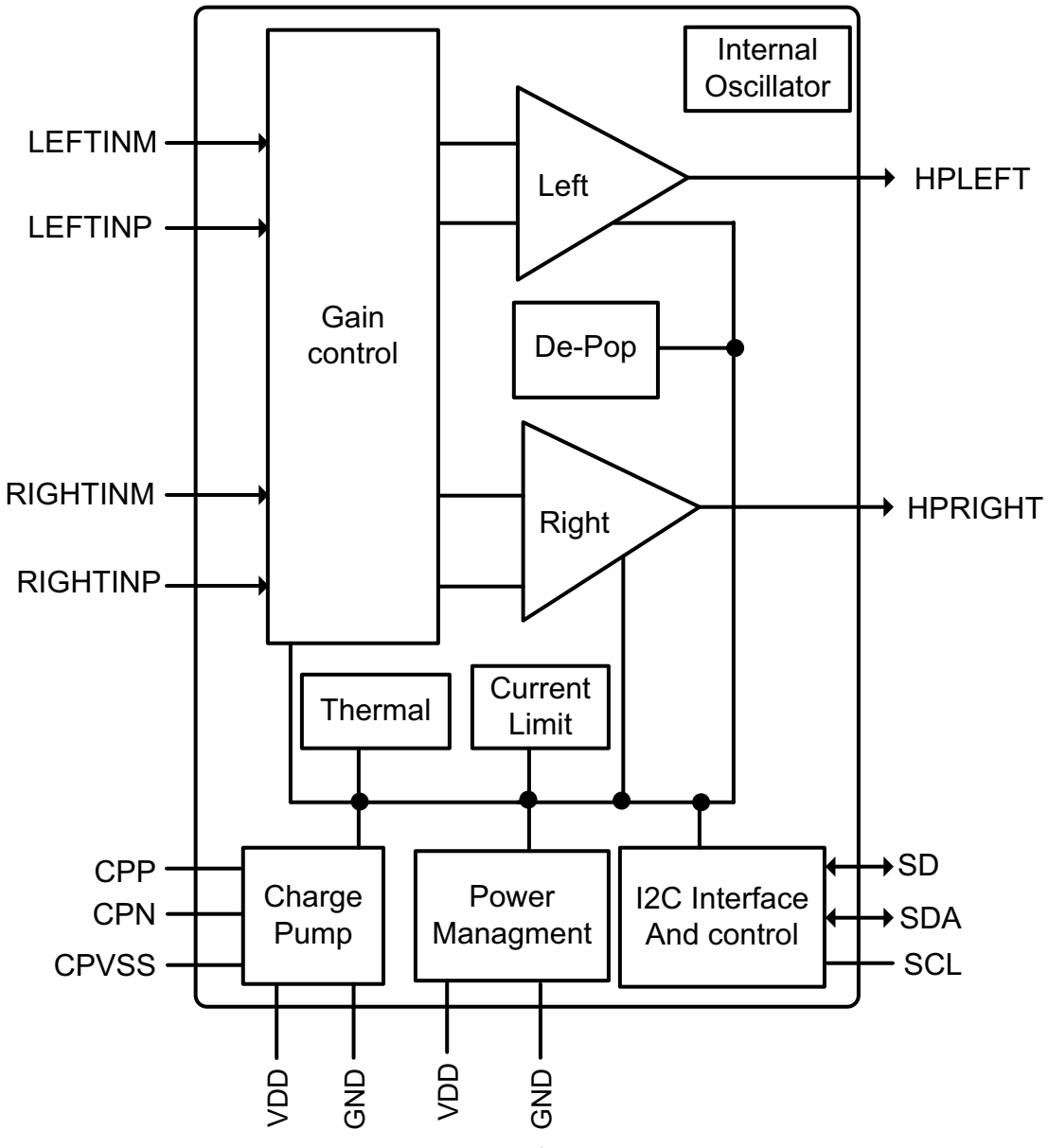


Figure 1. Block Diagram

3. FUNCTION DESCRIPTION

3.1. Internal Oscillator

The TSDP1xx uses an internal oscillator to generate a master reference clock. This clock is used to run the charge pump, anti-pop circuitry monitor the chip temperature sensor and shutdown circuitry. The oscillator runs at 830kHz(typical).
The internal oscillator can be varied with register control. The adjustment of frequency can be done with registers if needed.

3.1.0.1. Oscillator Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 22 SELF_OSC_CTRL1 (15Ch)	7:6	SELFOSC_DIV CLK_SEL	RW	0h	Selects the initial divider from the selfosc input clock to be used for the chopping clock & apopclock setting
	5:4	SELFOSC_VC HP_SEL	RW	0h	Selects the divider from the selfosc input clock to be used for the Charge Pump clock setting
	3:0	SELFOSC_FRE Q_SEL	RW	5h	Selects the desired output frequency setting

3.1.0.2. Oscillator *Control Register*

Register Address	Bit	Label	Type	Default	Description
Reg 23 SELF_OSC_CTRL2 (16h)	7:5	RESERVED	RO	0h	Reserved
	4	SELFOSC_PW D	RW	0h	Powers down (i.e. when high) the self oscillator circuitry
	3	SELFOSC_RST B	RW	1h	resets (i.e. when low) the dflops in the divider circuitry
	2	SELFOSC_CH PRCLK_PWDB	RW	0h	Powers down (i.e. when low) the chopping clock output
	1	SELFOSC_AP OPCLK_PWDB	RW	1h	Powers down (i.e. when low) the antipop clock output (i.e. also used for tempsensor)
	0	SELFOSC_AP OPCLK_SEL	RW	0h	Selects the desired output frequency for the apopclock setting

4. AUDIO INPUTS

The TSDP1xx provides differential audio analog inputs

4.1. Headphone/ DirectConnect™

Single-supply headphone drivers traditionally have their outputs biased about a half the nominal DC voltage for maximum dynamic range. In other words, to block the DC bias, large capacitors are needed to couple the signal to the headphone driver. Without these capacitors, wasted large DC current will unnecessarily flow to the headphone speaker, and possibly damage both headphone driver and/or speaker. The Capless DirectConnect™ architecture uses charge pump to create an internal negative supply. This allows the outputs of the TSDP1xx to be centered around GND. In addition, the creation of the negative internal supply doubles the dynamic range while operating from a single supply. With the ground (GND) reference, there is no need for the large DC-blocking capacitors. Instead of two large very linear capacitors that can be as much as 220μF (often tantalum capacitors for linearity), the TSDP1xx charge pump requires four small value capacitors. This reduces board space and BOM cost, while improving the frequency response of the headphone driver.
The HPR/HPL pins can drive a 16Ω, 32Ω headphone load or line output load up to 10KΩ without any external components. The signal volume of the headphone amplifier volume can be independently adjusted under software control by writing to HPVOL_L and HPVOL_R. Also setting the volume to 00000 will power down amp.The amplifier can be set to mute by enabling the mute register or setting the volume to 00010.The output remains at ground, so that no click noise is produced when muting or un-muting. Gains above 0dB run the risk of clipping large signals.

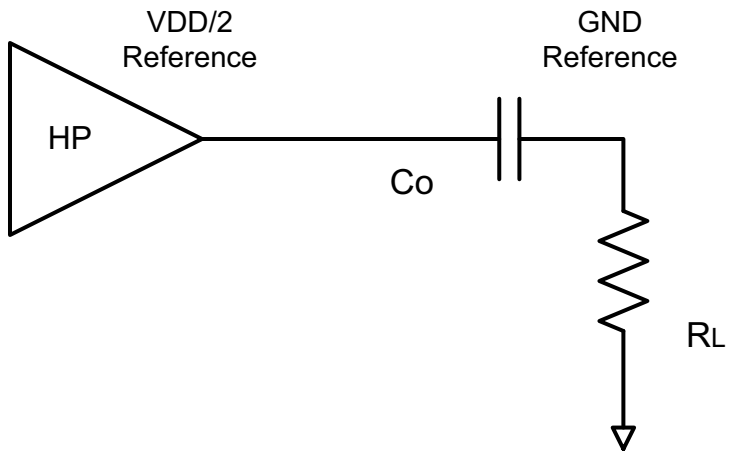


Figure 2. conventional headphone amplifier connection to the headphone jack and output signal diagram

4.1.1. Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, the output signal is severely clipped, and large amounts of dc current rush through the headphones, potentially damaging them. The functional diagram shown above illustrates the conventional headphone amplifier connection to the headphone jack and output signal. DC blocking capacitors are typically large in value to avoid attenuation of Bass (or low frequency) content. The headphone speakers (typical resistive values of 16Ω or 32Ω) combine with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between
the load impedance (RL), the capacitor (CO), and the pass frequency (fC).

$$F_c = \frac{1}{2\pi * R_L * C_0} \quad (1)$$

C_O can be determined from (1), where the load impedance and the cutoff frequency are known thus:

$$C_0 = \frac{1}{2\pi * R_L * F_C} \quad (2)$$

If f_c is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

4.1.2. Volume Control

The TSDP1xx features two independent controls for left/right volume ranging from +6dB to -22dB and mute. Changes in volume are walked automatically to the new target volume using an advanced pop suppression circuitry which eliminates unwanted audio pops and clicks at the output.

Channel volume can be controlled across a gain and attenuation range of -22dB to +6dB (1.0dB steps). The level of attenuation is specified by 5-bit code 'VOL_x', where 'x' is L, or R. The value 00010" indicates mute; other values describe the number of 1.0dB steps above -22dB.

4.1.2.1. Volume Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 19 HDPH_CTR2((12h)	7	RESERVED	RW	0	Reserved
	6	HP_DISCHOP_ANTIPOP	RW	1	Disables the chopping for antipop when high. Only turns chopping at power up/down (i.e. code 1) on when both d2a_dischop_antipop low and d2a_dischop_amp is high.
	5	HP_DISCHOP_AMP	RW	1	Will enable chopping always when low and disable chopping when high.
	4:0	HP_CNT_TARGET_L	RW	10	Sets the left channel final target gain for the anti-pop ramping circuitry (00000==> pwd,00010==> mute,00011==> -22.8919dB, 10000b==> 0dB, 10100b ==> +2dB, 11001b ==> +4dB, 11111b ==> +6dB)
Reg 20 HDPH_CTRL3(13h)	7	RESERVED	RW	0	Reserved
	6	RESERVED	RW	0	Reserved
	5	RESERVED	RW	0	Reserved
	4:0	HP_CNT_TARGET_R	RW	10	Sets the right channel final target gain for the anti-pop ramping circuitry (10000b==> 0dB, 10100b ==> +2dB, 11001b ==> +4dB, 11111b ==> +6dB)

4.1.3. Current Limiter

Advanced short-circuit protection protects amplifier outputs from shorting conditions

To avoid damage to the outputs if a short circuit condition should occur, the headphone amplifier implements a current limiter protection circuits. The headphone output amplifier will detect the load current and limit its output if in an over current state.

Register Address	Bit	Label	Type	Default	Description
Reg 18 HDPH_CTRL1(11h)	7:6	HP_ILIM	RW	3h	Sets the current output limit for the headphones (i.e. 00b ==> powerdown, 01b ==> ~ 100mA, 10b ==> ~150mA, 11b ==> ~200mA)
	5	HPL_PWD	RW	0h	Left Headphone power down
	4	HPR_PWD	RW	0h	Right Headphone power down
	3	RESERVED	RW	0h	Reserved.
	2	RESERVED	RW	0h	Reserved.
	1	HPL_MUTE	RW	0h	Left Headphone mute (sets ampfiier to unity gain with postive differential input set to GNDA)
	0	HPR_MUTE	RW	0h	Right Headphone mute (sets ampfiier to unity gain with postive differential input set to GNDA)

4.1.4. Anti-pop Circuit

Advanced anti-pop circuit prevents amplifier outputs from creating audible pop conditions

4.1.4.1. Click and Pop

Due to the nature of power management and audio path configurability, many situations will introduce undesirable sounds. It is not possible to prevent loud pops in all situations, but it is desired to prevent pops under many situations.The headphone should be fully powered down prior to removal of VDD

State Change	Description	Desired (dBV Awt)
Application of VDD	Headphone Output 10K-ohm load	-65
Application of VDD	Headphone Output 32-ohm load	-65
Removal of VDD	Headphone Output 10K-ohm load	-65
Removal of VDD	Headphone Output 32-ohm load	-65

Table 1.

4.1.4.2. Anti Pop Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 21 HDPH_CTRL4(14h)	7	RESERVED	RW	0h	Reserved
	6	RESERVED	RW	0h	Reserved
	5	RESERVED	RW	1h	Reserved
	4	HP_OUTGND_REG	RW	0h	Register used to control the headphone output grounding switch when d2a_hp_outgnd_ovrd is set high
	3	HP_OUTGND_OVRD	RW	0h	Over rides (i.e. when high) the antipop ramping control of the headphone output grounding switch with value from "d2a_hp_outgnd_reg"
	2	RESERVED	RW	0h	Reserved
	1	RESERVED	RW	0h	Reserved
	0	HP_CONNECT_GND_VAG	RW	1h	Turns on switches (i.e. when high) at the differential inputs to reference inputs to ground (i.e. DC blocking caps cause inputs to need reference). This was mainly added incase we needed to tristate inputs for Global Headset functionality.

4.1.5. Short-Circuit Protection

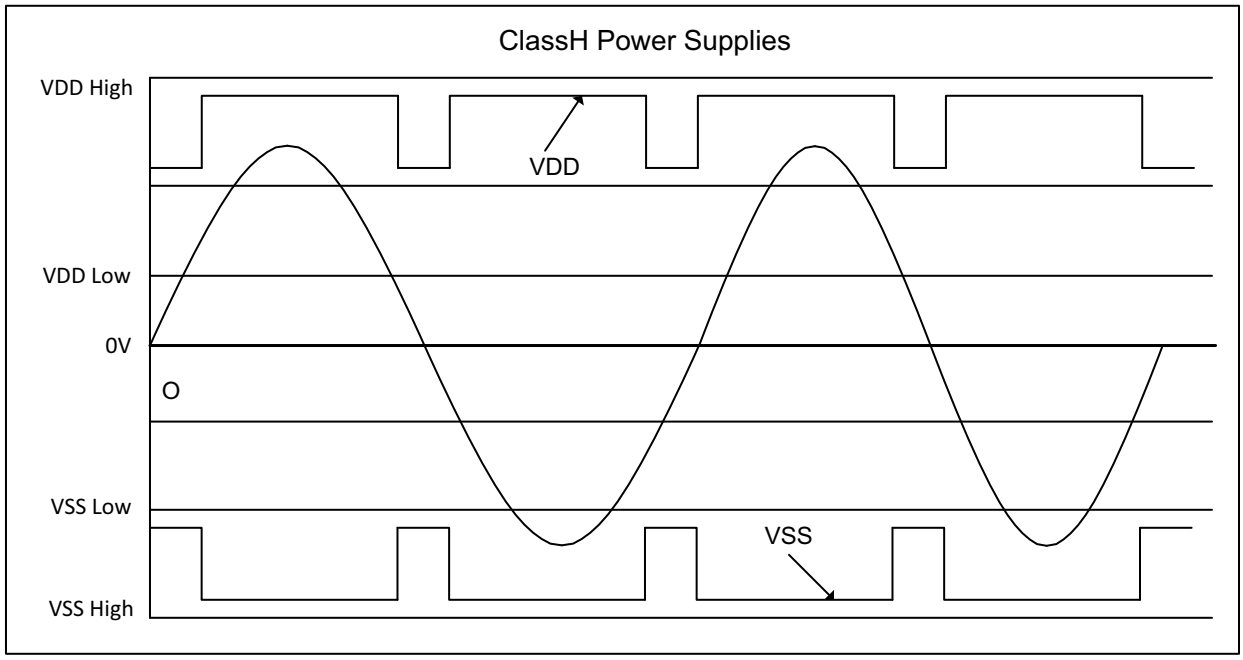
The right channel and left channel audio outputs have independent current limit detection circuits with common register control settings. The current limit can be set to ~100mA , ~150mA, ~200mA, or the protection circuit can be disabled.

The current limiting allows limiting the power delivered to the load without disabling the amplifiers. The lowest setting allows limiting the power delivered to the load to just above 1VRMS into a 16 ohm load while still protecting against a short circuit event. The highest setting protects against a short circuit event while still delivering the maximum power into a 16 ohm load.

4.2. Charge Pump

Charge Pump Class H

The TSDP1xx features 830kHz switching low-noise charge pump architecture. The architecture features controlled switching that minimizes noise generated by turn-on and turn-off transients. The switching frequency is well beyond the audio range, and does not interfere with the audio signals. By controlling the Clocking of the switches, the impulse current noise caused by the parasitic bond wire and trace inductance is minimized or completely eliminated. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of the capacitor at CPVSS to CPGND, CPVDD to CPGND as well as CFLY (fly cap) between CPFP and CPFN. The TSDP1xxclass H amplifier employs a class AB output stage with power-supply voltages that are adjusted based on the output signal level. The output stage senses the output voltage level and adjusts the charge pump supply voltage dynamically. As indicated in the figure below, the adjustment is made on a cycle by cycle basis. Thus when the music level is small, the charge pump supply voltage is correspondingly decreased; and when the music level is high, the charge pump voltage is increased. For typical listening level, this feature can lower the power used in playback mode by almost 45% thus extending battery life by several hours or alternatively the designer could save BOM cost and board space by using smaller battery.



Charge Pump Capacitors

The VREG output (i.e. pin14) should have a 10uF capacitor to ensure both stability and reduced ripple on the LDO output while supplying power to create the class H output supplies. The charge pump outputs CPVDD (pin 12), CPVSS (pin 9) are the class H output supplies providing power to the headphone amplifiers and should each be decoupled to ground with 5uF capacitors. The generated supply voltage across these capacitors will change dependent on the combination of the two headphone output signal levels. A 5uF capacitance should also be placed across the CPFP (pin 13) and CPFN (pin 10) nodes. This capacitor helps create the positive (CPVDD) and negative (CPVSS) supply voltages via charge sharing. Providing a 10uF to the VDD (pin 15) will help to reduce instantaneous demands from the power supply when providing

power to the LDO. It should be noted that using a 0.1uF ceramic capacitor in parallel with the larger Tantalum capacitors at all supply pins can help to reduce unwanted high frequency noise on the supplies at the pins.

Short-Circuit Protection

The Charge Pump also has short circuit detection circuitry which will disable the Charge Pump if a short circuit causes too large a current demand. The Charge Pump will be disabled for 511 charge pump clock cycles and then re-enabled for 63 charge pump clock cycles to see if the short circuit event has been removed. This algorithm will continue until the short circuit event has been removed.

Register Address	Bit	Label	Type	Default	Description
Reg14 CP_SCUR_CTRL1 (0Dh)	7:4	0]	RO	0	Reserved.
	3	RESVERED	RW	1	resets (i.e. when low)the dflop used to latch the output of the comparator detecting Charge Pump Short Circuit event and resets the LSFR used to time the short circuit event checking
	2	VCHP_SC_PWD	RW	0	Powers down the Charge Pumpe Short Circuit block
	1	VCHP_SC_BYPS	RW	0	Bypasses the Short Circuit Event and forces Charge Pump to keep running
	0	RESVERED	RW	0	Reserved

4.3. Modes of Operation

HiZ is enabled, when the headphone amplifiers are powered down, by writing logic 1 in register 14 (i.e. HDPH_CTRL4), bit 3 and ensuring that register 14 bits 4 and 0 are set to logic 0. Place logic 0 in register 14, bit 3 and logic 1 in register 14 bit 0 to disable the HiZ state of the outputs. The HiZ state puts the headphone outputs into a state of high impedance. Use this configuration when the outputs of the TSDP1xxshare traces with other devices whose outputs may be active.

4.4. Jack Detection and Configuration Algorithm

The “SD” pin of the TSDP1xxcan be utilized to effect a Jack Detection and power up the chip when a plug is in inserted in to the Jack. The Jack pin connected to the SD pin should be default ground prior to inserting the plug and pulled to VDDA when the plug is inserted into the JACK

4.5. Thermal Shutdown

There are 2 trip points, “high” and “low”. The “high” trip point should always be set to a higher value than the “low” trip point. If the temperature of the chip increases above the “high” trip point, the headphone outputs will be powered down which will cause the output volumes to be decreased from the current volume toward mute and then the amplifiers will be powered down. The amplifiers will not be powered back up until the temperature on the chip has reduced to the “low” trip point. When the temperature drops below the “low” trip point, the amplifiers will be allowed to power back up and ramp back to the original volume setting. With proper settings on the clock division multiplexers, the “high” and “low” trip points are polled every ~1.5msec or ~3msec.

4.5.1. Thermal Shutdown Registers

4.5.1.1. Temp Sensor Control/Status

The temperature sensor circuit is configured and monitored using the Temp Sensor Control/Status Register

Register Address	Bit	Label	Type	Default	Description
Reg 28-TEMP_SENSE_CTRL1(1Bh) Temp Sensor Control/Status	7:5	HI_TEMP_SEL	RW	3	Temp sensor block hi trip points (000b==>110C, 001b==>125C, 010b==>140C, 011b==>155C, 100b==>170C, 101b==>185C, 110b==>200C,111b==>215C)
	4:2	LO_TEMP_SEL]	RW	2	Temp sensor block low trip points (000b==>110C, 001b==>125C, 010b==>140C, 011b==>155C, 100b==>170C, 101b==>185C, 110b==>200C,111b==>215C)
	1:0	VBG_TRIM_SEL	RW	1	Adjusts the VBG voltage in the Tempsensor by 8mV increments (i.e. 00 ==> 1.215V, , 01b ==> 1.223V, 10b ==> 1.2318V, 11b ==> 1.24V)

4.5.1.2. Headphone Thermal Shutdown Control Register

The thermal shutdown algorithm is configured using the Speaker Thermal Algorithm Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 29 TEMP_SENSE_CTRL2(1Ch) Speaker Thermal Shutdown Control	7:3	RESERVED	RO	0	Reserved
	2	RESERVED	RW	0	Reserved
	1	TEMPSENSE_PWD	RW	0	Temp sensor power down 1b=power down
	0	TEMPSENSE_RSTB	RW	1	Temp sensor reset-0b, reset the tempsense logic

4.6. Asynchronous I2C

4.6.1. I^2C, 2-Wire Control Interface

The TSDP1xx device includes a 2-Wire I^2C compatible interface for communicating with an external controller. This interface supports communication to external micro-controller or other I^2C compatible peripheral chips. The I^2C interface supports normal and fast mode operation.

Device Address Register 0

Register Address	Bit	Label	Type	Default	Description
Reg 1 DEVADD0((00h)	7:1	DEV_ADD0[6:0]	RW	68	Register I2C Device Address
	0	RSVD	R	0	Reserved

Device Identification Register

Register Address	Bit	Label	Type	Default	Description
Reg 2 DEVID(01h)	7:0	DEV_ID[7:0]	R	01000x xxb	8-bit device identification number. The least significant three bits reflect the state of the Bond-Out pins.

Device Revision Register

Register Address	Bit	Label	Type	Default	Description
Reg 3 DEVREV(02h)	7:4	MAJ_REV[3:0]	R	0001	4-bit major revision number (all layer) currently = 1 (1st release) MMMM.mmmm currently = 1.0
	3:0	MIN_REV[3:0]	R	0000	4-bit minor revision number (metal revision) currently = 0 (no revisions-initial release)

4.6.1.1. Register Write Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the TSDP1xx and the R/W bit is '0', indicating a write, then the TSDP1xx responds by pulling SDA low on the next clock pulse (ACK); otherwise, the TSDP1xx returns to the idle condition to wait for a new start condition and valid address.
Once the TSDP1xx has acknowledged a correct device address, the controller sends the TSDP1xx register address. The TSDP1xx acknowledges the register address by pulling SDA low for one clock pulse (ACK). The controller then sends a byte of data (B7 to B0), and the TSDP1xx acknowledges again by pulling SDA low.
When there is a low to high transition on SDA while SCL is high, the transfer is complete. After receiving a complete address and data sequence the TSDP1xx returns to the idle state. If a start or stop condition is detected out of sequence, the device returns to the idle condition.

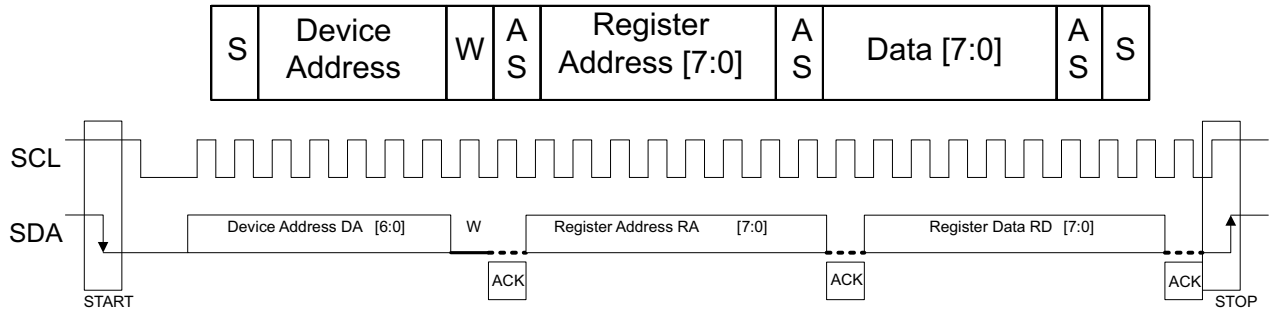


Figure 3. Page Register Write -2 Wire Serial Control Interface

4.6.1.2. Register Burst Write Cycle

The controller may write more than one register within a single write cycle. To write additional registers, the controller will not generate a stop or start (repeated start) command after receiving the acknowledge for the second byte of information (register address and data). Instead the controller will continue to send bytes of data. After each byte of data is received, the register address is incremented.

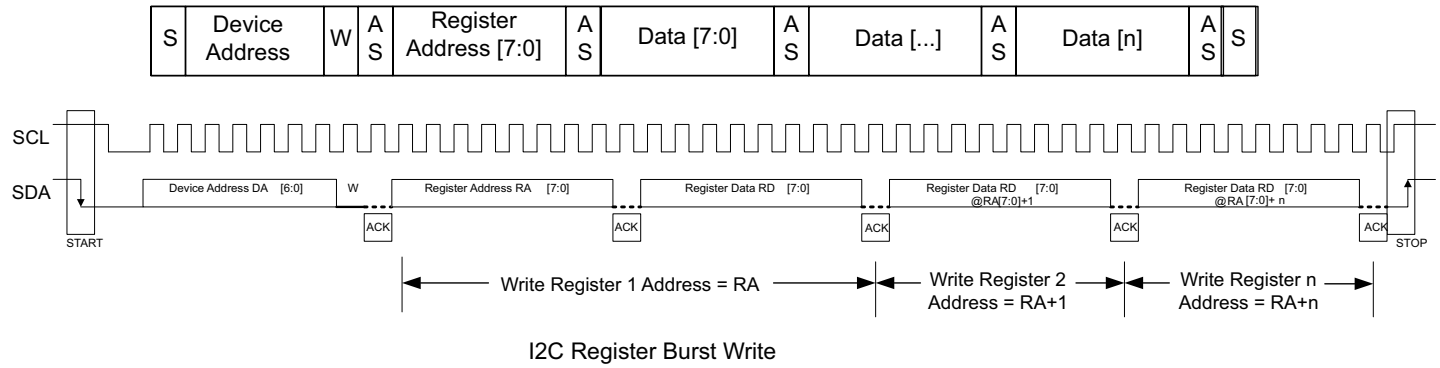


Figure 4. Page Register Burst Write Cycle

4.6.1.3. Register Read Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. If the device address received matches the address of the TSDP1xx and the R/W bit is '0', indicating a write, then the TSDP1xx responds by pulling SDA low on the next clock pulse (ACK); otherwise, the TSDP1xx returns to the idle condition to wait for a new start condition and valid address.

Once the TSDP1xx has acknowledged a correct address, the controller sends a restart command (high to low transition on SDA while SCL remains high). The controller then re-sends the devices address with the R/W bit set to '1' to indicate a read cycle.The TSDP1xx acknowledges by pulling SDA low for one clock pulse. The controller then receives a byte of register data (B7 to B0).

For a single byte transfer, the host controller will not acknowledge (high on data line) the data byte and generate a low to high transition on SDA while SCL is high, completing the transfer. If a start or stop condition is detected out of sequence, the device returns to the idle condition.

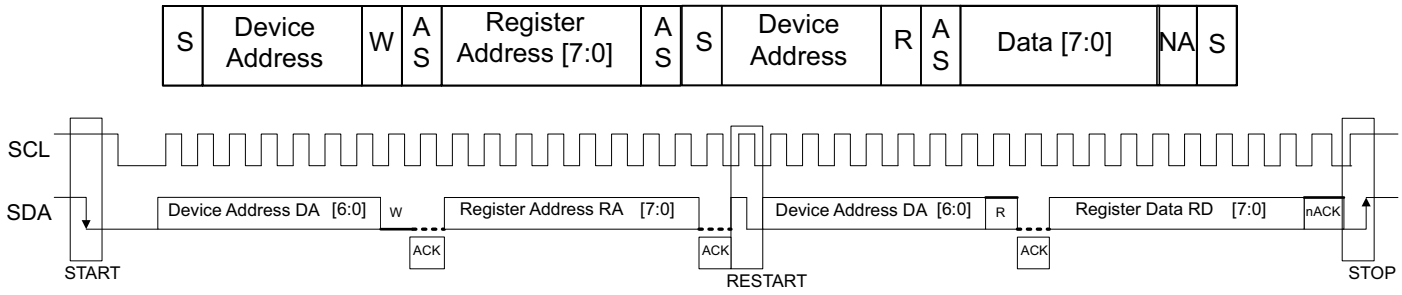
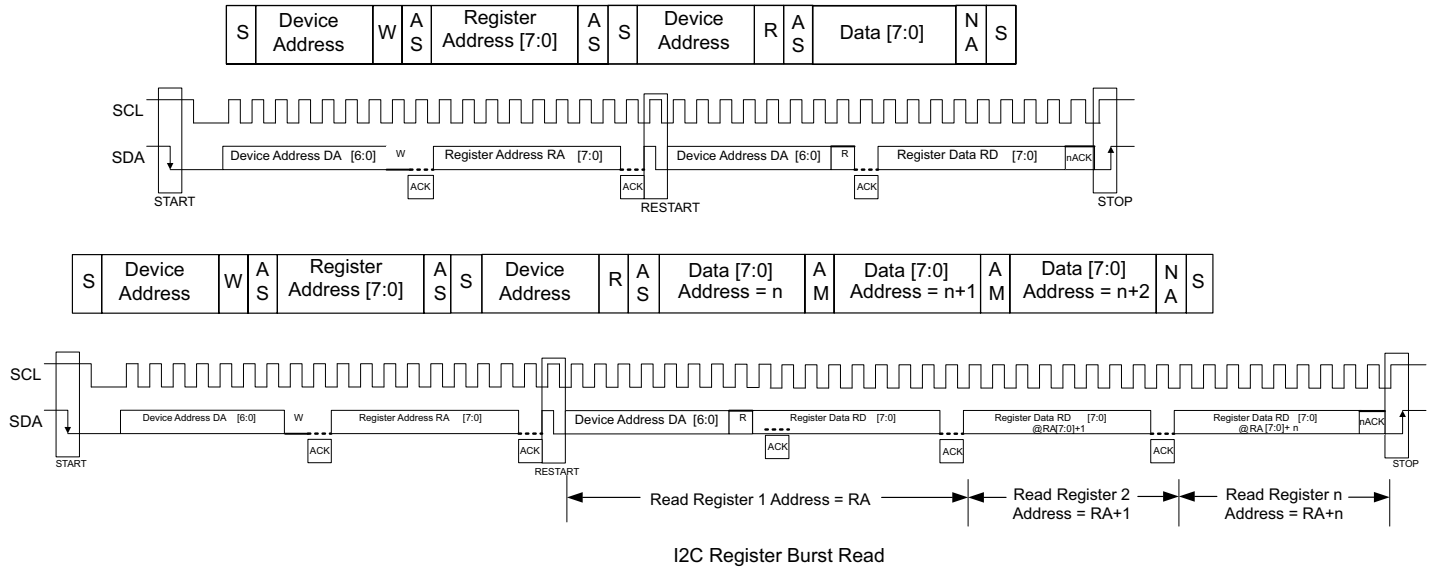


Figure 5. Page Register Single Byte Read Cycle

4.6.1.4. Page Register Burst Read Cycle

The controller may read more than one register within a single read cycle. To read additional registers, the controller will not generate a stop or start (repeated start) command after sending the acknowledge for the byte of data. Instead the controller will continue to provide clocks and acknowledge after each byte of received data. The TSDP1xx will automatically increment the internal register address after each register has had its data successfully read (ACK from host) but will not increment the register address if the data is not received correctly by the host (nACK from host) or if the bus cycle is terminated

unexpectedly. By automatically incrementing the internal register address after each byte is read, all the internal registers of the TSDP1xx may be read in a single read cycle.



I2C Register Burst Read

Figure 6. Page Register Burst Multi-byte Read Cycle

5. REGISTERS

5.0.0.1. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 4 STATUS0(03h)	7	VREG_SC_DET	RO	0h	Short Circuit Detected on LDO output when high(Requires vreg_sc_rstb in Reg8(07h) to be toggled)
	6	VDDA_BELOW_3P1V	RO	0h	Detects VDDA supply level for 2.5V operation (i.e. trip ~3.1V)
	5	SUPPLY_OSC	RO	0h	Detects VDDA supply level for 3.3 to 5V operation (i.e. trip ~4.16V)
	4	RESERVED	RO	0h	Reserved
	3	RESERVED	RO	0h	Reserved
	2	TEMP_OVERHEAT	RO	0h	Temp sensor statemachine overheat output.
	1	OVERHEAT_HIGH	RO	0h	Temp sensor high overheat indicator.
	0	OVERHEAT_LOW	RO	0h	Temp sensor low overheat indicator.

5.0.0.2. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 5 STATUS1(04h)	7:2	RESERVED	RO	0h	Reserved
	1	SD	RO	0h	Input signal Shutdown from Pin.
	0	VCHP_SC_DET	RO	0h	Short Circuit Detected on Charge Pump VPOS or VNEG output when high(Will automatically reset)

5.0.0.3. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 6 CP_CTRL1(05h)	7	DELAY_MODE	RW	0h	Reserved
	6	MODE_DELAY_BYPS	RW	1h	Reserved
	5:3	VCHP_CLKSEL	RW	1h	Reserved
	2	VCHP_HIZ_VPOS_OVRD	RW	0h	Reserved
	1	VCHP_HIZ	RW	0h	Reserved
	0	VCHP_PWD	RW	0h	Powers down the Charge Pump

5.0.0.4. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 7 CP_CTRL2(06h)	7:4	RESERVED	RO	0h	Reserved
	3	AB_OVR_MODE	RW	0h	When "d2a_ab_ovr_en" is high, this bit will select the mode of operation (i.e. 0==> Split Mode, 1 ==> Invert Mode)
	2	AB_OVR_EN	RW		Enables the over riding of the automatic Class H operation when high
	1:0	DROP_SEL	RW	0h	Timing options for delaying the change from Invert to Split

5.0.0.5. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 8 VREG_CTRL(07h)	7	RESERVED	RO	0h	Reserved
	6:5	VREG_SEL	RW	2h	Selects the output voltage setting for the LDO (i.e. 00b => 2.395V, 01b ==> 2.592V, 10b ==> 2.793V, 11b ==> 3.076V)
	4	VREG_SC_RSTB	RW	1h	Resets the Short Circuit detection latched output
	3	RESERVED	RW	0h	Reserved
	2	RESERVED	RW	0h	Reserved
	1	RESERVED	RW	0h	Reserved
	0	VREG_PWD	RW	0h	Powers down the LDO output and pulls the LDO output to ground.

5.0.0.6. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 9 VDDA_SENSE_CTRL(08h)	7	RESERVED	RO	0h	Reserved
	6	RESERVED	RW	1h	Reserved
	5	RESERVED	RW	0h	Reserved
	4	RESERVED	RW	0h	Reserved
	3	VDDSENSE_PWD	RW	0h	Powers down the vddsense block
	2	RESERVED	RW	1h	Reserved
	1:0	RESERVED	RW	0h	Reserved

5.0.0.7. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 25 BIASG_CTRL2(18h)	7:1	RESERVED	RO	0h	Reserved
	0	POR	RW	0h	This signal is Ored with the POR output to generate "a2d_por_5v"

5.0.0.8. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 26 REF_SUP_CTRL(19h)	7:4	RESERVED	RO	0h	Reserved
	3	REFSUPPLY DET_PWD	RW	0h	Powers down the refsupply detection amplifier.
	2	RESERVED	RW	0h	Reserved
	1	RESERVED	RW	0h	Reserved
	0	RESERVED	RW	0h	Reserved

5.0.0.9. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 30 PAD_CTRLTATUS0 (1Dh)	7	SD_B_PUB	RW	1h	SD pin pull up resistor, 1 is off
	6	SD_B_PD	RW	1h	SD pin pull down resistor, 1 is on
	5	I2C_DATA_PUB	RW	0h	I2C data pin pull up resistor, 0 is on
	4	I2C_DATA_PD	RW	0h	I2C data pin pull down resistor,0 is off
	3	I2C_CLK_PUB	RW	0h	i2c clock pin pull up resistor, 0 is on
	2	I2C_CLK_PD	RW	0h	i2c clock pin pull down resistor, 0 is off
	1	CLK_DEGLITCH_BYPS	RW	0h	Bypasses the deglitch circuitry in the I2C CLK pad
	0	DATA_DEGLITCH_BYPS	RW	0h	Bypasses the deglitch circuitry in the I2C DATA pad

5.0.0.10. Control Register

Register Address	Bit	Label	Type	Default	Description
Reg 31 SHUTDOWN(1Eh)	7:1	RESERVED	RO	0h	Reserved
	0	SHOUTDOWN_B	RW	1h	Software Controlled Shutdown

5.1. Register Map

5.1.1. Register Map Summary Table

Table 2. Register Map

Register	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R1 (00h)	DEVADD0	Device Address 0	DEV_ADD0[6:0]							RSVD	68h
R2 (01h)	DEVID	Device iD	DEV_ADD1[6:0]								40h
R3 (02h)	DEVREV	Device Revision	MAJ_REV[3:0]				MIN_REV[3:0]				10h
R4 (03h)	STATUS	Status	VREG_SC_DET	VDDA_BELOW_3P1V	SUPPLY_OSC			TEMP_OVERHEAT	OVERHEAT_HIGH	OVERHEAT_LOW	00h
R5 (04h)	STATUS	Status							SD	VCHIP_SC_DET	00h
R6 (05h)	CP_CTRL1L	Control	DELAY MODE	MODE_DELAY_BYPAS	VCHP_CLKSEL			VCHP_HIZ_VPOS_OVRD]	VCHP_HIZ	VCHP_PWD	48h
R7(06h)	CP_CTRL2	Control					AB_OVER_MODE	AB_OVER_EN	DROP_SEL		0h
R8 0(7h)	VREG_CTRL	REG Control		VREG_SEL	VREG_SEL	VREG_RSTB	VREG__HALFCUR	VREG_GNDSHRT	VREG_BYPAS	VREG_PWD	50h
R9(08h)	VDAA_SENSE_CTRL	SENSE Control		VDDSENSE_VREG_SEL_OV	VDDSENSE_MODE_OVRD	VDDSENSE_HALFCUR	VDDSENSE_PWD	VDDSENSE_RSTB	VDD_TRP_SEL		44
R10(09h)	CLSH_SENSE_CTRL1		RESERVED				REFN_SEL_PWD	REFP_SEL_PWD	HPSENSE_HALFCUR	HPSENSE_PWD	0h
R11(OAh)	CLSH_SENSE_CTRL2		HP_REFNS_SEL		HP_REFNI_SEL		HP_REFPS_SEL		HP_REFPI_SEL		0h
R12(0Bh)	HI_CUR_CTRL1				SW1_SW4_KILL_EN	SW_INVERT_KILL_EN	SW1_WEAK_STRONGB	STARTUP_ONESHOT_RSTB	STARTUP_CNT_64_32B	STARTUP_SW_EN	37h
R13(0Ch)	HI_CUR_CTRL2						SW_REFNS_SEL		SW_REFPI_SEL		0h
R14(0Dh)	CP_SCUR_CTRL1						VCHP_SC_RSTB	VCHP_SC_PWD	VCHP_SC_BYPS	VCHP_SC_HALFCUR	08h
R15(0Eh)	CP_SCUR_CTRL2		SC_REFPI_SEL		SC_REFPS_SEL		SC_REFNI_SEL		SC_REFNS_SEL		80h
R16(0Fh)	CP_REG_CTRL1						CLKREG_RSTB	CLKREG_PWD	CLKREG_BYPS	CLKREG_HALFCUR	08h
R17(10h)	CP_REG_CTRL2				CLKREG_REFP_SEL		CLKREG_REFNI_SEL		CLKREG_REFNS_SEL		0h
R18(11h)	HDPH_CTRL1		HP_ILIM		HPL_PWD	HPR_PWD	HP_PWD_OVRD	HP_ANTIPOP_BYPASS	HPL_MUTE	HPR_MUTE	C0h
R19(12h)	HDPH_CTRL2		BST_HP_GAIN	HP_DISCHOP_ANTIPOP	HP_DISCHOP_AMP	HP_CNT_TARGET_L					10h
R20(13h)	HDPH_CTRL3			REDUCE_HP_IBAT	HP_D3	HP_CNT_TARGET_R					10h
R21(14h)	HDPH_CTRL4		HP_ANTIPOP_CNT_LOAD	HP_ANTIPOP_CNT_HOLD	HP_ANTIPOP_RSTB	HP_OUTGND_REG	HPOUTGND_OVRD	HP_AMPIN_GND_REG	HP_AMPIN_GND_OVRD	HP_CONNECT_GND_VAG	21h
R22(15h)	SELF_OSC_CTRL1		SELFOSC_DIVCLK_SEL		SELFOSC_VCHP_SEL			SELFOSC_FERQ_SEL			05h
R23(16h)	SELF_OSC_CTRL2					SELFOSC_PWD	SELFOSC_RSTB	SELFOSC_CHPCLK_PWDB	SELFOSC_AOPCLK_PWDB	SELFOSC_APOPCLK_SEL	0Ah

Register	Name	Remarks	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Default
R24(17h)	BIASG_CTRL 1		IBIAS_NONDAC				IBIAS_SEL		IBIAS_REF _CORE_PW D	IBIAS_GEN _MUX	0h
R25(18h)	BIASG_CTRL 2									POR	0h
R26(19h)	REF_SUP_C TRL						REFSUPPL Y_PWD	SUPOVR_V AL	SUPOVR_E N	INVERT_SU PPLY_OSC	0h
R27(1Ah)	BANGAP_CT RL							BGCORE_BYPS		BGCORE_I BIAS_MUX	0h
R28(1Bh)	TEMP_SENS E_CTRL1	TEMPATURE Control	HI_TEMP_SEL			IO_TEMP_SEL			VBG_TRIM_SEL		69h
R29(1Ch)	TEMP_SENS E_CTRL2							TS_TEST_ MODE	TEMPSENS E_PWD	TEMPSENS E_RSTB	01h
R30(1Dh)	PAD_CTRL		SD_B_PUB	SD_B_PD	I2C_DATA_ PUB	I2C_DATA_ PD	I2C_CLK_P UB	I2C_CLK_P D	CLK_DEGLI TCH_BYPS	DATA_DEG LITCH_BYP S	C0h
R31(1Eh)	SHUTDOWN									SHUTDOW N_B	01h
R32(1Fh)	SPARE2		TST								0h
R33(1Gh)	SPARE2		TST								0h

Notes:

1 Registers not described in this map should be considered “reserved”.

6.PIN CONFIGURATION AND DESCRIPTION

6.1. 20-Pin QFN TSCS10XX

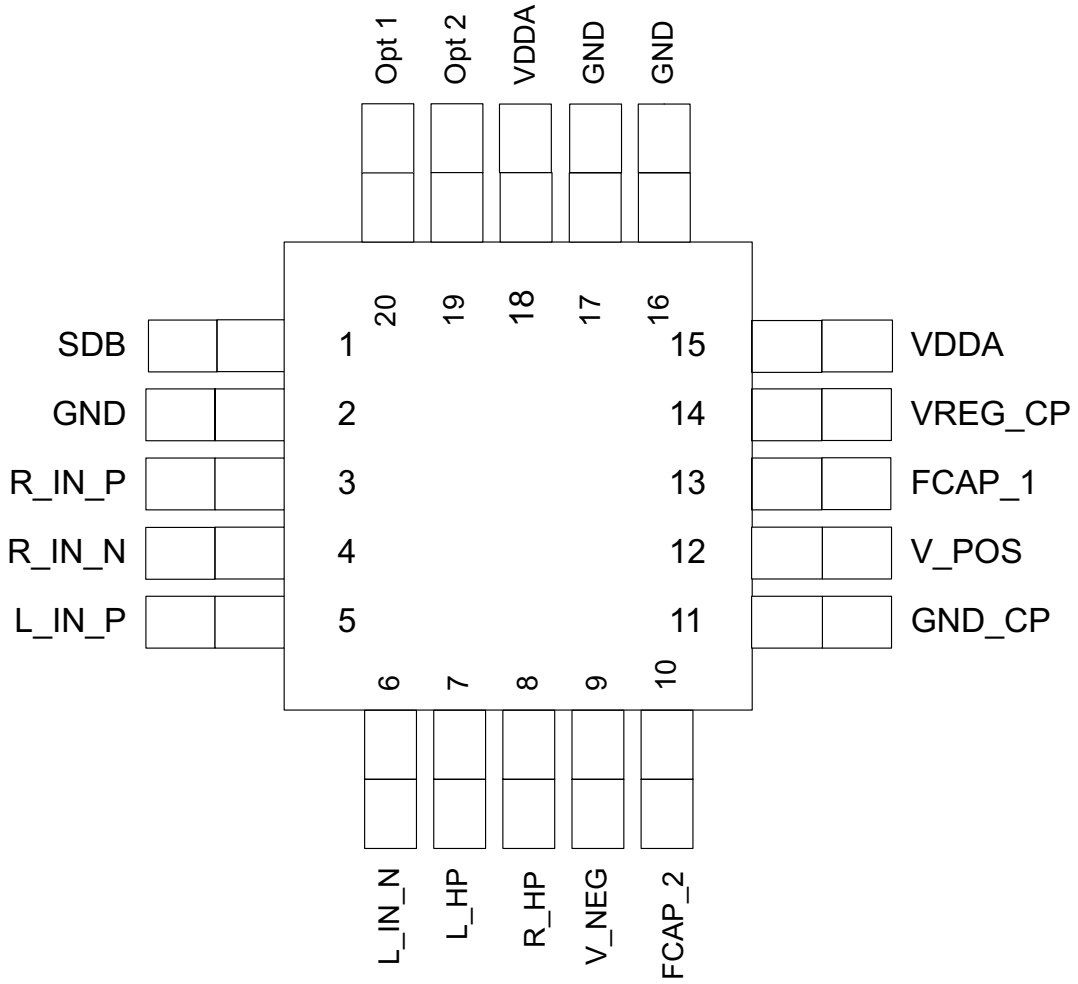


Figure 7. 20-Pin TSDP1xxQFN

6.2. 20-Pin QFN TSCS11XX

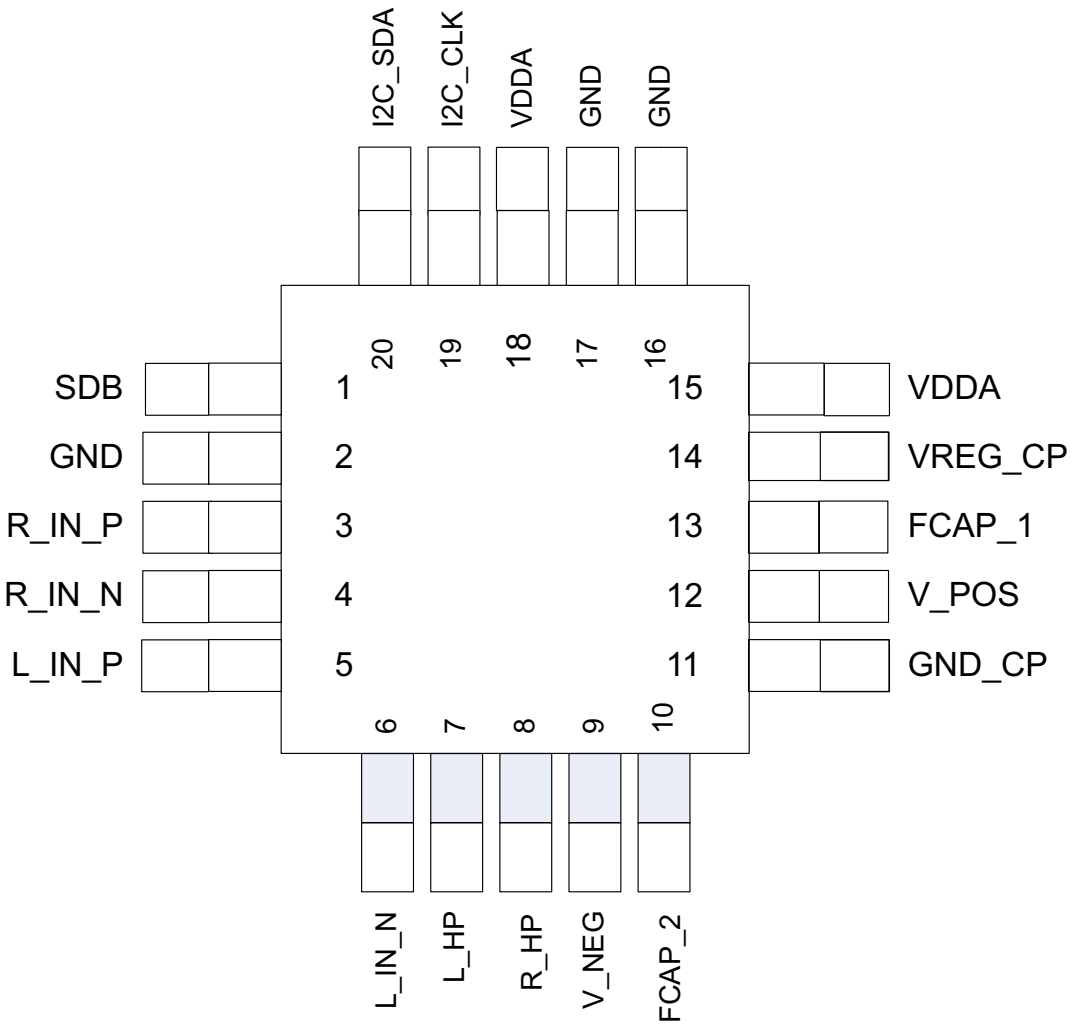


Figure 8. 20-Pin TSDP11XX QFN

6.3. Pin Table for pin QFN package

POWER

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	20 pin location
VDDA	**Positive supply**	I(Power)	-	18,15
GND	**Ground supply**	I(Power)	-	2,16,17
V_POS	**Charge pump positive supply**	I(Power)	-	12
V_NEG	**Charge pump negative supply**	I(Power)	-	9
FCAP_1	**Flying cap**	I/O(Power)	-	13
FCAP_2	**Flying cap**	I/O(Power)	-	10
VREG_CP	**LDO filter CAP**	I/O(Power)		14

ANALOG INPUT

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	20 pin location
L_IN_P	**Left Audio Positive Input**	I(Analog)	None	5
L_IN_N	**Left Audio Negative Input**	I(Analog)	None	6
R_IN_P	**Right Audio Positive Input**	I(Analog)	None	3
R_IN_N	**Right Audio Negative Input**	I(Analog)	None	4

ANALOG OUTPUT

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	20 pin location
L_HP	**Audio Headphone Output Left** - ground referenced	O(Analog)	None	7
R_HP	**Audio Headphone Output Right** - ground referenced	O(Analog)	None	8

10 pins
DATA and CONTROL

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	20 pin location
I2C_CLK	**I^2C shift clock** for serial control port	I(Digital)	Pull-Up	19
I2C_SDA	**I^2C shift data** for serial control port	I/O(Digital)	Pull-Up	20
SD	**Shutdown Control** for chip	I(Digital)	Pull-Down	

6.4. PIN FUNCTION

PIN QFN	NAME	INPUT/OUTPUT POWER	DESCRIPTION
1	SD	I (DIG)	Shutdown. SD is active low. SD turns the IC on and off. When SD is low, the device is in shutdown mode and the jack insertion detect circuitry is active. SD has to be high to turn on the device and run the jack configuration detect algorithm. Typically, SD is held low until the system gets an interrupt from the IC, indicating that a jack has been inserted. The system then pulls SD high. 0 = The IC is in shutdown mode with jack detection circuitry active. 1 = The IC is active. The jack configuration algorithm runs immediately after a load has been detected.
2	GND	P (GND)	Headphone Ground Reference. This need to be very clean ground for best results.
3	R_INP	I (ANA)	Headphone Right Positive Differential Input
4	R_IN_N	I (ANA)	Headphone Right Negative Differential Input
5	L_IN_P	I (ANA)	Headphone Left Positive Differential Input
6	L_IN_N	I (ANA)	Headphone Left Negative Differential Input
7	L_HP	O (ANA)	Headphone Left Output
8	R_HP	O (ANA)	Headphone Right Output
9	V_NEG	P	Charge Pump Negative Power Output. Connect one side of 5µF capacitor to CPNEG and the other side to CPGND.
10	FCAP_2	P	Charge Pump Negative Fly Cap. Connect one side of 5µF capacitor to CPFP (pin 13)and the other side to CPFN (pin 10) with wide traces.
11	CP_GND	P (GND)	Charge Pump Output Ground Reference
12	V_POS	P	Charge Pump Positive Power Output. Connect one side of 5 µF capacitor to CPPOS and the other side to CPGND (pin 11).
13	FCAP_1	P	Charge Pump Positive Fly Cap. Connect one side of 5µF capacitor to CPFN (pin 10) and the other side to CPFP (pin 13) with wide traces.
14	VREG_CP	P	Regulator Positive Power Output. Connect 10uF cap to GND (pin 16)
15	VDDA	P (VDD)	Regulator Input Positive Power . Connect 10uF cap to GND (pin 16)
16	GND	P (GND)	Regulator Input Ground Reference
17	GND	P (GND)	Clean Analog Ground
18	VDD	P (VDD)	Clean Analog Power—Battery or regulated supply. A separate 1µF decoupling cap must be connected directly from VDD (pin18) to GND (pin 17).
19	I2C_CLK	I (DIG)	I2C Serial Clock Input For Register Read/Write
20	I2C_SDA	I/O (DIG)	Serial Data I/O. Register Interface

ELECTRICAL CHARACTERISTICS
VDD=5V, GND=0, etc

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}		2.5		5.5	V
Quiescent Supply Current		One channel enabled		4		mA
		Two channels enabled		7	9	
Shutdown Supply Current				10		µA
Shutdown Threshold		V_{IH}		0.7X VDD		V
		V_{IL}		0.3X VDD		
Shutdown Input Leakage Current						µA
Shutdown to full Operation		No pop/click start-up		30		ms
CHARGE PUMP						
Oscillator Frequency	F_{OSC}			830	970	kHz
AMPLIFIERS						
Input Offset Voltage	V_{OS}			0.1		µV
DC Power supply rejection ratio	PSSR			-90		dB
Power supply rejection ratio	CMRR			-101		dB
Output Power	P_{OUT}	RL=16Ω		210		mW
		RL=32Ω		105		
		RL=10KΩ		.333		

OPERATING CHARATERISTICS
V_{DD}=5V, T_A=25C, R_L = 16Ω (unless otherwise noted)

Parameter	Symbol	CONDITIONS	MIN	TYP	MAX	Units
Signal-to-Noise Ratio	SNR	A-weighted; 0dB gain		104		dB
Total Harmonic Distortion + Noise	THD+N	RL=32Ω, P_{OUT}=25mW		0.008		%
		RL=16Ω, P_{OUT}=50mW		0.008		
Slew Rate	SR			TBD		V/µs
Maximum Capacitive Load	C_L	No sustained oscillations		300		pF
Crosstalk				90		dB

7. CHARACTERISTICS

7.1. Audio Fidelity

SNR: >100dB, A-Weighted, 5.0V

7.2. Electrical Specifications

7.2.1. Absolute Maximum Ratings:

Voltage on any pin relative to Ground	Vss - 0.3V TO Vdd + 0.5V
Industrial Temperature	-40 ^{o}C TO 85 ^{o}C
Storage Temperature	-65 ^{o}C TO +150 ^{o}C
Soldering Temperature	260 ^{o}C
Headphone Output Current	230mA
Maximum Supply Voltage	5.5 Volts = VDD

Table 3.

7.3. Recommended Operating Conditions

Parameter	**Min**	**Typ**	**Max**	**Unit**
Power Supplies VDD	2.5	5.0	5.5	V
Industrial Temperature	-40	25	85	^{o}C
T_j			150	^{o}C

Table 4. Recommended Operating Conditions

Note: ***ESD:*** *The TSDP1xx is an ESD (Electrostatic discharge) sensitive device. Even though the TSDP1xx family implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.*

7.4. Characteristics

Test Conditions

Unless stated otherwise, VDD=5.0V, TA=+25C, 997Hz signal, Input Signal=0.44VRMS,

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Inputs (L_{INP}, L_{INN}, R_{INP}, R_{INN})						
Full Scale Input Voltage	V_{FSIV}	L/R_{INx} Differential Mic		1.0 0	.	Vrms dBV
Input Impedance				50	??	KΩ
Input Capacitance				10		pF
Volume Control						
Programmable Gain Min				0		dB
Programmable Gain Max				6		dB
Programmable Gain Step Size				2		dB
Headphone Outputs (HPL, HPR)						
Full Scale Output Level	V_{FSOV}	RL = 10KΩ		??		Vrms
		R_L = 16Ω		1.84		Vrms
Output Power	P_O	997Hz full scale signal, R_L = 16Ω		35		mW (avg)
Signal to Noise Ratio	SNR	A-weighted, R_L = 16Ω		101		dB
Total Harmonic Distortion +Noise	THD+N	R_L = 16Ω, -3dBFS		-72		dB
		R_L = 16Ω, -6dBFS		-78		dB
		R_L = 32Ω, -3dBFS		-75		dB
		R_L = 32Ω, -6dBFS		-80		dB
Digital Input/Output						
Input Capacitance				5		pF
Input Leakage			-0.9		0.9	uA
DC Characteristics for SD						
Input High Level	VIH		0.7x DVDD_IO			V
Input LOW Level	VIL				0.3x DVDD_IO	V
DC Characteristics for SCL and SDA						
Input High Level	VIH		0.7x DVDD_IO			V
Input LOW Level	VIL				0.3x DVDD_IO	V
Output Low Level	VOL	IOL = 1mA		0.1xDVDD_IO		V
ESD / Latchup						
IEC1000-4-2			1			Level
JESD22-A114-B			2			Class
JESD22-C101			4			Class

7.5. Low Power Mode Power Consumption

Mode	VDD (V)	I_{VDD} (mA)	P_{TOTAL} (mW)	Notes
Headphone enabled	5.0	??	??	Full scale 1Vrms/10KΩ,
Headphone enabled	5.0	??	??	Full scale 0.1Vrms/10KΩ,
Headphone enabled	5.0	??	??	Full scale 1Vrms/16Ω,
Headphone enabled	5.0	??	??	Full scale 0.1Vrms/32Ω,

8. APPLICATION NOTES

Power Supply Bypass Capacitor
The power-supply bypass capacitor lowers the power supply impedance and provides instantaneous current to the TSDP10XX. Describe capacitor values and why

Layout and Grounding Recommendations
Proper layout and grounding are essential for optimum performance of the TSDP10XX. DESCRIBE Connections

9. ORDERING GUIDE

TSDP10xx1NLGXyyX	FIXED FUNCTION
TSDP11xx1NLGXyyX	WITH I2C CONTROL

Please contact an TSI Sales Representative for more information.

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11. REVISION HISTORY

Rev	Date	Description of changes
0.3	4/20/2015	Initial Release
0.9	8/17/2015	Updated Description and Register
0.95	8/24/2016	Updated pinout
0.99	12/5/2016	Updated diagrams and format
1.0	1/12/2017	updated year and removed confidential

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