TS Type Stratum III Voltage Controlled Temperature Compensated Crystal Oscillator

RoHS Compliant Standard

FEATURE

1. Typical 7.0 x 5.0 x 2.0 mm ceramic SMD package.
2. Stratum 3 (Overall ±4.6ppm including 20 years aging)
3. CMOS and Clipped Sine wave (without DC-cut capacitor) output optional.
4. Packing: Tape & Reel 1000/3000 pcs per Reel.

Actual Size 

ORDERING INFORMATION

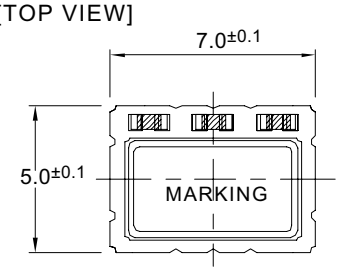
T	S	E	A	T	L	J		A	N	F	_	?
TCXO	Package (mm)	Supply Voltage (V)	Pulling Range (ppm)	Freq. Stability (ppm)	Temp. Range (°C)	Output Logic and Symmetry		Oscillator Mode	Appearance	Lead Free	Dash	Freq. (MHz)
	S: 7.0 x 5.0 x 2.0	C:5V E:3.3V	A: ±5 B: ±8 T: TCXO	T : ±4.6 (Including 20 Years Aging)	C : -20~+70 L : -40~+85		50±5%	-A: AT Fundamental * Not Selectable by Customer	N : Normal	F : RoHS Compliant		XX.XXXXXX
						CMOS 15pF	J					
						S: Clipped Sine Wave						

Ordering Example: TSEATLJANF-12.800000 MHz

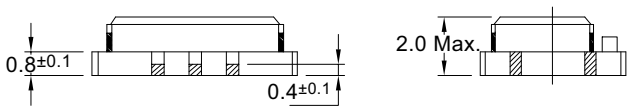
TCXO S-TYPE; V_{DD}:3.3V; Pulling Range: ±5ppm; Freq. Stability: ±4.6 (Including 20 Years Aging); Temp. Range: -40°C to +85°C; Load: CMOS 15pF, Symmetry: 50±5%; AT Fundamental; Normal Appearance; RoHS Compliant; Freq.: 12.800000 MHz.

OUTLINE DRAWING

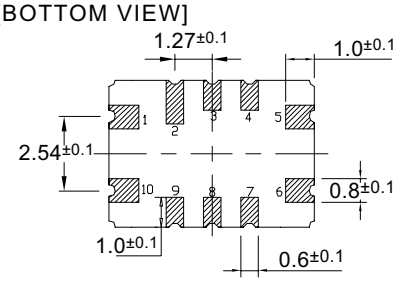
[TOP VIEW]

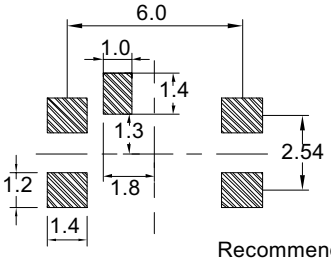


[SIDE VIEW]



[BOTTOM VIEW]





Recommended Soldering Pattern

Pad	Function
1	VCON : VC-TCXO NC : TCXO
2	NC
3	NC
4	NC
5	GND
6	CMOS/ Clipped Sinewave Output
7	NC
8	NC
9	Tri-State Control*
10	V_{DD}

*Tri-state:
1. Pad 9 > 70%VDD or NC: Output Enable
2. Pad 9 < 30%VDD or NC: Output Enable

*Contact Sales@taitien.com.tw for special request.

ELECTRICAL SPECIFICATION

Parameter	Min.		Max.		Unit
	5.0	3.3	5.0	3.3	V
Supply Voltage Variation(V_{DD}) 5%	4.75	3.13	5.25	3.47	V
Frequency Range	10		26		MHz
Standard Frequency (for CMOS)	12.800				MHz
Standard Frequency (for Clipped sine)	10.00, 12.80, 19.20, 19.44, 25.60				MHz
Operating Temp. Range	Refer to Ordering Information				°C
Frequency Stability (Overall)	±4.6				ppm
Frequency Stability					
Vs Temperature Range (@-20°C ~ +70°C)	–		±0.28		ppm
Vs Temperature Range (@-40°C ~ +85°C)	–		±0.37		ppm
Supply Current (CMOS output)	–		6		mA
Supply Current (Clipped Sine-wave output)	–		3.5		mA
Output Level (CMOS)					
Output High (Logic "1")	90% V_{DD}		–		V
Output Low (Logic "0")	–		10% V_{DD}		V
Duty	45%		55%		%
Output Level (Clipped Sine Wave)	0.8		–		Vp-p
Vc Input Impedance	100		–		KΩ
Phase Noise @12.8MHz					
100Hz	-120				dBc/Hz
1KHz	-140				dBc/Hz
10KHz	-148				dBc/Hz
Start Time	–		2		mSec
Tri-state					
Disable	–		(V_{DD})*20%		V
Enable	(V_{DD})*80%		–		V
Storage Temp. Range	-55		125		°C

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