



TSP3N80N / TSF3N80N

800V N-Channel MOSFET

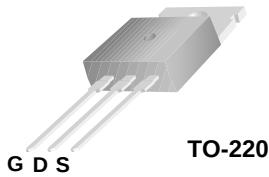
General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.

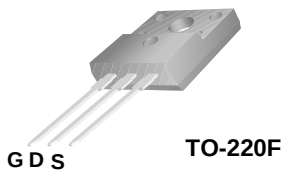
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

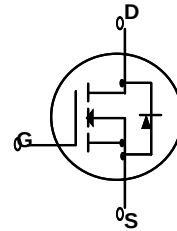
- 3.0A, 800V, $R_{DS(on)} = 5.00\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 15nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220



TO-220F



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	TSP3N80N	TSF3N80N	Units
V_{DSS}	Drain-Source Voltage	800		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	3.0	3.0*	A
	- Continuous ($T_C = 100^\circ\text{C}$)	1.8	1.8 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	12	12*	A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	336		mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	10.7		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	107	39	W
	- Derate above 25°C	0.85	0.31	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	TSP3N80N	TSF3N80N	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.17	3.2	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$



TSP3N80N / TSF3N80N

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	800	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	1	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$	--	3.8	5.0	Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	550	--	pF
C_{oss}	Output Capacitance		--	60	--	pF
C_{rss}	Reverse Transfer Capacitance		--	8	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 3.0\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	20	--	ns
t_r	Turn-On Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	--	ns
t_f	Turn-Off Fall Time		--	30	--	ns
Q_g	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 3.0\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	15	-	nC
Q_{gs}	Gate-Source Charge		--	3.5	--	nC
Q_{gd}	Gate-Drain Charge		--	7.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	3.0	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 3.0 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 3.0 A, dI _F / dt = 100 A/μs	--	650	--	ns
Q _{rr}	Reverse Recovery Charge	(Note 4)	--	5.0	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 70\text{ mH}, I_{AS} = 3.0\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 3.0\text{ A}, dI/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature



Typical Characteristics

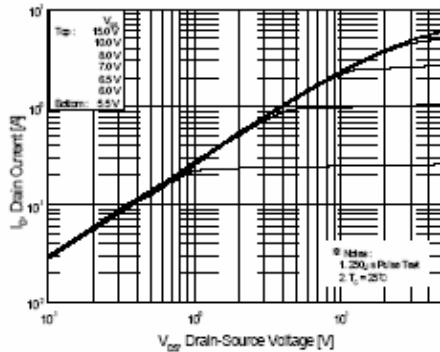


Figure 1. On-Region Characteristics

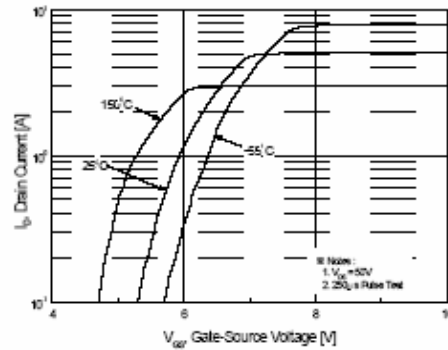


Figure 2. Transfer Characteristics

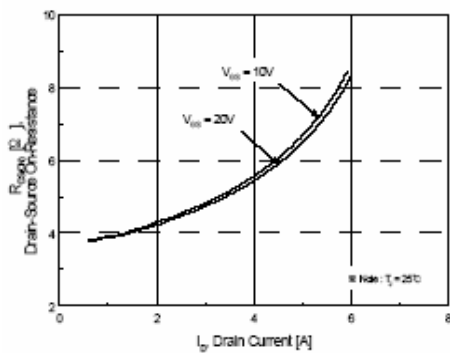


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

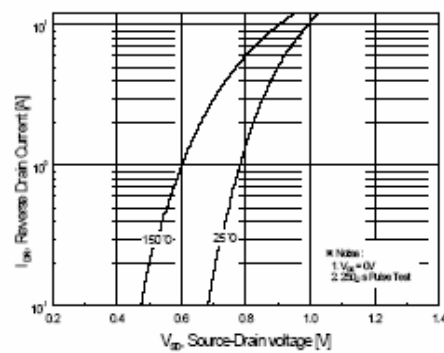


Figure 4. Body Diode Forward Voltage Variation with Source Current

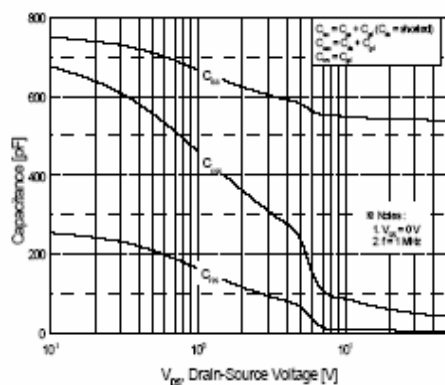


Figure 5. Capacitance Characteristics

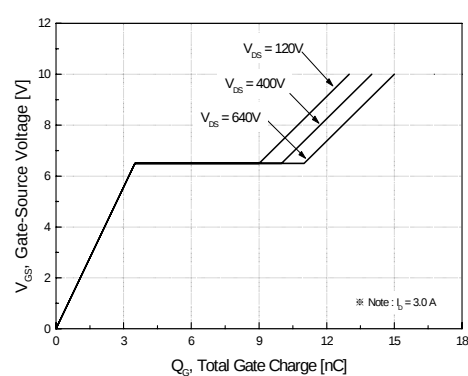


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

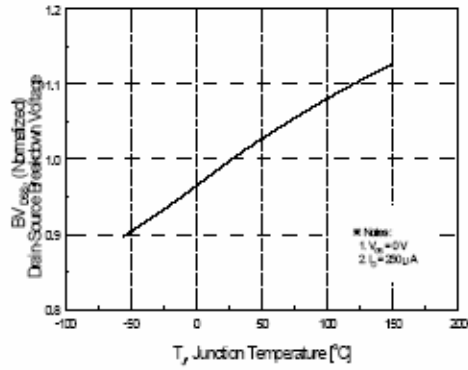


Figure 7. Breakdown Voltage Variation vs Temperature

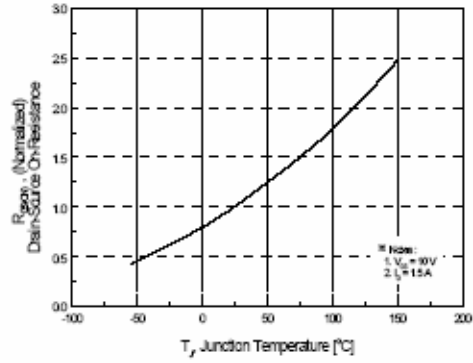


Figure 8. On-Resistance Variation vs Temperature

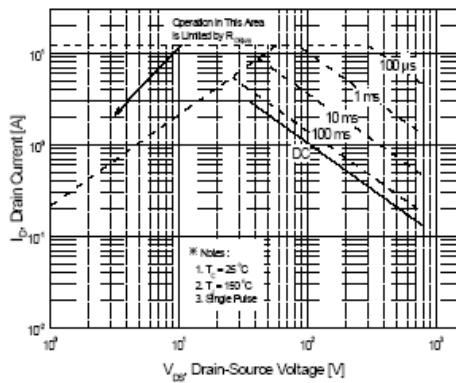


Figure 9-1. Maximum Safe Operating Area for TSP3N80N

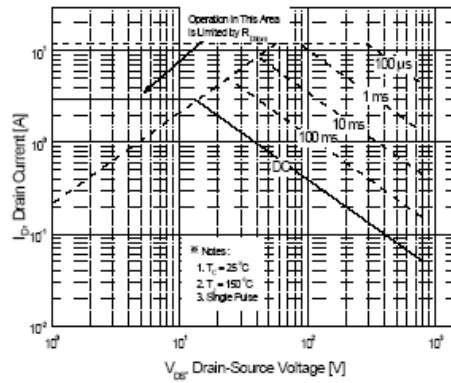


Figure 9-2. Maximum Safe Operating Area for TSF3N80N

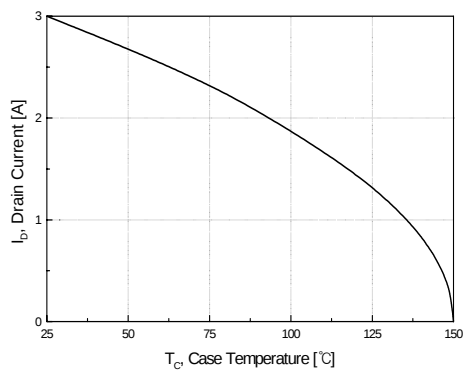


Figure 10. Maximum Drain Current vs Case Temperature



Typical Characteristics (Continued)

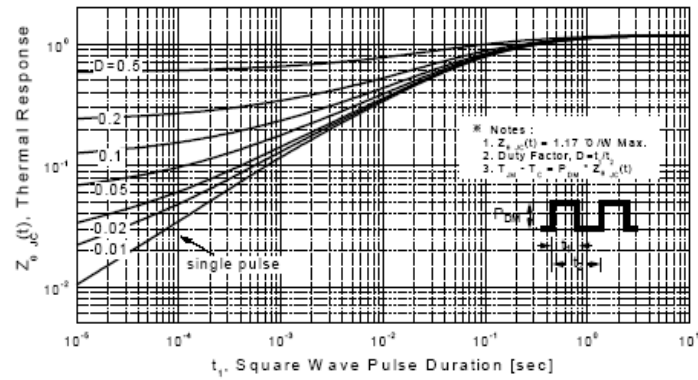


Figure 11-1. Transient Thermal Response Curve for TSP3N80N

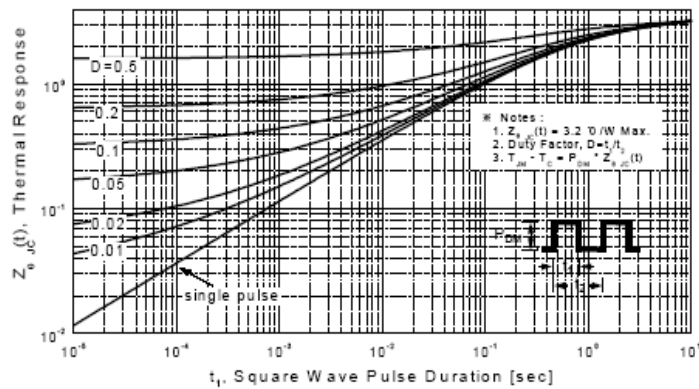
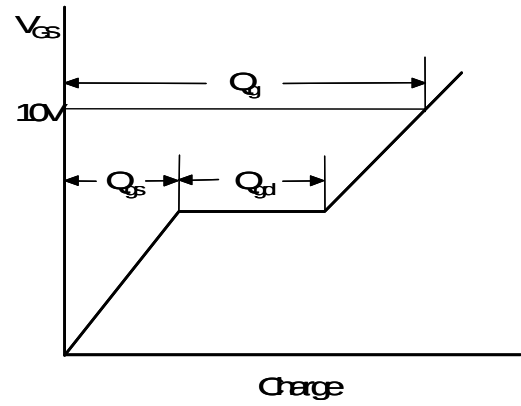
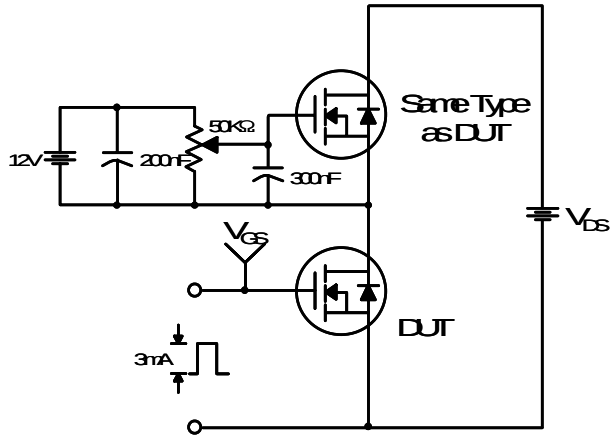


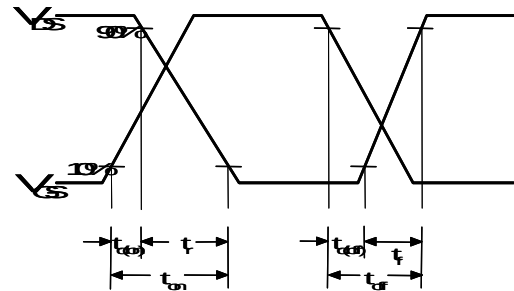
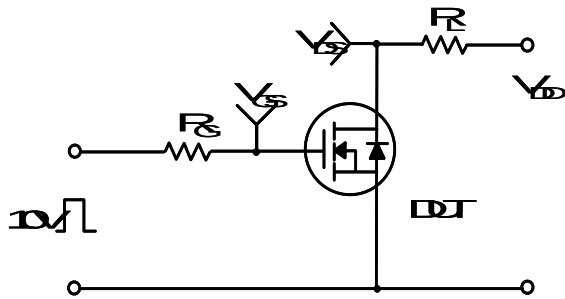
Figure 11-2. Transient Thermal Response Curve for TSF3N80N



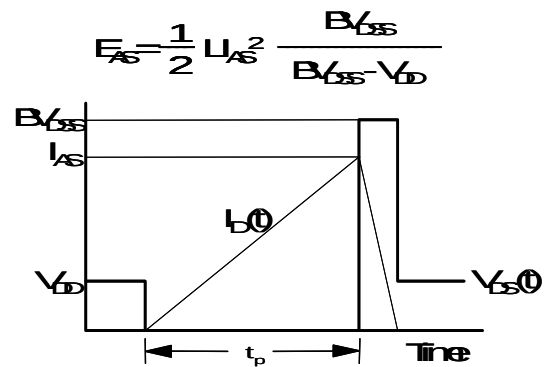
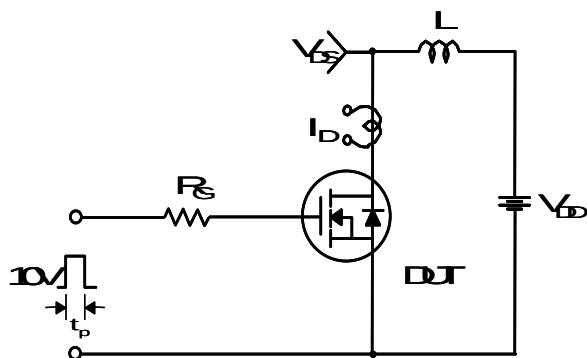
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

The diagram illustrates a test circuit and its corresponding waveforms for measuring the peak diode recovery dv/dt of a MOSFET's body diode.

Circuit Diagram:

- A MOSFET (DUT) is connected in a common-source configuration. Its source is grounded, and its drain is connected to a load inductor L and a supply voltage V_{DD} .
- A driver MOSFET (Same Type as DUT) is used to switch the DUT. Its gate is driven by a square wave V_{GS} through a gate resistor R_G . Its source is grounded, and its drain is connected to the DUT's source.
- The DUT's drain current is labeled I_{SD} , and the drain-source voltage is V_{DS} .
- Annotations:
 - dv/dt controlled by R_G
 - I_{SD} controlled by pulse period

Waveforms:

- V_{GS} (Driver):** A square wave pulse. The duty cycle is defined as $D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$. The pulse height is 10 V.
- I_{SD} (DUT):** The drain current of the DUT. It shows a forward current I_{FW} (Body Diode Forward Current) during the gate pulse, followed by a reverse current I_{RM} (Body Diode Reverse Current) during the recovery phase. The slope of the reverse current is labeled di/dt .
- V_{DS} (DUT):** The drain-source voltage of the DUT. It shows a forward voltage drop V_{SD} (Body Diode Forward Voltage Drop) during the forward current, followed by a recovery phase where the voltage rises to V_{DD} . The peak recovery dv/dt is indicated.

