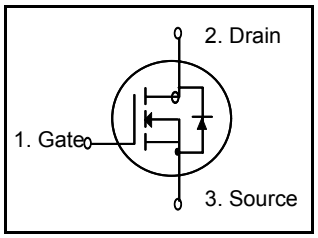
TSF8N65C

Pb Free Plating Product

7.5A,650V Insulated N-Channel Type Power MOSFETs

Features

- High ruggedness
- $R_{DS(on)}$ (Max 1.0 Ω)@V_{GS}=10V
- Gate Charge (Typical 48nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



BV_{DSS} = 650V

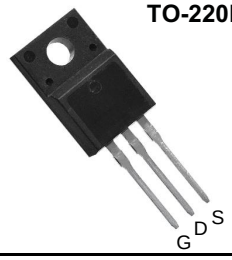
$R_{DS(ON)}$ = 1.0 ohm

I_D = 7.5A

General Description

This N-channel enhancement mode field-effect power transistor using THINKI Semiconductor advanced planar stripe, DMOS technology intended for off-line switch mode power supply.
Also, especially designed to minimize rds(on) and high rugged avalanche characteristics. The TO-220F pkg is well suited for adaptor power unit and small power inverter application.

TO-220F



Absolute Maximum Ratings

Symbol	Parameter		Value	Units
V_{DSS}	Drain to Source Voltage		650	V
I_D	Continuous Drain Current(@T_C = 25°C)		7.5	A
	Continuous Drain Current(@T_C = 100°C)		4.6	A
I_{DM}	Drain Current Pulsed	(Note 1)	30	A
V_{GS}	Gate to Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	560	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	14	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Total Power Dissipation(@T_C = 25 °C)		140	W
	Derating Factor above 25 °C		1.14	W/°C
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature		- 55 ~ 150	°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300	°C

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min.	Typ.	Max.	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		-	0.88	°C/W
$R_{\theta CS}$	Thermal Resistance, Case to Sink	-	0.5	-	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	62.5	°C/W

Electrical Characteristics (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	650	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature coefficient	I_D = 250uA, referenced to 25 °C	-	0.68	-	V/°C
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 600V, V_{GS} = 0V	-	-	10	uA
		V_{DS} = 480V, T_C = 125 °C	-	-	100	uA
I_{GSS}	Gate-Source Leakage, Forward	V_{GS} = 30V, V_{DS} = 0V	-	-	100	nA
	Gate-source Leakage, Reverse	V_{GS} = -30V, V_{DS} = 0V	-	-	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-state Resistance	V_{GS} =10 V, I_D = 4.5A	-	0.89	1	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} =0 V, V_{DS} =25V, f = 1MHz	-	820	980	pF
C_{oss}	Output Capacitance		-	140	170	
C_{rss}	Reverse Transfer Capacitance		-	43	50	
Dynamic Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD} =300V, I_D =7.5A, R_G =25Ω ※ **see fig. 13.** (Note 4, 5)	-	32	70	ns
t_r	Rise Time		-	85	160	
$t_{d(off)}$	Turn-off Delay Time		-	70	145	
t_f	Fall Time		-	65	120	
Q_g	Total Gate Charge	V_{DS} =480V, V_{GS} =10V, I_D =7.5A ※ **see fig. 12.** (Note 4, 5)	-	48	55	nC
Q_{gs}	Gate-Source Charge		-	6.8	-	
Q_{gd}	Gate-Drain Charge(Miller Charge)		-	25	-	

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
I_S	Continuous Source Current	Integral Reverse p-n Junction Diode in the MOSFET	-	-	7.5	A
I_{SM}	Pulsed Source Current		-	-	30	
V_{SD}	Diode Forward Voltage	I_S =7.5.0A, V_{GS} =0V	-	-	1.4	V
t_{rr}	Reverse Recovery Time	I_S=7.5A, V_{GS}=0V, dI_F/dt=100A/us	-	400	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.9	-	uC

※ NOTES
1. Repeativity rating : pulse width limited by junction temperature
2. L = 22.3mH, I_{AS} =7.50A, V_{DD} = 50V, R_G = 50Ω , Starting T_J = 25°C
3. I_{SD} ≤ 7.5A , di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse Width ≤ 300us, Duty Cycle ≤ 2%
5. Essentially independent of operating temperature.

Fig 1. On-State Characteristics

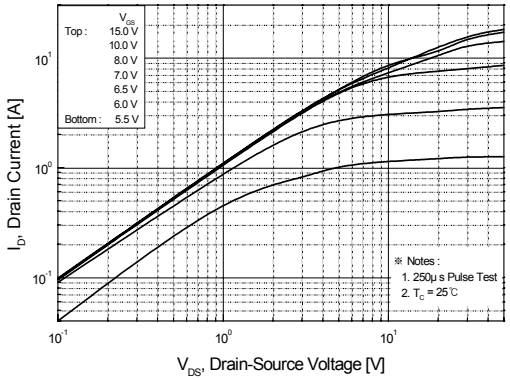


Fig 2. Transfer Characteristics

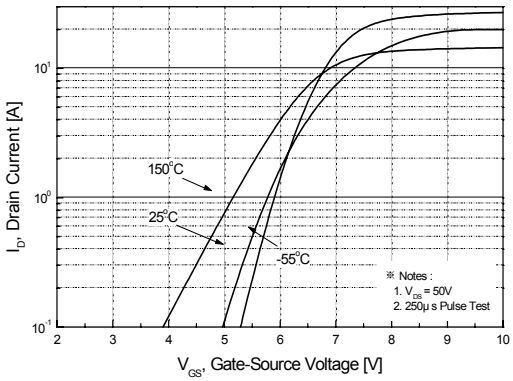


Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage

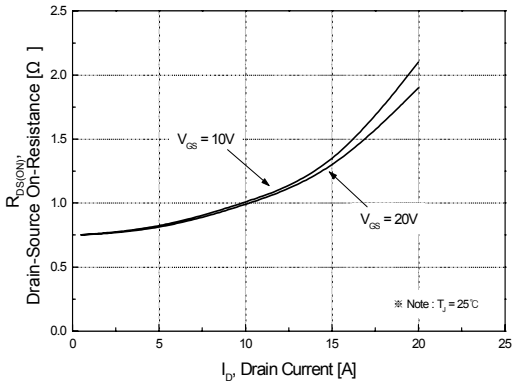


Fig 4. On State Current vs. Allowable Case Temperature

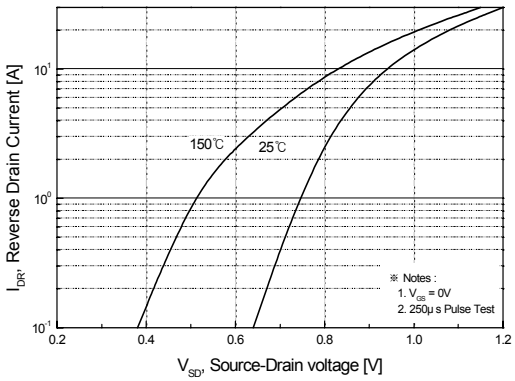


Fig 5. Capacitance Characteristics

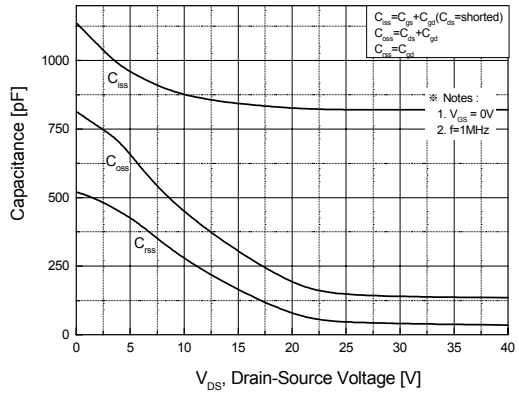


Fig 6. Gate Charge Characteristics

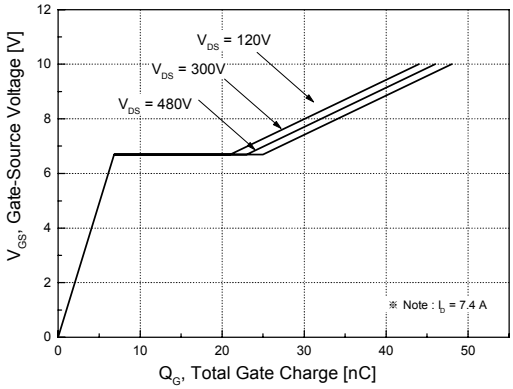


Fig 7. Breakdown Voltage Variation vs. Junction Temperature

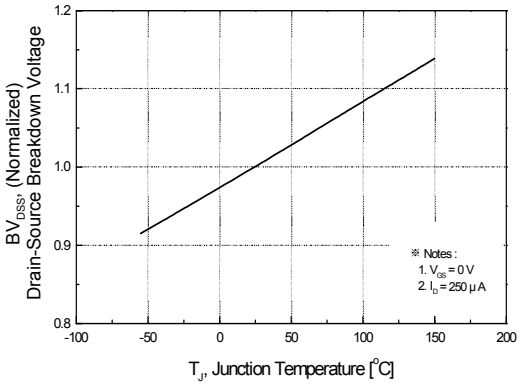


Fig 8. On-Resistance Variation vs. Junction Temperature

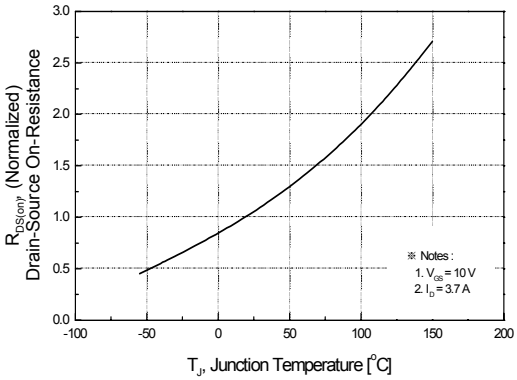


Fig 9. Maximum Safe Operating Area

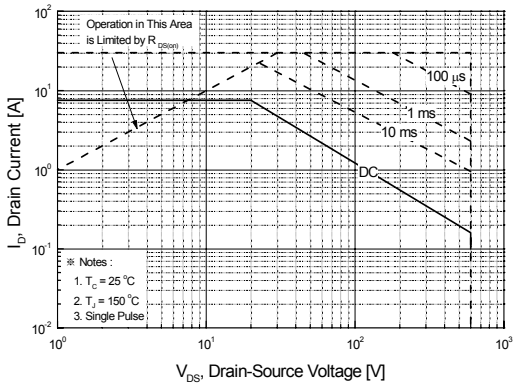


Fig 10. Maximum Drain Current vs. Case Temperature

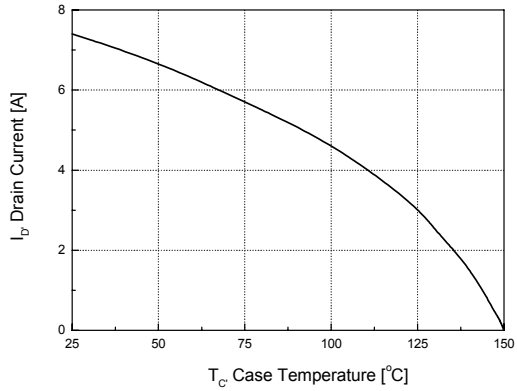


Fig 11. Transient Thermal Response Curve

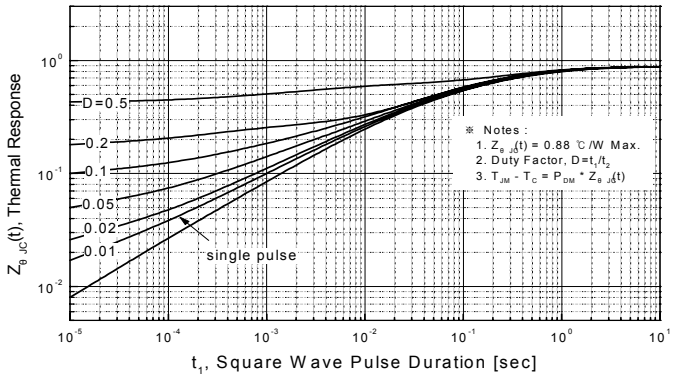


Fig. 12. Gate Charge Test Circuit & Waveforms

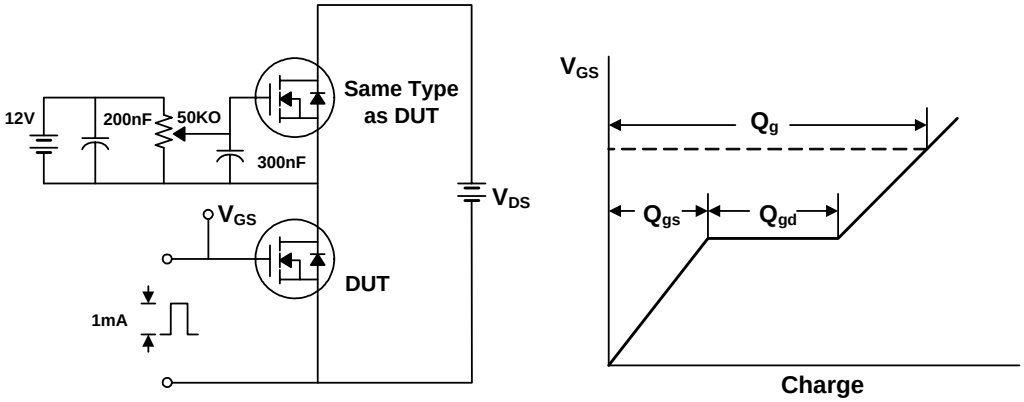


Fig 13. Switching Time Test Circuit & Waveforms

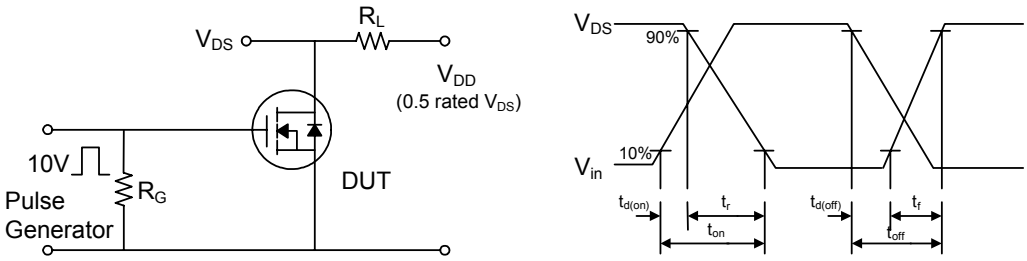


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

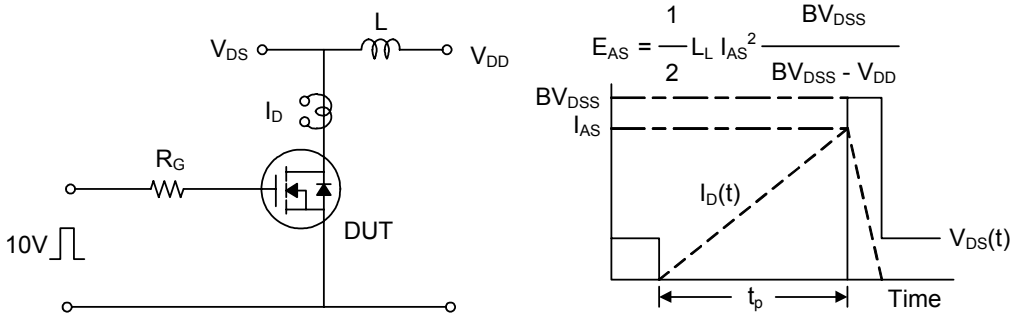


Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms