



TSH321

WIDE BANDWIDTH AND MOS INPUTS SINGLE OPERATIONAL AMPLIFIER

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 300MHz
- GAIN OF 2 STABILITY
- SLEW RATE : 400V/ μ s
- VERY FAST SETTTLING TIME : 60ns (0.1%)
- VERY HIGH INPUT IMPEDANCE

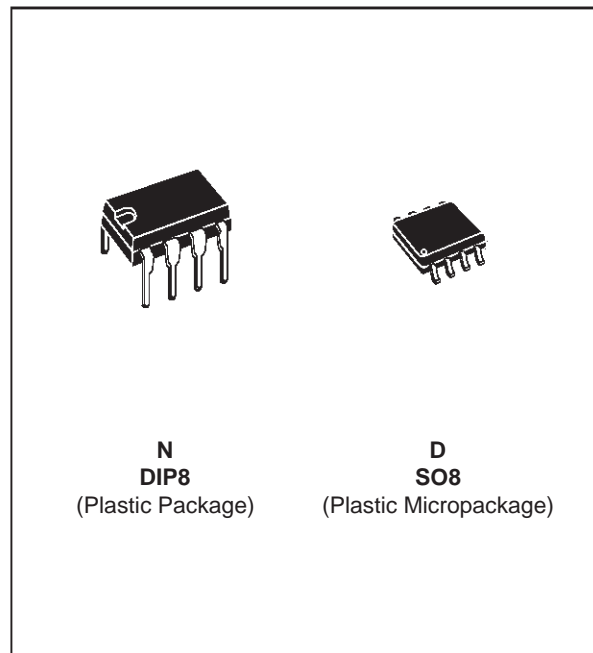
DESCRIPTION:

The TSH321 is a wideband monolithic operational amplifier, requiring a minimum close loop gain of 2 for stability.

The TSH321 features extremely high input impedance (typically greater than $10^{12}\Omega$) allowing direct interfacing with high impedance sources.

Low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The TSH321 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD883C-Class2.

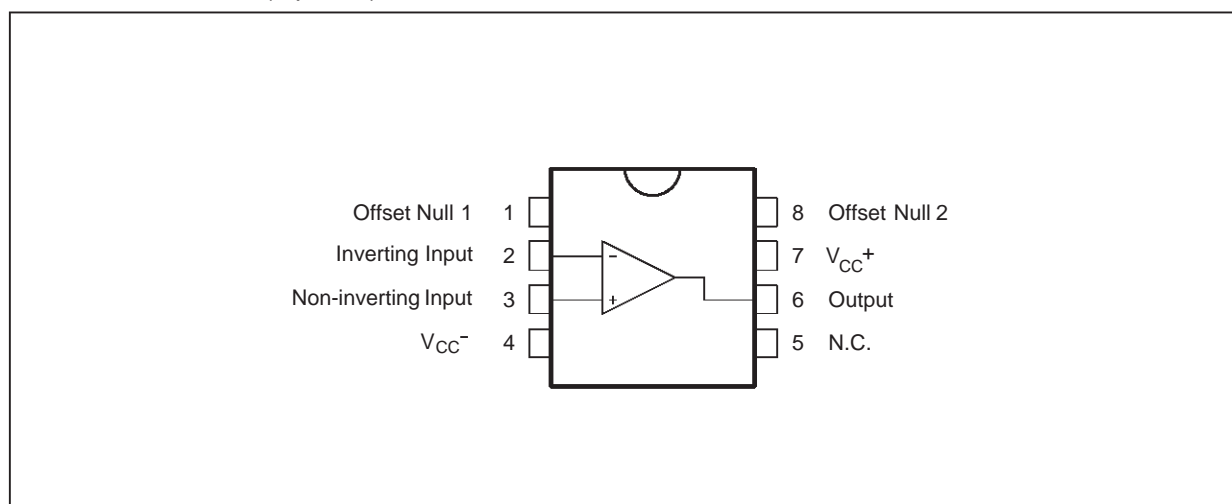


ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH321I	-40°C, 125°C	•	•

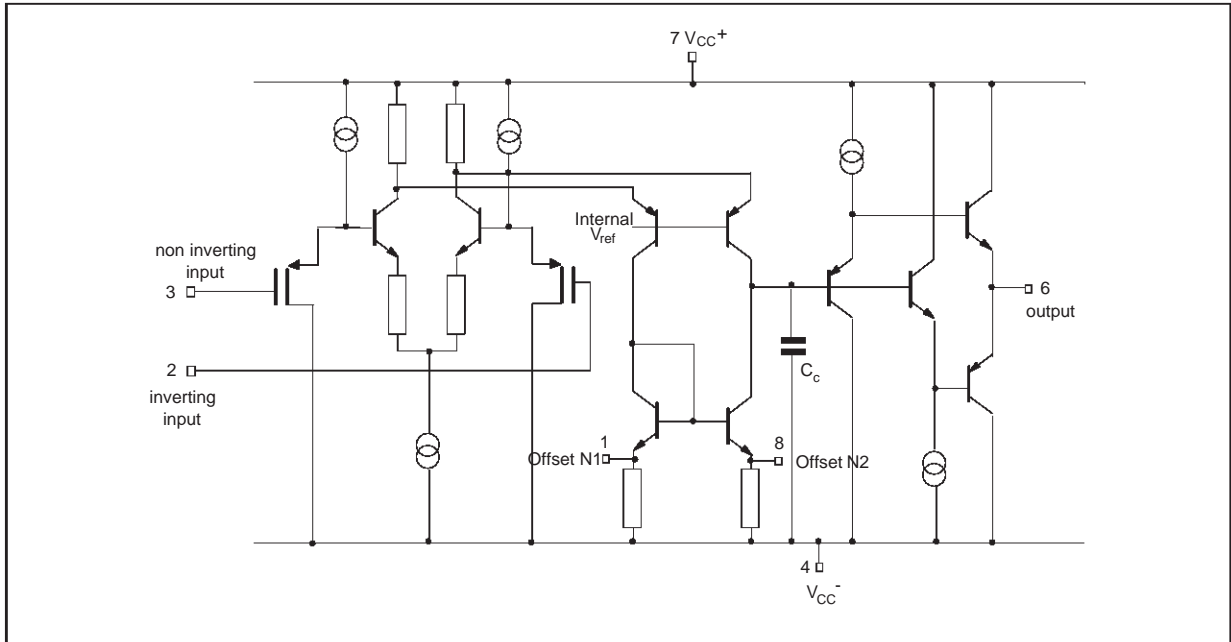
321-01.TBL

PIN CONNECTIONS (top view)



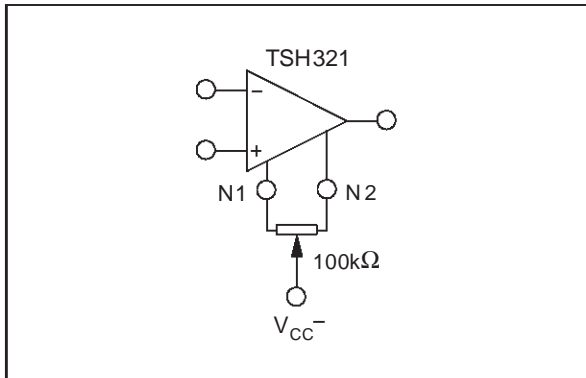
321-01.EPS

SCHEMATIC DIAGRAM



321-02.EPS

INPUT OFFSET VOLTAGE NULL CIRCUIT



321-03.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 7	V
V_{id}	Differential Input Voltage	± 5	V
V_i	Input Voltage Range	± 5	V
I_{in}	Current On Offset Null Pins	± 20	mA
T_{oper}	Operating Free-Air Temperature Range	TSH321I $-40^{\circ}\text{C}, 125^{\circ}\text{C}$	$^{\circ}\text{C}$

321-03.TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 3 to ± 6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC-} to $V_{CC+} - 3$	V

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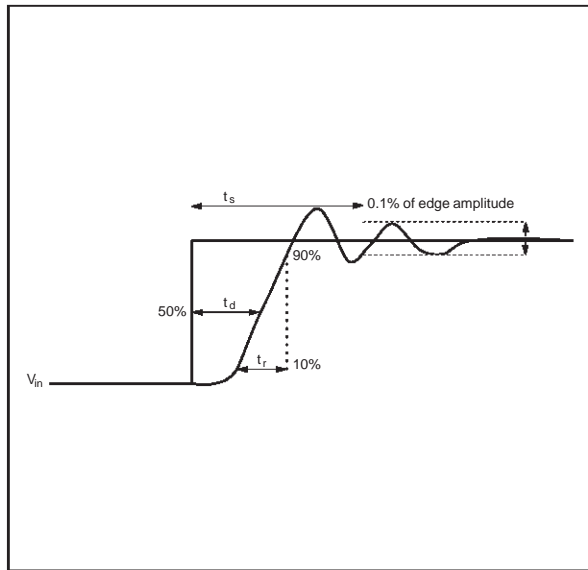
ELECTRICAL CHARACTERISTICSV_{CC} = ± 5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{io}	Input Offset Voltage T _{min} ≤ T _{amb} ≤ T _{max} .		0.5	10 12	mV
DV _{io}	Input Offset Voltage Drift T _{min} ≤ T _{amb} ≤ T _{max} .		10		μV/°C
I _{ib}	Input Bias Current		2	300	pA
I _{io}	Input Offset Current		2	200	pA
I _{CC}	Supply Current, no load T _{min} ≤ T _{amb} ≤ T _{max} .		V _{CC} = ± 5V 23 V _{CC} = ± 3V 21 V _{CC} = ± 6V 25 V _{CC} = ± 5V 32	30 28 40 32	mA
A _{vd}	Large Signal Voltage Gain V _o = ±2.5V				V/V
		R _L = ∞ 800 R _L = 100Ω 300 R _L = 50Ω 200	1300 850 650		
V _{icm}	Input Common Mode Voltage Range	-5 to +2	-5.5 to +2.5		V
CMR	Common Mode Rejection Ratio V _{ic} = V _{icm min.}	60	100		dB
SVR	Supply Voltage Rejection Ratio V _{CC} = ± 5V to ± 3V	50	70		dB
V _o	Output Voltage T _{min} ≤ T _{amb} ≤ T _{max} .	R _L = 100Ω ± 3 R _L = 50Ω ± 2.8 R _L = 100Ω ± 2.9 R _L = 50Ω ± 2.7	+3.5 -3.7 +3.3 -3.5		V
I _o	Output Short Circuit Current V _{id} = ±1V, V _o = 0V	± 50	± 100		mA
GBP	Gain Bandwidth Product A _{VCL} = 100, R _L = 100Ω, C _L = 15pF, f = 7.5MHz		300		MHz
SR	Slew Rate V _{in} = ± 1V, A _{VCL} = 2, R _L = 100Ω, C _L = 15pF	200	400		V/μs
e _n	Equivalent Input Voltage Noise R _S = 50Ω		fo = 1kHz 20 fo = 10kHz 18.2 fo = 100kHz 18.1 fo = 1MHz 18.2		$\frac{nV}{\sqrt{Hz}}$
K _{ov}	Overshoot V _{in} = ± 1V, A _{VCL} = 2, R _L = 100Ω, C _L = 15pF		15		%
t _s	Settling Time 0.1% - (note 1) V _{in} = ± 1V, A _{VCL} = -1		60		ns
t _r , t _f	Rise and Fall Time - (note 1) V _{in} = ±100mV, A _{VCL} = 2		2		ns
t _d	Delay Time - (note 1) V _{in} = ±100mV, A _{VCL} = 2		2		ns
∅ _m	Phase Margin A _{VM} = 2, R _L = 100Ω, C _L = 15pF		45		Degrees
THD	Total Harmonic Distortion A _{VCL} = 10, f = 1KHz, V _o = ± 2.5V, no load		0.02		%
FPB	Full Power Bandwidth - (note 2) V _o = 5V _{pp} , R _L = 100Ω V _o = 2V _{pp} , R _L = 100Ω		26 64		MHz

Note 1: See test waveform figure**Note 2:** Full power bandwidth = $\frac{SR}{\pi V_{opp}}$

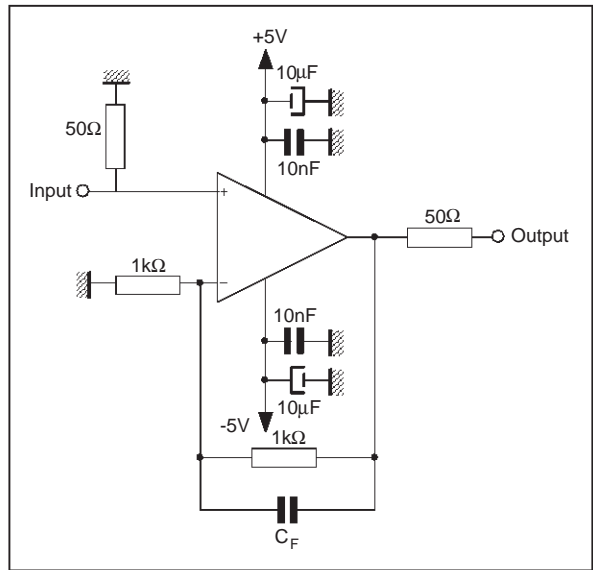
321-04-TBL

TEST WAVEFORM



321-04.EPS

EVALUATION CIRCUIT



321-05.EPS

PRINTED CIRCUIT LAYOUT

As for any high frequency device, a few rules must be observed when designing the PCB to get the best performances from this high speed op amp.

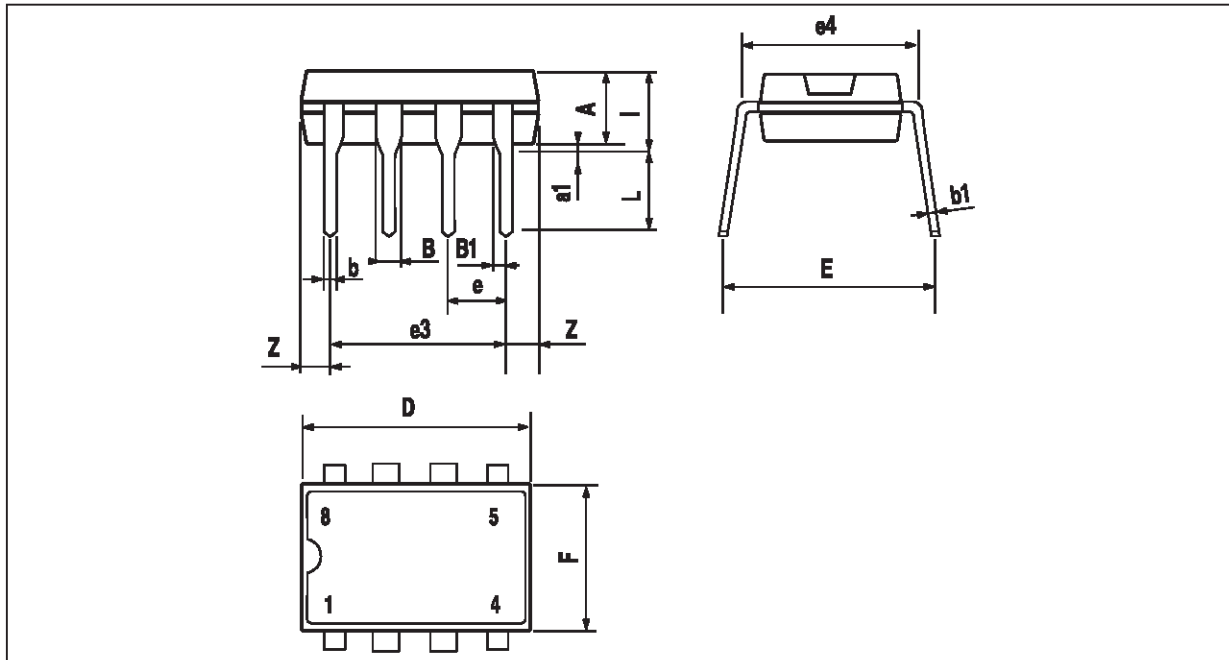
From the most to the least important points :

- Each power supply lead has to be bypassed to ground with a 10nF ceramic capacitor very close to the device and a 10μF tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitance and

inductance.

- Use small resistor values to decrease time constant with parasitic capacitance.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. One can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC DIP

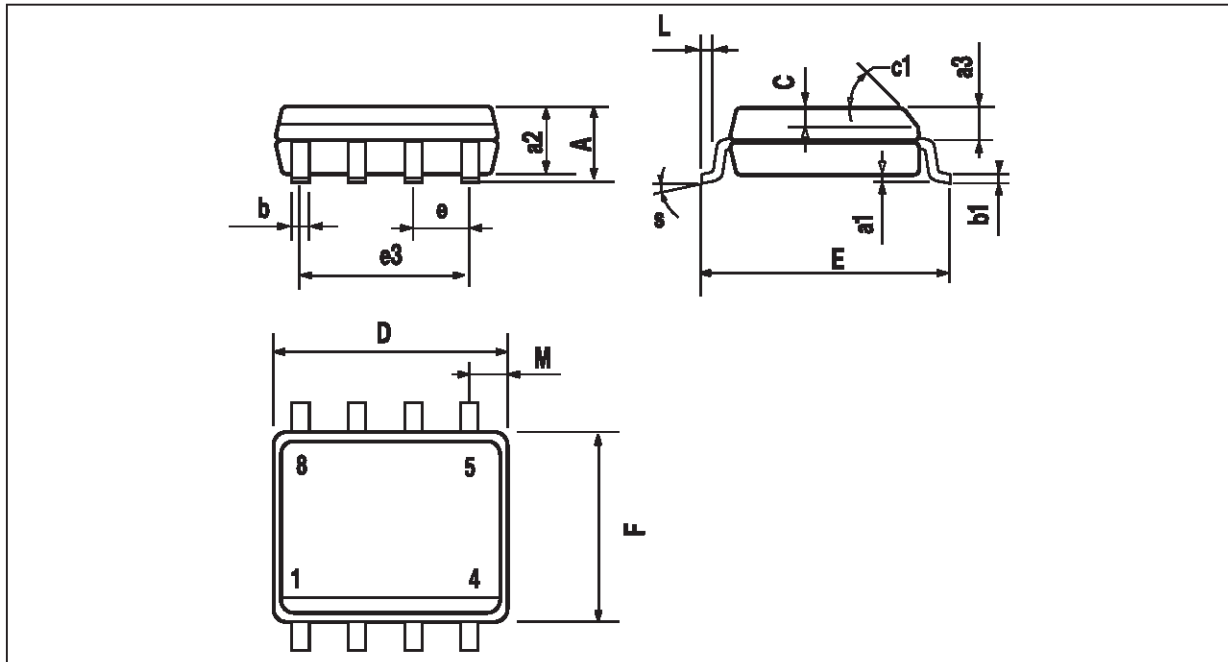


PM-DIP8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SO8.TBL

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