Two Speed Processor (for Coarse/Fine Synchro/Resolver Systems)

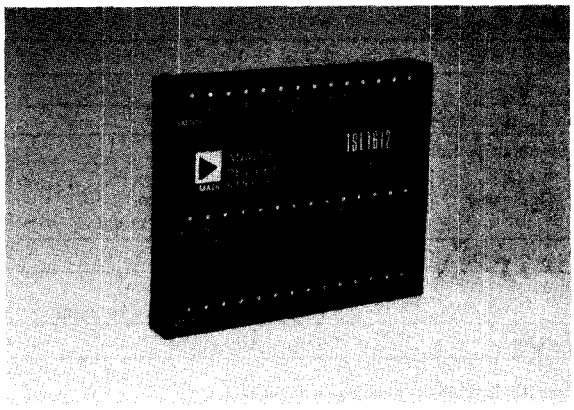
TSL1612

FEATURES

- **36:1, 18:1 or 9:1 Ratios with Same Module**
- **No False Output Readings**
- **Fast (500ns) Parallel Operation**
- **Easy to Use**
- **Up to 19-Bits Resolution**
- **Automatic Correction for Misalignment Between Synchros or Resolvers**
- **Low Profile – 0.4" (10.2mm)**

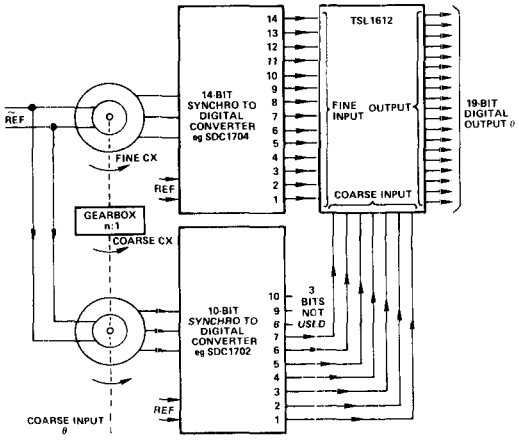
APPLICATIONS

- **Combining the Digital Outputs of Synchro-or-Resolver-to-Digital Converters in Coarse/Fine Systems**



GENERAL DESCRIPTION

The TSL1612 is used for combining the digital outputs of two Synchro- or Resolver-to Digital Converters in a mechanically or electrically geared coarse/fine system in order to produce a single unambiguous digital word representing the coarse shaft angle (see diagram).



DIGITIZING THE OUTPUT OF THE COARSE AND FINE SYNCHRO TRANSMITTERS (CX'S) IN A TWO SPEED SYSTEM

The unit described in this data sheet provides for ratios of 9:1, 18:1 and 36:1 in a single module. However, other ratios are sometimes encountered in coarse/fine Synchro or Resolver Systems, and details of special versions of the TSL1612 for use with ratios of 2:1 thru 35:1 are available on request.

The digital inputs to the TSL1612 are up to 14 bits from the fine converter and up to 7 bits from the coarse converter according to the gear ratio required. The output is up to 19-bits parallel binary angle data. The module may be used with any Synchro or Resolver Converters which produce parallel binary output.

MODELS AVAILABLE

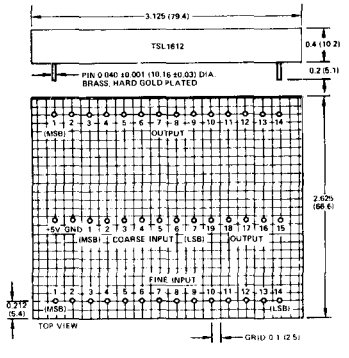
The standard TSL1612 which provides for ratios of 36:1, 18:1 and 9:1 has two options. They are as follows:

TSL1612500	0 to +70°C Operating Temperature
TSL1612600	-55°C to +105°C Operating Temperature

13

OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).



MATING SOCKET: CAMBION 450-3388-01-03

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Ratios:	36:1, 18:1, 9:1
Fine Synchro Input	Up to 14-Bits Parallel Binary Angle
Coarse Synchro Input	Up to 7-Bits Parallel Binary Angle
Logic Levels	DTL/TTL Compatible
Input Loading	2TTL Loads
Output Fan Out	5TTL Loads
Digital Output	Up to 19-Bits Parallel Binary Angle
Accuracy	±1LSB
Conversion Time	500ns
Temperature Range	
Storage	-55°C to +125°C
Operating	0 to +70°C Standard -55°C to +105°C Extended
Power Supplies	+5V ±5% @ 600mA
Size	3.125" X 2.625" X 0.4" 79.4mm X 66.6mm X 10.2mm
Weight	3.5ozs. 100 grams

Specifications subject to change without notice.

CONNECTING THE TSL1612

For all ratios the fine SDC outputs connect directly to the fine TSL1612 inputs i.e. bit (1) out to bit (1) in through to bit 14 out to bit 14 in. If a Synchro- or Resolver-to-Digital Converter with a resolution of less than 14 bits is used to provide the fine input, then the unused inputs to the TSL1612 should be grounded and the output accuracy will be reduced accordingly by the same number of bits.

The connections of the coarse inputs and the TSL1612 outputs change according to the ratio to be obtained ie:-

36:1 RATIOS

Bits 1 to 7 from the coarse Synchro- or Resolver-to-Digital Converter should be connected to bits 1 to 7 on the coarse input of the TSL1612. The output is taken from bits 1 to 19.

18:1 RATIOS

Bits 1 to 6 from the coarse Synchro- or Resolver-to-Digital Converter should be connected to bits 2 to 7 on the coarse input of the TSL1612. The output is taken from bits 2 to 19 (bit 2 is the MSB of the output word).

9:1 RATIOS

Bits 1 to 5 from the coarse Synchro- or Resolver-to-Digital Converter should be connected to bits 3 to 7 on the coarse input of the TSL1612. The output is taken from bits 3 to 19 (bit 3 is the MSB of the output word).

CORRECTION FOR MISALIGNMENT OF THE COARSE AND FINE SYNCHROS OR RESOLVERS

In the two speed digital converters which receive inputs from both the coarse and fine synchros, circumstances will occur when the coarse angle determined by the most significant digits of fine synchro will conflict with the overlapping least significant digits of the coarse synchro. (This is due to the backlash in the gearing or misalignment in the synchros causing different readings at the major transition points.) Digital logic circuits for resolving this conflict are included in the TSL1612. The digital reading from the fine synchro is made to dominate in the overlapping region, and a correction is made bringing the coarse reading into line to provide an unambiguous digital representation of the angle of the coarse shaft. The TSL1612 will correct for a misalignment of (90 divided by the ratio) degrees.

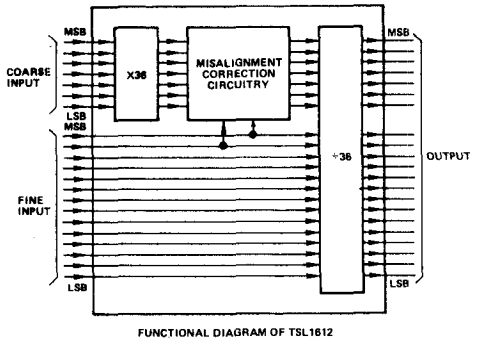
DATA TRANSFER FROM THE TSL1612

Data transfer can be made in a number of ways in which two are listed below.

1. The BUSY outputs of the fine and coarse Synchro/Resolver-to-Digital Converter can be "OR"ed together to give an indication of when neither converter is being updated (see appropriate converter data sheet). The data can then be taken from the TSL1612. (The conversion time of the TSL1612 is usually insignificant.)
2. The INHIBIT can be applied to both the Synchro/Resolver-to-Digital Converters simultaneously in order to freeze their outputs (see appropriate data sheet). When the inputs to the TSL1612 are frozen the output data can be taken. In cases where 12 bits is sufficient for the fine input, the three-state input SDC1725 Synchro/Resolver-to-Digital Converter should be used in conjunction with the SDC1726 on the coarse input. These converters allow the INHIBIT to be used without any risk of opening the internal converter tracking loop (see data sheet).

THEORY OF OPERATION

The theory of operation of the TSL1612 is shown in the diagram below.



FUNCTIONAL DIAGRAM OF TSL1612

ORDERING INFORMATION

Order:-

TSL1612500 for 0 to +70°C Operating Temperature Range.

TSL1612600 for -55°C to +105°C Operating Temperature Range.