

# TSL201CL

## 64 × 1 Linear Sensor Array

### General Description

The TSL201CL linear sensor array consists of a 64 × 1 array of photodiodes and associated charge amplifier circuitry. The pixels measure 120µm (H) by 68µm (W) with 125µm center-to-center spacing and 57µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

The TSL201CL is intended for use in a wide variety of applications including mark detection and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning as well as optical linear and rotary encoding.

*Ordering Information and Content Guide appear at end of datasheet.*

### Key Benefits & Features

The benefits and features of the TSL201CL, 64 × 1 Linear Sensor Array are listed below:

**Figure 1:**  
Added Value of Using TSL201CL

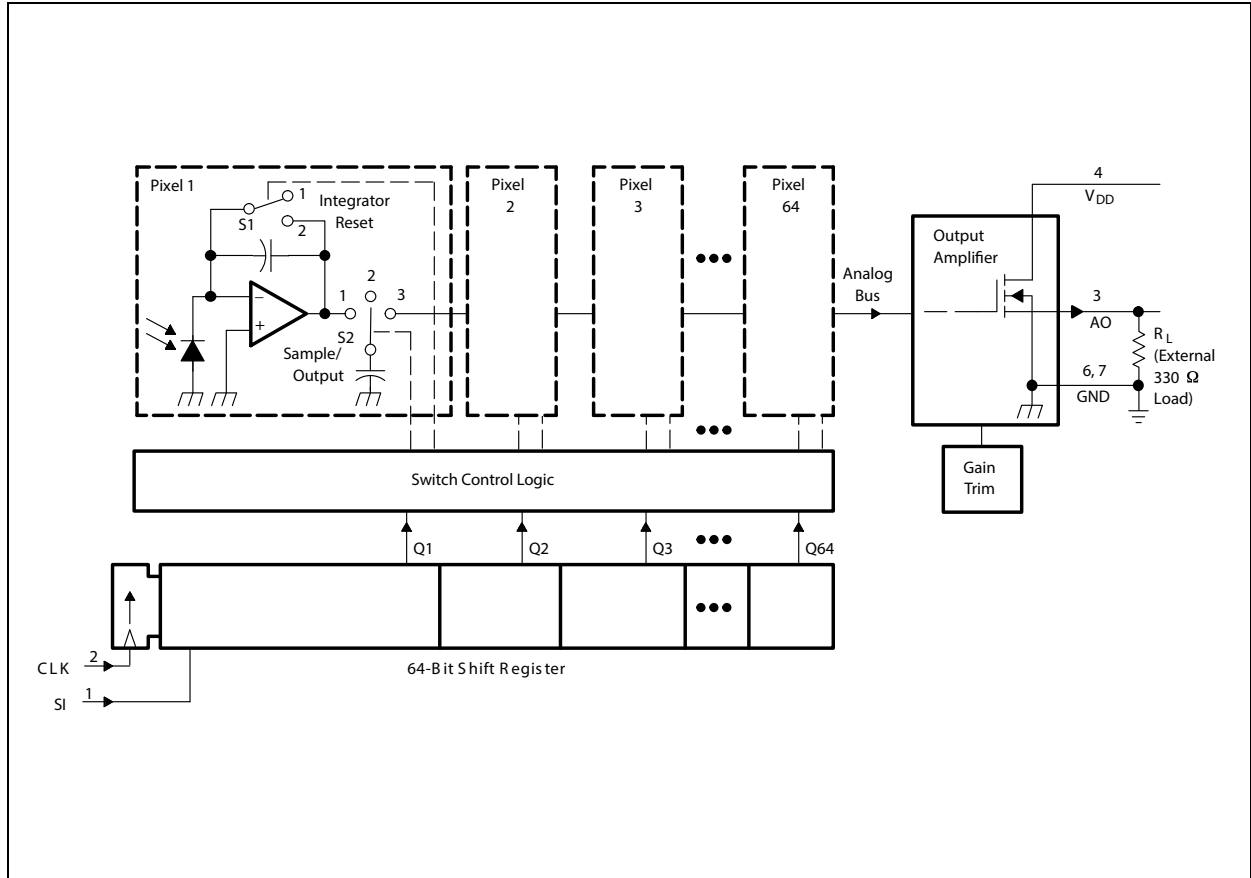
Benefits	Features
<ul style="list-style-type: none"> <li>Provides high density pixel count</li> </ul>	<ul style="list-style-type: none"> <li>64 x 1 sensor-element organization</li> </ul>
<ul style="list-style-type: none"> <li>Enables high resolution scanning</li> </ul>	<ul style="list-style-type: none"> <li>200 Dots-Per-Inch (DPI) sensor pitch</li> </ul>
<ul style="list-style-type: none"> <li>Enables capacitive threshold sensing</li> </ul>	<ul style="list-style-type: none"> <li>High linearity and uniformity</li> </ul>
<ul style="list-style-type: none"> <li>Provides full dynamic range</li> </ul>	<ul style="list-style-type: none"> <li>Rail-to-rail output swing</li> </ul>

- Wide dynamic range: 2000:1 (66dB)
- Output referenced to ground
- Low image lag: 0.5% Typ
- Operation to 5MHz
- Single 5V supply
- Replacement for TSL201, TSL201R, and TSL201R-LF

### Block Diagram

The functional blocks of this device are shown below:

Figure 2:  
TSL201CL Block Diagram

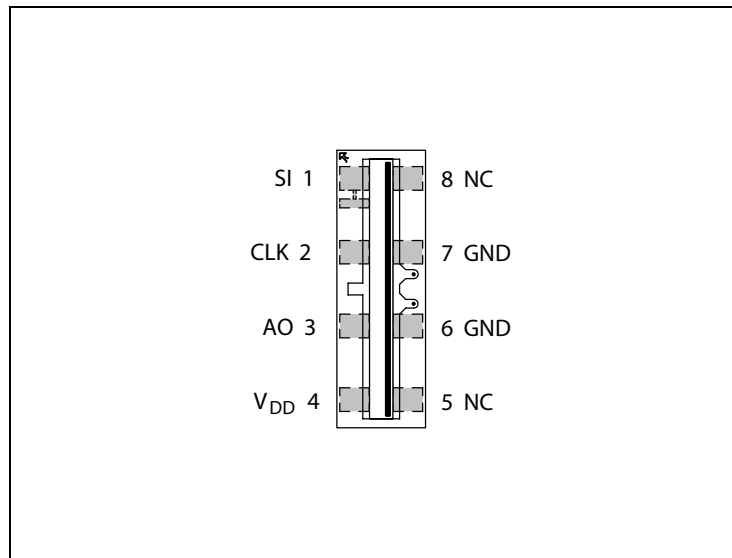


## Pin Assignment

The TSL201CL pin assignment is described below:

**Figure 3:**  
Pin Diagram (Top View)

**CL Package:**  
NC - No internal connection



**Figure 4:**  
Terminal Functions

Terminal		Description
Name	No.	
SI	1	Serial input. SI defines the start of the data-out sequence.
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
AO	3	Analog output.
V <sub>DD</sub>	4	Supply voltage. Supply voltage for both analog and digital circuits.
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.

## Detailed Description

The sensor consists of 64 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel. During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time. The integration time is the interval between two consecutive output periods.

The output and reset of the integrators is controlled by a 64-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI for one positive going clock edge (see [Figure 10](#) and [Figure 11](#))<sup>1</sup>. As the SI pulse is clocked through the 64-bit shift register, the charge on the sampling capacitor of each pixel is sequentially connected to a charge-coupled output amplifier that generates a voltage output, AO. When the bit position goes low, the pixel integrator is reset. On the 65th clock rising edge, the SI pulse is clocked out of the shift register and the output assumes a high-impedance state. Note that this 65th clock pulse is required to terminate the output of the 64th pixel and return the internal logic to a known state. A subsequent SI pulse can be presented as early as the 66th clock pulse, thereby initiating another pixel output cycle.

The voltage developed at analog output (AO) is given by:

$$(EQ1) \quad V_{out} = V_{drk} + (R_e) (E_e) (t_{int})$$

where:

- $V_{out}$  is the analog output voltage for white condition
- $V_{drk}$  is the analog output voltage for dark condition
- $R_e$  is the device responsivity for a given wavelength of light given in  $V/(\mu J/cm^2)$
- $E_e$  is the incident irradiance in  $\mu W/cm^2$
- $t_{int}$  is integration time in seconds

AO is driven by a source follower that requires an external pulldown resistor (330 $\Omega$  typical). The output is nominally 0V for no light input, 2V for normal white-level, and 3.4V for saturation light level. When the device is not in the output phase, AO is in a high impedance state.

A 0.1 $\mu$ F bypass capacitor should be connected between  $V_{DD}$  and ground as close as possible to the device.

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1. For proper operation, after meeting the minimum hold time condition, SI must go low before the next rising edge of the clock.

## Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**  
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD}$	Supply voltage range	-0.3	6	V
$V_I$	Input voltage range	-0.3	$V_{DD} + 0.3V$	V
$I_{IK}$	Input clamp current, ( $V_I < 0$ ) or ( $V_I > V_{DD}$ )	-20	20	mA
$I_{OK}$	Output clamp current, ( $V_O < 0$ ) or ( $V_O > V_{DD}$ )	-25	25	mA
$V_O$	Voltage range applied to any output in the high impedance or power-off state	-0.3	$V_{DD} + 0.3V$	V
$I_O$	Continuous output current, ( $V_O = 0$ to $V_{DD}$ )	-25	25	mA
	Continuous current through $V_{DD}$ or GND	-40	40	mA
$I_O$	Analog output current range	-25	25	mA
$T_A$	Operating free-air temperature range	-25	85	°C
$T_{strg}$	Storage temperature range	-25	85	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds <sup>(1)</sup>		260	°C
$ESD_{HBM}$	ESD tolerance, human body model	±2000		V

**Note(s):**

1. Not recommended for solder reflow.

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**  
Recommended Operating Conditions (see [Figure 10](#) and [Figure 11](#))

Symbol	Parameter	Min	Nom	Max	Unit
$V_{DD}$	Supply voltage	4.5	5	5.5	V
$V_I$	Input voltage	0		$V_{DD}$	V
$V_{IH}$	High-level input voltage	2		$V_{DD}$	V
$V_{IL}$	Low-level input voltage	0		0.8	V
$\lambda$	Wavelength of light source	400		1000	nm
$f_{clock}$	Clock frequency	5		5000	kHz
$t_{int}$	Sensor integration time	0.013		100	ms
$T_A$	Operating free-air temperature	0		70	°C
$R_L$	Load resistance	300		4700	$\Omega$
$C_L$	Load capacitance			470	pF

**Figure 7:**  
**Electrical Characteristics at  $f_{\text{clock}} = 1\text{MHz}$ ,  $V_{\text{DD}} = 5\text{V}$ ,  $T_{\text{A}} = 25^{\circ}\text{C}$ ,  $\lambda_{\text{p}} = 640\text{nm}$ ,  $t_{\text{int}} = 5\text{ms}$ ,  $R_{\text{L}} = 330\Omega$ ,  
 $E_{\text{e}} = 16.5\mu\text{W}/\text{cm}^2$  (unless otherwise noted)**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{\text{out}}$	Analog output voltage (white, average over 64 pixels)	See note (1)	1.6	2	2.4	V
$V_{\text{drk}}$	Analog output voltage (dark, average over 64 pixels)	$E_{\text{e}} = 0$	0	50	120	mV
PRNU	Pixel response nonuniformity	See note (2) and See note (3)		$\pm 4\%$	$\pm 7.5\%$	
	Nonlinearity of analog output voltage	See note (3)		$\pm 0.4\%$		FS
	Output noise voltage	See note (4)		1		mVrms
$R_{\text{e}}$	Responsivity	See note (5)	18	23		V/ ( $\mu\text{W}/\text{cm}^2$ )
SE	Saturation exposure	See note (6)		142		nJ/cm <sup>2</sup>
$V_{\text{sat}}$	Analog output saturation voltage		2.5	3.4		V
DSNU	Dark signal nonuniformity	All pixels, $E_{\text{e}} = 0$ (7)		25	120	mV
IL	Image lag	See note (8)		0.5%		
$I_{\text{DD}}$	Supply current, output idle			3.4	5	mA
$I_{\text{IH}}$	High-level input current	$V_{\text{I}} = V_{\text{DD}}$			1	$\mu\text{A}$
$I_{\text{IL}}$	Low-level input current	$V_{\text{I}} = 0$			1	$\mu\text{A}$
$C_{\text{i(SI)}}$	Input capacitance, SI			5		pF
$C_{\text{i(CLK)}}$	Input capacitance, CLK			5		pF

**Note(s):**

- The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640nm.
- PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated at the white irradiance level. PRNU includes DSNU.
- Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
- RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
- $R_{\text{e(min)}} = [V_{\text{out(min)}} - V_{\text{drk(max)}}] \div (E_{\text{e}} \times t_{\text{int}})$
- Minimum saturation exposure is calculated using the minimum  $V_{\text{sat}}$ , the maximum  $V_{\text{drk}}$ , and the maximum  $R_{\text{e}}$ .
- DSNU is the difference between the maximum and minimum output voltage in the absence of illumination.
- Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$\text{IL} = \frac{V_{\text{out(IL)}} - V_{\text{drk}}}{V_{\text{out(white)}} - V_{\text{drk}}} \times 100$$

**Figure 8:**  
Timing Requirements (see Figure 10 and Figure 11)

Symbol	Parameter	Min	Nom	Max	Unit
$t_{su(SI)}$	Setup time, serial input <sup>(1)</sup>	20			ns
$t_{h(SI)}$	Hold time, serial input <sup>(1), (2)</sup>	0			ns
$t_w$	Pulse duration, clock high or low	50			ns
$t_r, t_f$	Input transition (rise and fall) time	0		500	ns

**Note(s):**

1. Input pulses have the following characteristics:  $t_r = 6\text{ns}$ ,  $t_f = 6\text{ns}$ .
2. SI must go low before the rising edge of the next clock pulse.

**Figure 9:**  
Dynamic Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (see Figure 11)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_s$	Analog output settling time to $\pm 1\%$	$R_L = 330\Omega, C_L = 10\text{pF}$		185		ns



## Typical Operating Characteristics

Figure 10:  
Timing Waveforms

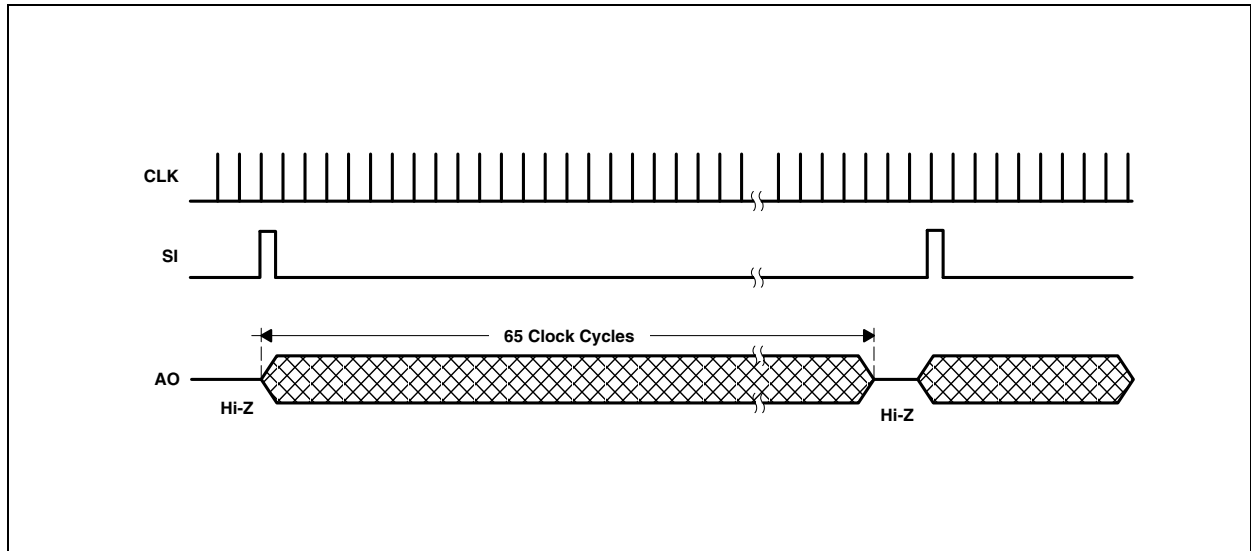


Figure 11:  
Operational Waveforms

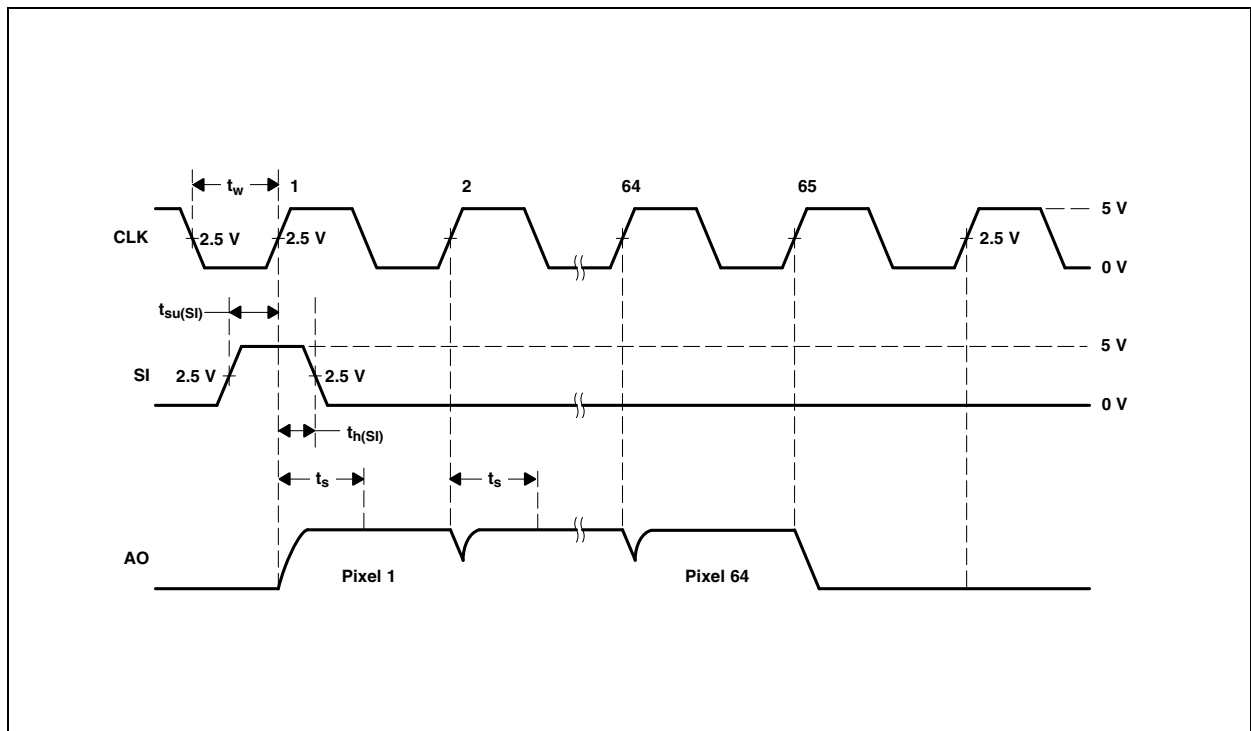


Figure 12:  
Photodiode Spectral Responsivity

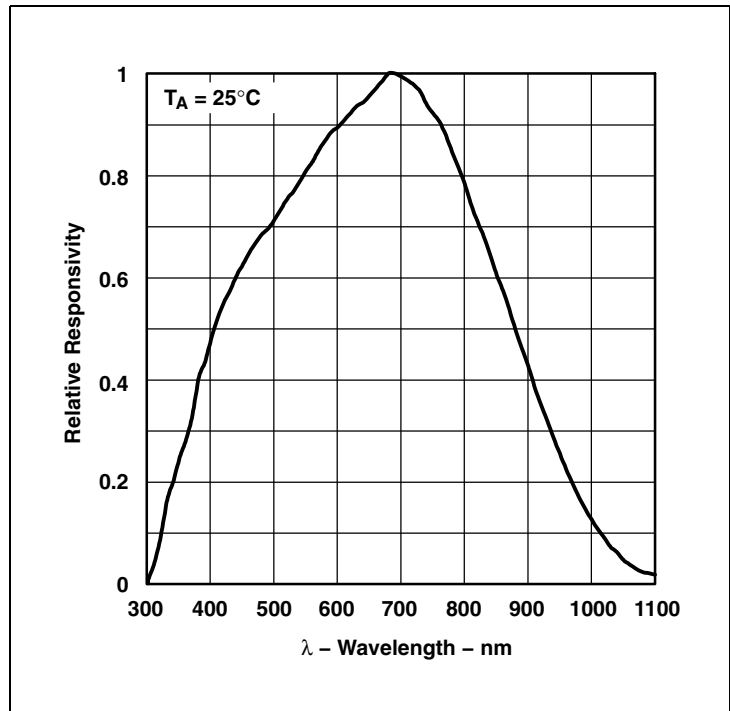
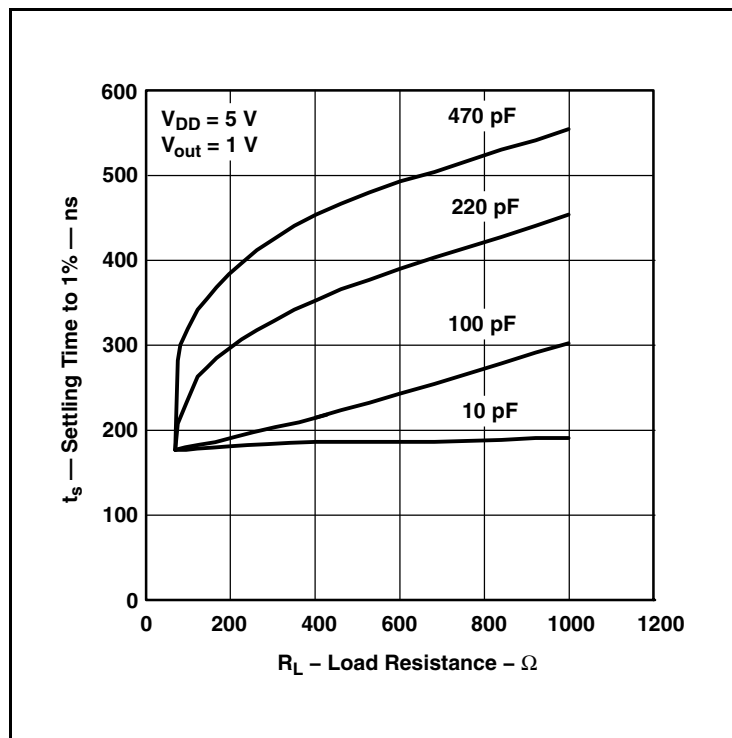


Figure 13:  
Analog Output Settling Time vs. Load Capacitance and Resistance



## Application Information

### Power Supply Considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01 $\mu$ F to 0.1 $\mu$ F capacitor with short leads mounted close to the device package.

### Integration Time

The integration time of the linear array is the period during which light is sampled and charge accumulates on each pixel's integrating capacitor. The flexibility to adjust the integration period is a powerful and useful feature of the **ams** TSL2xx linear array family. By changing the integration time, a desired output voltage can be obtained on the output pin while avoiding saturation for a wide range of light levels.

Each pixel of the linear array consists of a light-sensitive photodiode. The photodiode converts light intensity to a voltage. The voltage is sampled on the Sampling Capacitor by closing switch S2 (position 1) (see [Figure 2](#)). Logic controls the resetting of the Integrating Capacitor to zero by closing switch S1 (position 2).

At SI input (Start Integration), pixel 1 is accessed. During this event, S2 moves from position 1 (sampling) to position 3 (holding). This holds the sampled voltage for pixel 1. Switch S1 for pixel 1 is then moved to position 2. This resets (clears) the voltage previously integrated for that pixel so that pixel 1 is now ready to start a new integration cycle. When the next clock period starts, the S1 switch is returned to position 1 to be ready to start integrating again. S2 is returned to position 1 to start sampling the next light integration. Then the next pixel starts the same procedure. The integration time is the time from a specific pixel read to the next time that pixel is read again. If either the clock speed or the time between successive SI pulses is changed, the integration time will vary. After the final ( $n^{\text{th}}$ ) pixel in the array is read on the output, the output goes into a high-impedance mode. A new SI pulse can occur on the ( $n+1$ ) clock causing a new cycle of integration/output to begin. Note that the time between successive SI pulses must not exceed the maximum integration time of 100ms.

The minimum integration time for any given array is determined by time required to clock out all the pixels in the array and the time to discharge the pixels. The time required to discharge the pixels is a constant. Therefore, the minimum integration period is simply a function of the clock frequency and the number of pixels in the array. A slower clock speed increases the minimum integration time and reduces the maximum light level for saturation on the output. The minimum integration time shown in this data sheet is based on the maximum clock frequency of 5 MHz.

The minimum integration time can be calculated from the equation:

$$(EQ2) \quad T_{int(min)} = \left( \frac{1}{\text{maximum clock frequency}} \right) \times n$$

where:

n is the number of pixels

In the case of the TSL201CL, the minimum integration time would be:

$$T_{int(min)} = 200ns \times 64 = 12.8\mu s$$

It is important to note that not all pixels will have the same integration time if the clock frequency is varied while data is being output.

It is good practice on initial power up to run the clock ( $n+1$ ) times after the first SI pulse to clock out indeterminate data from power up. After that, the SI pulse is valid from the time following ( $n+1$ ) clocks. The output will go into a high-impedance state after the  $n+1$  high clock edge. It is good practice to leave the clock in a low state when inactive because the SI pulse required to start a new cycle is a low-to-high transition.

The integration time chosen is valid as long as it falls in the range between the minimum and maximum limits for integration time. If the amount of light incident on the array during a given integration period produces a saturated output (Max Voltage output), then the data is not accurate. If this occurs, the integration period should be reduced until the analog output voltage for each pixel falls below the saturation level. The goal of reducing the period of time the light sampling window is active is to lower the output voltage level to prevent saturation. However, the integration time must still be greater than or equal to the minimum integration period.

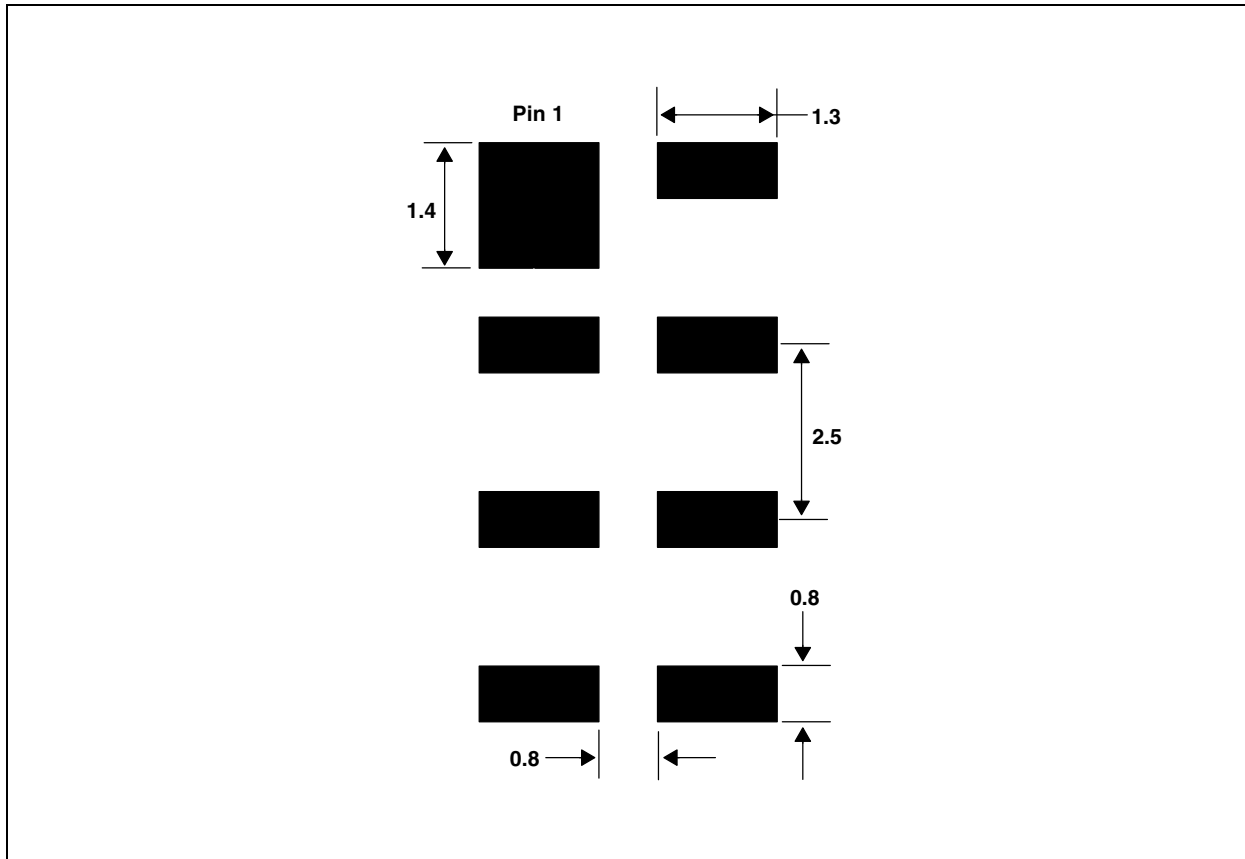
If the light intensity produces an output below desired signal levels, the output voltage level can be increased by increasing the integration period provided that the maximum integration time is not exceeded. The maximum integration time is limited by the length of time the integrating capacitors on the pixels can hold their accumulated charge. The maximum integration time should not exceed 100 ms for accurate measurements.

Although the linear array is capable of running over a wide range of operating frequencies up to a maximum of 5 MHz, the speed of the A/D converter used in the application is likely to be the limiter for the maximum clock frequency. The voltage output is available for the whole period of the clock, so the setup and hold times required for the analog-to-digital conversion must be less than the clock period.

## Application Information: Hardware

Suggested PCB pad layout guidelines for the CL package are shown in [Figure 14](#).

**Figure 14:**  
Suggested CL Package PCB Layout

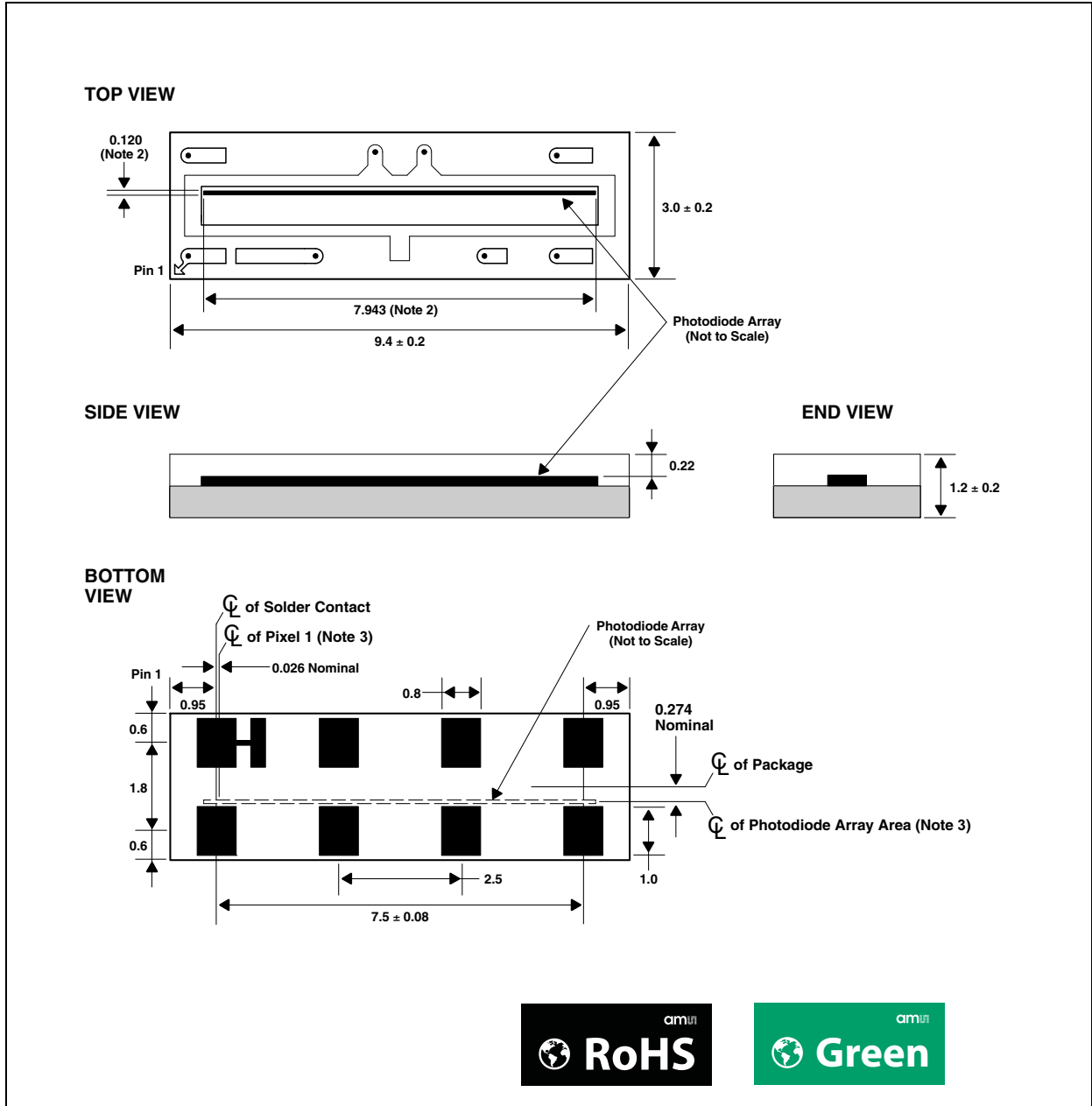


**Note(s):**

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

## Package Drawings & Markings

Figure 15:  
Package CL Configuration

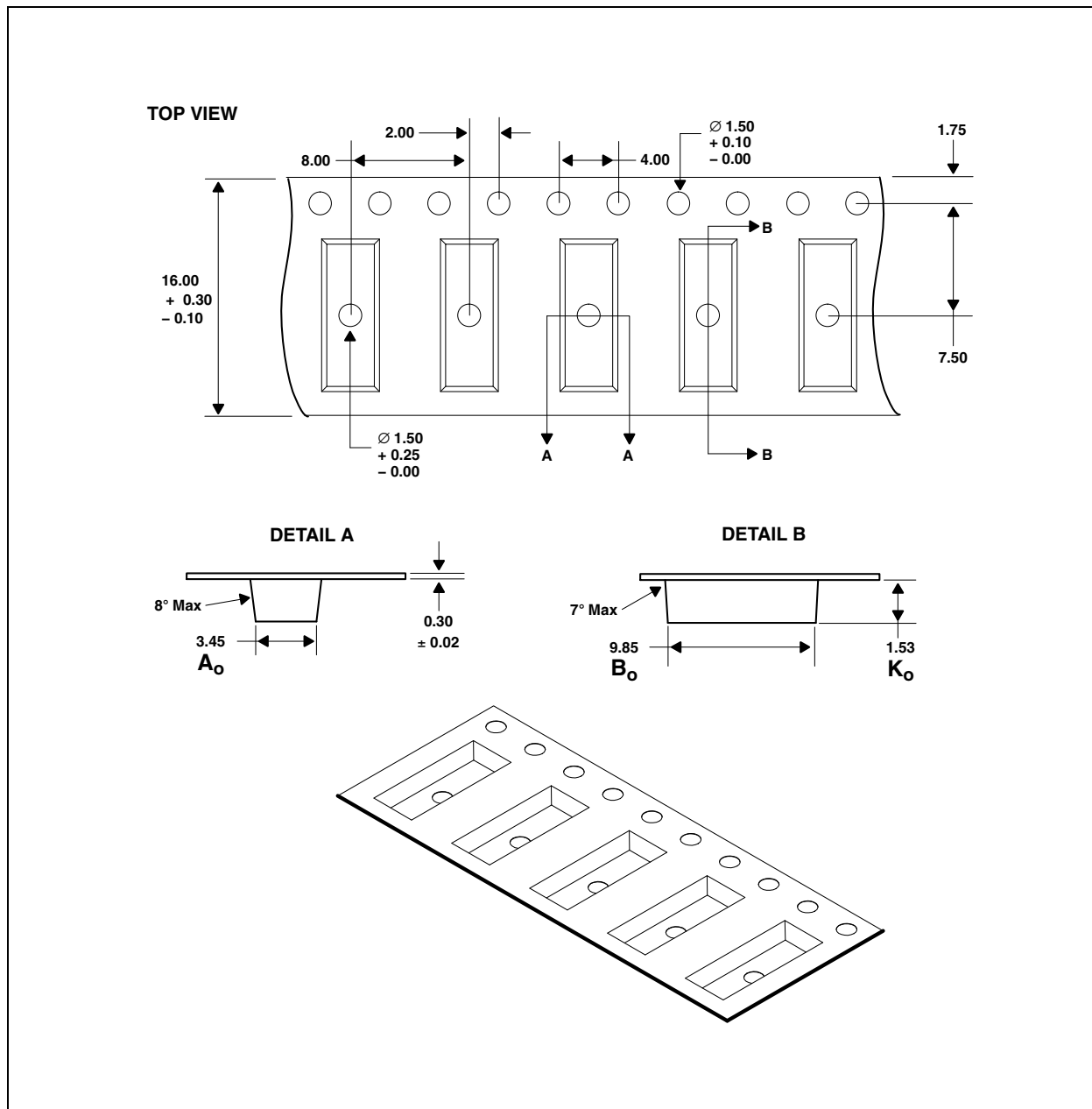


**Note(s):**

1. All linear dimensions are in millimeters. Dimension tolerance is  $\pm 0.05$ mm unless otherwise noted.
2. Nominal photodiode array dimension. The array is made up of 64 pixels with pixel #1 closer to Pin 1. Each pixel is  $68\mu\text{m}$  wide by  $120\mu\text{m}$  high, spaced on  $125\mu\text{m}$  centers.
3. The die is centered within the package within a tolerance of  $\pm 0.05$ mm.
4. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.56.
5. Contact finish is soft gold plated.
6. This package contains no lead (Pb).
7. This drawing is subject to change without notice.

## Carrier Tape & Reel Information

Figure 16:  
Package CL Carrier Tape



**Note(s):**

1. All linear dimensions are in millimeters. Dimension tolerance is  $\pm 0.10$  mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing  $A_o$ ,  $B_o$ , and  $K_o$  are defined in ANSI EIA Standard 481–B 2001.
4. Each reel is 178 millimeters in diameter and contains 1000 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481–B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

### Soldering & Storage Information

The CL package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 17: Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	$t_{soak}$	2 to 3 minutes
Time above 217 °C ( $T_1$ )	$t_1$	Max 60 s
Time above 230 °C ( $T_2$ )	$t_2$	Max 50 s
Time above $T_{peak} - 10$ °C ( $T_3$ )	$t_3$	Max 10 s
Peak temperature in reflow	$T_{peak}$	260 °C
Temperature gradient in cooling		Max -5 °C/s

Figure 18: Solder Reflow Profile Graph

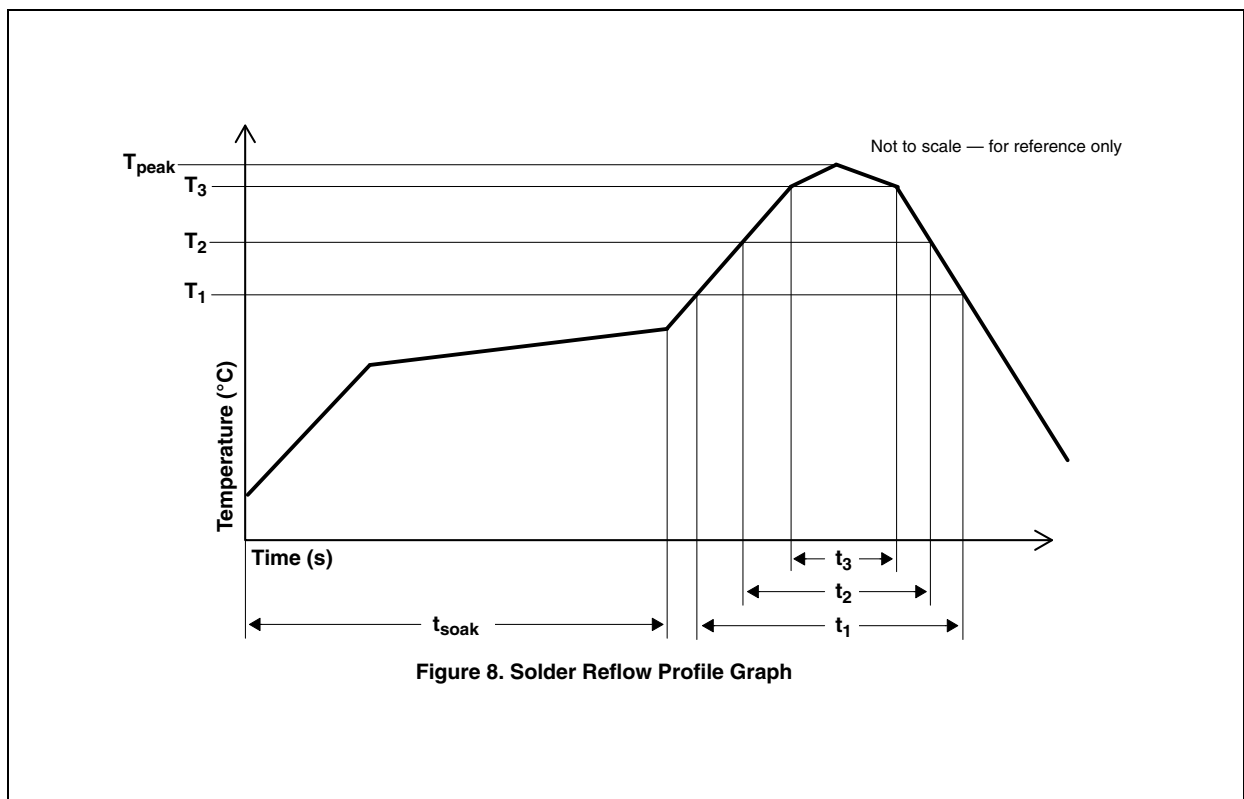


Figure 8. Solder Reflow Profile Graph



## Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The CL package has been assigned a moisture sensitivity level of MSL 5a and the devices should be stored under the following conditions:

- Temperature Range: 5°C to 50°C
- Relative Humidity: 60% maximum
- Total Time: 6 months from the date code on the aluminized envelope - if unopened
- Opened Time: 24 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 6 months or if the aluminized envelope has been open for more than 24 hours. If rebaking is required, it should be done at 60°C for 24 hours.

## Ordering & Contact Information

Figure 19:  
Ordering Information

Ordering Code	Type	Delivery Form	Delivery Quantity
TSL201CL	64 x 1 Array	Tape & Reel	1000 pcs/reel

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## Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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## Revision Information

Changes from TAOS146 (2012-Apr) to current revision 1-00 (2016-May-20)	Page
Content of TAOS datasheet was converted to the latest <b>ams</b> design	
Added Figure 1	1
Added Figure 19	18

**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

## Content Guide

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