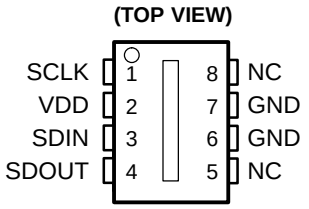
TSL2301
102 × 1 LINEAR OPTICAL SENSOR ARRAY WITH ANALOG-TO-DIGITAL CONVERTER

TAOS007 – JULY 2000

- **102 × 1 Sensor Element Organization**
- **300 Dots-per-Inch Pixel Pitch**
- **On-Chip 8-Bit Analog-to-Digital Converter**
- **Three-Zone Programmable Offset (Dark Level) and Gain**
- **High Speed (10 MHz) Clocked Serial Interface**
- **1-MHz Pixel Rate**
- **Single 5-V Supply**



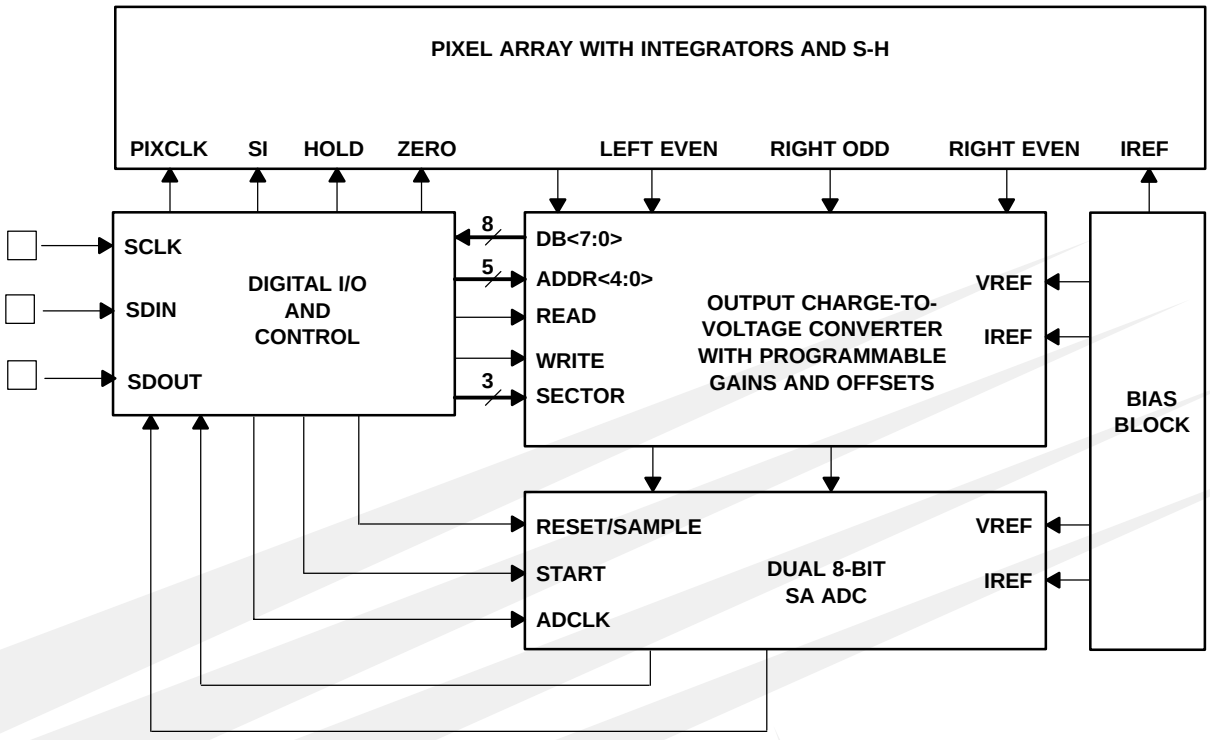
NC – No internal connection

Description

The TSL2301 is a 300-dpi, 102-pixel linear optical sensor array with an integrated 8-bit analog-to-digital converter. The pixels are on 85-µm centers and measure 85 µm (H) by 77 µm (W) with 8 µm between pixels. Associated with each pixel is a charge integrator/amplifier and sample-hold circuit. All pixels have concurrent integration periods and sampling times. Data communication is accomplished through a three-wire serial interface. The array is split into three 34-pixel zones, with each zone having programmable gain and offset levels.

The TSL2301 is intended for use in high-performance, cost-critical imaging and optical sensing applications.

Functional Block Diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	6, 7		Ground
SCLK	1		Clock input for SDIN and SDOUT
SDIN	3		Serial data input. Data is clocked in on the rising edge of CLK.
SDOUT	4		Serial data output. Data is clocked out on the falling edge of CLK.
V_{DD}	2		Supply voltage, V_{DD} is nominally 5 V.

Detailed Description

The sensor consist of 102 photodiodes, also called pixels, arranged in a linear array. Light energy impinging on the pixels generates a photocurrent, which is then integrated by the active integration circuitry associated with each pixel. During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity (E_e) on that pixel and the integration time (t_{int}).

The array is divided into three 34-pixel zones, with each zone having programmable gain and offset (dark signal) correction. The offset correction is controlled by an 8-bit DAC and is performed in the analog domain prior to the digital conversion. There is a separate offset DAC for each of the three zones. The offset value is signed, with codes 0 – 7Fh corresponding to positive offset values and codes 80h – FFh corresponding to increasingly negative offset values. Offset adjustments should be made before setting the gain, but may have to be readjusted after the gain changes are made. The gain adjustment is controlled by a 5-bit DAC, with positive gain values ranging from 0 to 1Fh. There is a separate gain DAC for each of the three zones. Table 1 lists the gain settings and the resulting gain change.

Integration, sampling, output, and reset of the integrators are performed by the control logic in response to commands input via the SDIN pin. A normal sequence of operation consists of a pixel reset (RESET), start of integration (STARTInt), sampling of integrators (SAMPLEInt), and pixel output (READPixel). Reset sets all the integrators to zero. Start of integration releases the integrators from the reset state and defines the beginning of the integration period. Sampling the integrators ends the integration period and stores the charge accumulated in each pixel in a sample and hold circuit. Reading the pixels causes the sampled value of each pixel to be converted to 8-bit digital format and output on the SDOUT pin. All 102 pixels are output sequentially unless interrupted by an abort (ABORTPixel) command or reset by a RESET command.

The commands coming from the controller via the SDIN line are synchronous with the SCLK, which nominally operates at 10 MHz. The protocol for both the data and control words employs the USART convention of start/stop delimiters. There is one start bit and one stop bit.

Table 1. Gain Settings and Results

GAIN CODE	RELATIVE GAIN	% INCREASE	GAIN CODE	RELATIVE GAIN	% INCREASE
0	1.00		16	1.52	3.23
1	1.02	2.17	17	1.57	3.33
2	1.05	2.22	18	1.62	3.45
3	1.07	2.27	19	1.68	3.57
4	1.09	2.33	20	1.74	3.70
5	1.12	2.38	21	1.81	3.85
6	1.15	2.44	22	1.88	4.00
7	1.18	2.50	23	1.96	4.17
8	1.21	2.56	24	2.05	4.35
9	1.24	2.63	25	2.14	4.55
10	1.27	2.70	26	2.24	4.76
11	1.31	2.78	27	2.35	5.00
12	1.34	2.86	28	2.48	5.26
13	1.38	2.94	29	2.61	5.56
14	1.43	3.03	30	2.77	5.88
15	1.47	3.13	31	2.94	6.25

Register address map

The TSL2301 contains seven registers (Table 2). Three registers control the gain of the analog-to-digital converters (ADCs). Three other registers allow the offset of the system to be corrected. Together the gain and offset registers are used to maximize the achievable dynamic range. The last register is a mode register that selects both device cascade options and production test options. Note that device cascade options do not apply to the 8-pin packaged device.

Table 2. Register Address Map

ADDRESS	REGISTER DESCRIPTION	REGISTER WIDTH
0	Pixels 0–33 Offset	8
1	Pixels 0–33 Gain	5
2	Pixels 34–67 Offset	8
3	Pixels 34–67 Gain	5
4	Pixels 68–101 Offset	8
5	Pixels 68–101 Gain	5
1F	Mode	4

The offset registers are 8-bit signed offsets and the gain registers are 5-bit magnitudes. The programmed offset correction is applied to the sampled energy, and then the gain is applied. (e.g., the gain will affect the offset correction). These two registers allow the user to maximize the dynamic range achievable in the given system.

The mode register is used during factory testing and for future product enhancements. The user should always program zeros into the mode register.

Absolute Maximum Ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} . . . . . 7 V
Digital output voltage range, V_O . . . . . –0.5 V to V_{DD} +0.5 V
Digital output current, ... –10 to +10 mA
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –25°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.25	V
High-level input voltage at SCLK, SDIN, V_{IH}	2			V
Low-level input voltage at SCLK, SDIN, V_{IL}			0.8	V
Operating junction temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, SDOUT		V_{DD} = 5.25 V, IO = 50 mA, See Note 1			3	V
			V_{DD} = 4.75 V, I_O = 4 mA	2.4			
V_{OL}	Low-level output voltage, SDOUT		V_{DD} = 4.75 V, V_{DD} = 4.75 V		0.01		V
			V_{DD} = 4.75 V, I_O = 4 mA			0.4	
I_{DD}	Supply current		A/D active		11	17	mA
			A/D inactive		6	11	
V_{IL}	Low-level input voltage (SCLK, SDIN)			0		0.8	V
V_{IH}	High-level input voltage (SCLK, SDIN)			2			V
I_{IH}	High-level input current (SCLK, SDIN)		V_I = V_{DD}			±10	µA
I_{IL}	Low-level input current	SCLK, SDIN	V_I = 0			±10	µA

NOTE 1: Output high level is nominally 0.6 V_{DD} with no load.

Optical Array Characteristics (single-die) at V_{DD} = 5 V, T_A = 25°C, λ_p = 590 nm, t_{int} = 200 μs (unless otherwise noted) Ee=??????

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DSNU	Dark signal non-uniformity	Gain register = 00000b, See Note 2		5	10	LSB
		Gain register = 11111b, See Note 2			14	
PRNU	Photo-response non-uniformity	See Notes 3 and 4		±4%	±5%	
	Dark-level effective illumination (measure of dark current)	T_A = 70°C		TBD		nJ/cm^2

NOTES: 2. DSNU is the difference between the highest value pixel and the lowest value pixel of the device under test when the array is not illuminated.
3. PRNU does not include DSNU.
4. PRNU is the difference between the highest value pixel and the lowest value pixel of the device under test when the array is uniformly illuminated at nominal white level (typical average output level = 200).

Switching Characteristics over recommended operating range (unless otherwise noted)

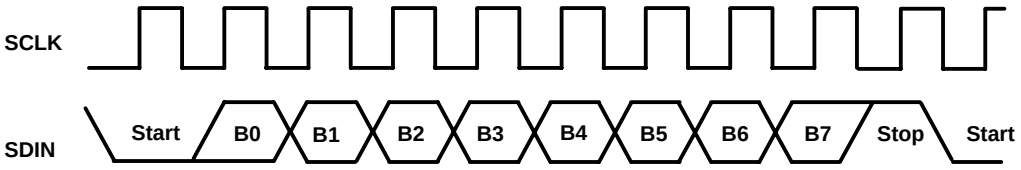
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		10			MHz
$t_{w(CLKH)}$	Clock high pulse duration		30			ns
$t_{w(CLKL)}$	Clock low pulse duration		30			ns
t_{su}	Input setup time		20			ns
t_h	Input hold time		20			ns
t_r	Rise time, output	C_L = 20 pF		10		ns
t_r	Fall time, output			10		ns
t_d	Delay from clock edge to data-out stable			20	TBD	ns
C_i	Input pin capacitance			10		pF

Light-to-Digital Transfer Characteristics at V_{DD} = 5 V, T_A = 25°C, λ_p = 590 nm, t_{int} = 200 μs (unless otherwise noted) E_e=???????

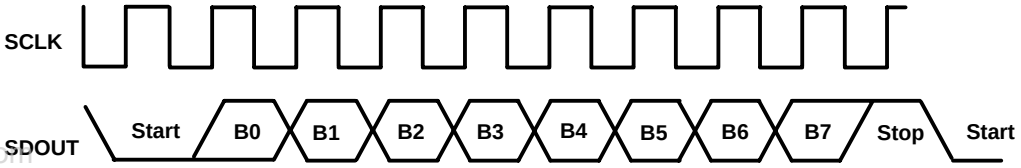
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A-to-D converter resolution				8		Bits
Full-scale reference	Gain register = 00000b		5	6.3	7.6	nJ/cm^2
	Gain register = 11111b			2.1		
Full-scale reference temperature sensitivity		For converter only, does not include photodiode characteristics		±150		ppm/°C
Average dark-level	Gain register = 00000b	Offset register = 00000000b	0	17	30	LSB
	Gain register = 11111b		TBD	TBD	TBD	
Average white level output	Gain register = 00000b	Offset register = 00000000b	170	200	230	LSB
	Gain register = 11111b		TBD	TBD	TBD	
Programmable offset steps				±64		
Programmable offset step size	Gain register = 00000b			0.5		LSB
	Gain register = 11111b			1.5		
Dark-level change with temperature		0°C < T_A < 70°C		2		LSB
Differential nonlinearity				±0.5		LSB
Integral nonlinearity				±1		LSB
Dark level noise	Gain register = 00000b			0.5		LSB
	Gain register = 11111b			1.5		
Power supply rejection ratio				TBD		dB

APPLICATION INFORMATION

Serial I/O



Serial Input Data Format



Serial Output Data Format

Command description

The TSL2301 is a slave device that reacts strictly to commands received from the controller. There are three types of commands, reset commands, pixel action commands and register commands. These commands cause the device to perform functions such as: reset, integrate, sample, etc. Each command is described in more detail in Table 3. All commands are single-byte except for the register write command, which is two bytes. There is a requirement for delay of 8 clocks after each command to allow for processing of the command.

Table 3. TSL2301 Command Set

COMMAND	DESCRIPTION
IRESET	Interface Reset
RESET	Reset Integration and Read blocks
STARTInt	Start pixel integration
SAMPLEInt	Stop integration and sample results
READPixel	Dump serial the contents of each sampled integrator
ABORTPixel	Abort any READPixel operation in progress
READHold	Combination of SAMPLEInt and READPixel commands
READHoldNStart	Combination of SAMPLEInt, READPixel and STARTInt commands
REGWrite	Write a gain, offset or mode register
REGRead	Read a gain, offset or mode register

Reset Commands

Reset commands are used to put the TSL2301 into a known state.

IRESET – Interface Initialization

Encoding: Break Character

IRESET initializes the internal state machine that keeps track of which command bytes have been received. This command should be first and given only once after power-up to synchronize TSL2301's command interpreter.

RESET – Main Reset

Encoding: 0x1b: <0001_1011>

RESET resets most of the internal control logic of the TSL2301 and any *READPixel* command currently in progress is aborted. *RESET* puts the pixel integrators into the auto-zero/reset state. Any values that were being held in the array's sample/hold circuits are lost.

NOTE:

On power up of the TSL2301, it is necessary to hold SDIN high for 30 clocks before initiating a reset command. In addition, to fully reset the device, it is recommended that 3 consecutive RESET commands be issued as part of the power up routine.

NOTE:

The value on the SDOUT pin is not guaranteed from the time power is applied until 30 clocks after the first RESET command is issued.

Pixel Action Commands

Pixel action commands allow the user to control pixel integration and reading of pixel data.

STARTInt – Start Integration

Encoding: 0x08: <0000_1000>

STARTInt causes each pixel to leave the reset state and to start integrating. The actual execution of *STARTInt* is delayed 20 clocks until the auto-zero cycle of the pixels has been completed.

SAMPLEInt – Stop Integration

Encoding: 0x10: <0001_0000>

SAMPLEInt causes each pixel to store its integrator's contents into a sample and hold circuit. Also, the Integrator is returned to the reset state.

READPixel – Read Pixel Data

Encoding: 0x02: <0000_0010>

READPixel causes the sampled value of each pixel to be converted to an 8-bit digital value that is clocked out on the *SDOUT* pin. The LSB is the first data bit, which is preceded by a START bit (logic 0) and followed by a STOP bit (logic 1). Each pixel in the device is presented on *SDOUT* starting from pixel 00 and completes with pixel 101. It takes 20 clocks before the first pixel is available to be read and 10 clocks per pixel thereafter until all pixels are output.

Gain and offset registers are used to adjust the ADC converter to maximize dynamic range and should be programmed prior to invoking the *READPixel* command.

ABORTPixel – Abort Pixel Data Read

Encoding: 0x19: <0001_1001>

ABORTPixel is an optional command that stops a *READPixel* command during its execution. It also causes pixel integration to terminate and to enter the auto-zero/reset state. Any values that were being held in the array's sample/hold circuits are lost.

READHold – Sample and Read Combination

Encoding: 0x12: <0001_0010>

READHold is a macro command that combines both the *SAMPLEInt* and *READPixel* commands into a single command. It is also provided as a shortcut for advanced users.

READHoldNStart Combination

Encoding: 0x16: <0001_0110>

READHold is a macro command that combines the *SAMPLEInt*, *READPixel,* and *StartInt* commands into a single command, and is provided as a shortcut for advanced users.

Register Commands

The register commands provide the user the capability of setting gain and offset corrections for each of the three zones of pixels. a4–a0 refer to the register address as given in Table 2.

REGWrite – Write a Gain/Offset/Mode Register

Encoding: 0x40 <data>: <010a4_a3a2a1a0> <d7d6d5d4_d3d2d1d0>

REGWrite writes a value into either a gain, offset, or mode register. The 5-bit address of the register is encoded into the command byte (the first byte). A second byte, which contains the data to be written, follows the command byte.

REGRead – Read a Gain/Offset/Mode Register

Encoding: 0x60: <011a4_a3a2a1a0>

REGRead reads the value previously stored in a gain, offset, or mode register. The 5-bit address of the register is encoded into the command byte. Then, following receipt of the *REGRead* command, the device places the contents of the selected register onto the SDOUT pin, LSB first. Data will be available to read 4 clocks after the execution of the command.

Table 4. Summary of Command Types and Formats

COMMAND TYPE	FORMAT
Reset	< Command byte >
Pixel action	< Command byte >
Register read	< Command byte >
Register write	< Command byte > < Data byte>

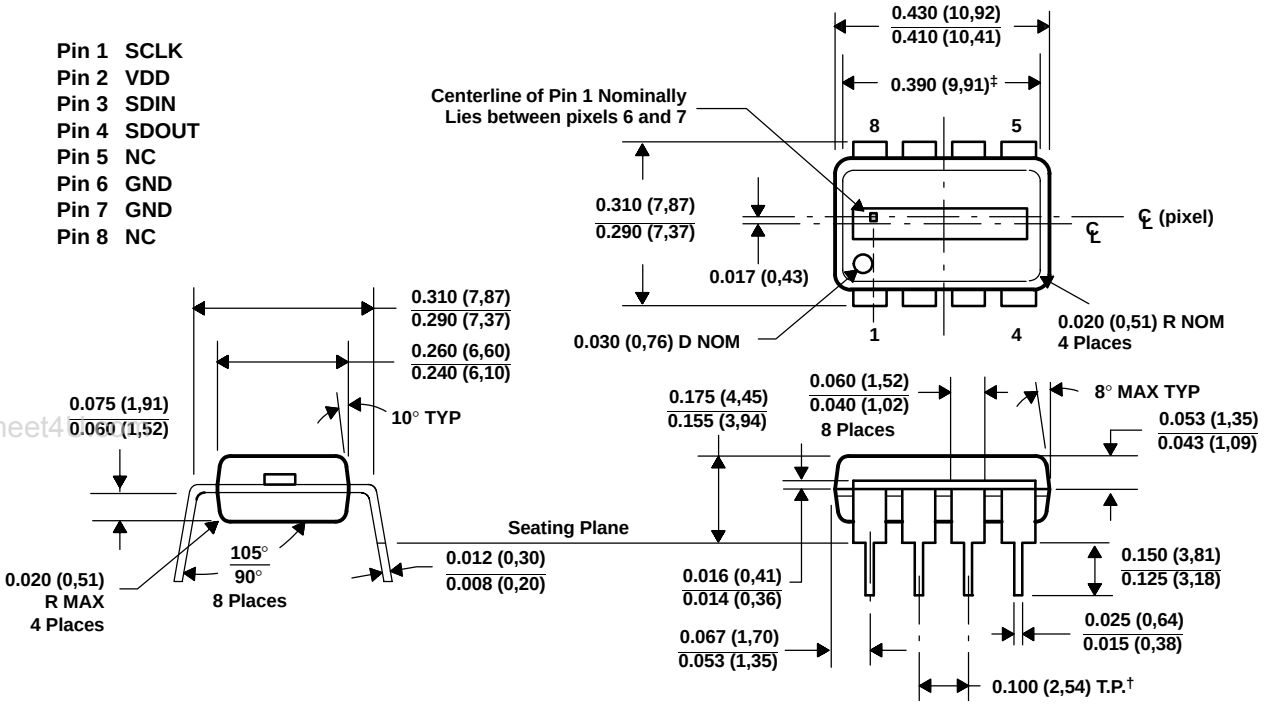
Normal programming sequence

This section describes a typical programming sequence that can be used with the TSL2301 device:

```
30 clocks with SDIN high
Send(RESET);
Send(RESET);
Send(RESET);
Calibration Cycle
  *
  *
while(1)
   for(i=0;i<=2;i++) {/* for each pixel page */
      Write page gain register
      Write page offset register
      Read page gain register and verify (optional)
      Read page offset register and verify (optional)
   }
}
Send(STARTInt) ;
DelayIntegrationTime( );  /* wait for appropriate time interval to elapse */
Send(SAMPLEInt);
Send(READPixel);
```

MECHANICAL INFORMATION

This dual-in-line package consists of an integrated circuit mounted on a lead frame and encapsulated with an electrically nonconductive clear plastic compound.



† True position when unit is installed
‡ Minimum flat-optical-surface length

NOTES: A. All linear dimensions are in inches and parenthetically in millimeters.
B. This drawing is subject to change without notice.
C. Index of refraction of clear plastic is 1.55.

Figure 1. Packaging Configuration

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