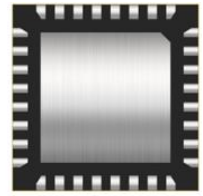
TSL8029N: Single channel 2 – 5GHz 100Watt Receiver Front End for MACRO base station

1.0 Features



Integrated single-channel RF front end

2-stage LNA and GaN SPDT switch On-chip bias and matching Single-supply operation

- Gain @ 3.6GHz: 33dB [High Gain mode]
  @ 3.6GHz: 14.5dB [Low Gain mode]
- NF @ 3.6GHz: 1.4dB [High Gain mode]
  @ 3.6GHz: 1.3dB [Low Gain mode]
- OP1dB@ 3.6GHz: 22dBm [High Gain mode]
  @ 3.6GHz: 12dBm [Low Gain mode]
- Operating frequency: 2 to 5GHz
- Insertion loss @ 3600MHz: 0.5dB [TX mode]
- Switch isolation @ 3.6GHz: 18dB [RX HG mode]
- RX isolation @ 3.6GHz: 53dB [PD=BP=0V]
  @ 3.6GHz: 42dB [PD=BP=5V]
  @ 3.6GHz: 38dB [PD=0V & BP=5V]
  @ 3.6GHz: 45dB [PD=5V & BP=0V]
- High power handling at TCASE = 105°C Full lifetime
- LTE average power [8 dB PAR]: 50dBm
- High OIP3 [high gain mode]: 31dBm typical
- High gain mode current: 90mA typical at 5V
- Low gain mode current: 45mA typical at 5V
- Power-down mode current: 4mA typical at 5V Positive logic control
- 5 mm × 5 mm, 32-lead LFCSP

RoHS/REACH/Halogen Free Compliance

2.0 Applications

- 4G/5G Infrastructure Radios, Macro base station
- Small Cells and Cellular Repeaters
- Phase Array Radar
- SDARS

3.0 Description

The TSL8029N is a single-channel, integrated RF, front-end, multichip module designed for different applications. The device operates from 2GHz to 5GHz.The TSL8029N is configured with a cascading, two-stage, GaAs LNA and a GaN based SPDT switch. In high gain mode, the cascaded two-stage LNA and switch offer a low noise figure of 1.3 dB and a high gain of 33 dB at 3.6 GHz with an output third-order intercept point (OIP3) of 33 dBm (typical) at high gain mode. In low gain mode, one stage of the two-stage LNA is in bypass, providing 14.5 dB of gain at a lower current of 50 mA. In power-down mode, the LNAs are turned off and the device draws 4 mA.
In transmit operation, when RF inputs are connected to a termination pin (TX), the switch provides low insertion loss of 0.5 dB at 3.6GHz and handles long-term evolution (LTE) average power (8 dB peak to average ratio (PAR)) of 50 dBm for full lifetime operation.
The device comes in an RoHS compliant, compact,
5 mm × 5 mm, 32-lead LFCSP.

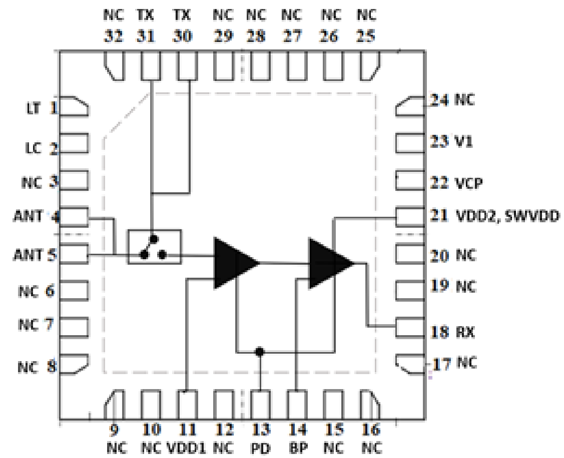


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TSL8029N	32 Pin 5×5×0.85mm QFN	Tape & Reel	3000	13” (330mm)	18mm	TSL8029NMTRPBF
Tuned Evaluation Board, 2300-2700 MHz						TSL8029N-EVB-A
Tuned Evaluation Board, 3300-4200 MHz [HG only]						TSL8029N-EVB-B
Tuned Evaluation Board, 3300-4200 MHz						TSL8029N-EVB-C
Tuned Evaluation Board, 3300-3800 MHz [HG only]						TSL8029N-EVB-D
Tuned Evaluation Board, 2900-3300 MHz						TSL8029N-EVB-E

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
1,2	LT, LC	Tuning inductor
3,6,7,8, 9,10,12,15,16,17,19,20, 24,25,26,27,28,29, and 32	NC	Not Internally Connected. It is recommended to connect NIC to the RF ground of the PCB.
4,5	ANT	RF Input. The ANT pin is ac-coupled to 0 V and matched to 50 Ω. Matching and a dc blocking capacitor are not required.
11	VDD1	Vdd1 supplied through an external choke inductor
13	PD	Bypass Second Stage LNA.
14	BP	Power-Down All Stages of LNA
18	RX	Receiver Output. The RX pin is the receiver path for the channel. The RX pin is ac matched to 50 Ω. No matching component is required. A dc blocking capacitor is required.
21	VDD2_ SWVDD	VDD2_SWVDD supplied voltage through an external choke inductor to LNAs and it connected with Supply Voltage for Switch also.
22	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time
23	V1	Control Voltage for Switch.
30,31	TX	Termination Output. The TX pin is the transmitter path. The TX pin is ac-coupled to 0 V and matched to 50 Ω. No matching and dc blocking capacitor is required.
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

Note: [**1**] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsink required.

6.0 Absolute Maximum Rating

Table 6.1 Absolute Maximum Rating @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, VDD1, VDD2, SWVDD	V_{dd}	+5.5	V
RF input power Transmit Input Power (LTE Peak,8dB PAR,) Receive Input Power (LTE Peak, 8 dB PAR)	RF_{IN}	58 25	dBm dBm
Digital Control Input Voltage V1, BP and PD		2.6 to 5.5	V
Digital Control Input Current V1, BP and PD		0.2	mA
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +105	°C
Maximum Junction Temperature	T_J	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	15.0	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Recommended DC Operating Conditions

Table 7.1 Recommended Operating Conditions @TA=+25°C Unless Otherwise Specified

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltages	VDD1		+5.0		V
	VDD2		+5.0		
Drain Bias Currents	I_{DQ1}, Set by external drain feed		50		mA
	I_{DQ2}, Set by external drain feed		90		
Switch Supply	SWVDD		+5		V
Switch Control Voltages	V1, BP and PD	-0.3		+5.5	V
RF Input Power in Tx mode At ANT	V1 = 5V, PD = 5 V, BP = 0 V. 8 dB PAR LTE full lifetime average		50		dBm
	V1 = 5V, PD = 0 V, BP = 0 V. 8 dB PAR LTE full lifetime average			TBD	dBm
	V1 = 5V, PD = 0 V, BP = 5 V. 8 dB PAR LTE full lifetime			TDB	dBm
Digital Inputs	V1, PD Low (VIL) High (VIH)	-0.3 2.6		0.5 Vdd	V
	BP Low (VIL) High (VIH)	0 2.6		0.5 Vdd	
Digital Input Currents	V1[=5V]			<7.5	µA
	PD[=5V]			200	
	BP[=5V]			100	
Switch control max current				7.5	µA
Operating Temperature Range	T_{op}	-40	+25	+105	°C

Table 7.2 Truth Table: Switch control

V1(Switch control)	Signal Path Select	
	Transmit Operation	Receive Operation
Low High	Off On	On Off

Table 7.3 Truth Table: Receive Operation

Receive Operation	PD	BP	Signal Path
High Gain Mode	Low	Low	ANT to RX
Low Gain Mode	Low	High	
Power-Down Mode [LNA is on HG]	High	Low	
Power-Down Mode [LNA is on LG]	High	High	

8.0 RF Electrical Specifications for EVBs

VDD1, VDD2_SWVDD = 5 V, BP=0V/5V and PD=0V TCASE = 25°C, and 50 Ω system, unless otherwise noted.

Table 8.1 2300 – 2700MHz EVB A

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency		2.3 G		2.7 G	Hz
Gain	LNAs on Bypass off (High gain)		34		dB
Gain	LNA1 on Bypass on (Low gain)		14-14.5		dB
Noise Figure (De-embedded)	LNAs on Bypass off (High gain)		1		dB
Noise Figure (De-embedded)	LNA1 on Bypass on (Low gain)		1		dB
Noise Figure [SMA-SMA]	LNAs on Bypass off (High gain)		1.2		dB
Noise Figure [SMA-SMA]	LNA1 on Bypass on (Low gain)		1.2		dB
Input Return Loss	LNAs on Bypass off (High gain)		< -9.3		dB
Input Return Loss	LNA1 on Bypass on (Low gain)		< -8.5		dB
Output Return Loss	LNAs on Bypass off (High gain)		< -8.4		dB
Output Return Loss	LNA1 on Bypass on (Low gain)		< -4		dBm
OP1dB	LNAs on Bypass off (High gain)		20-21		dBm
OP1dB	LNA1 on Bypass on (Low gain)		14-16		dBm
OIP3	LNAs on Bypass off (High gain) 0dBm/tone, Tone Spacing 1MHz		29.5-31.5		dBm
OIP3	LNA1 on Bypass on (Low gain) -2dBm per tone, Tone Spacing 1MHz		23-30		dBm
Current, Id	LNAs on Bypass off (High gain)		93		mA
Current, Id	LNA1 on Bypass on (Low gain)		55		mA
Current, Id	PD mode ON (Both LNAs OFF)		4		mA
Insertion Loss [SMA-SMA]	Transmit operation		0.7-0.9		dB
Insertion Loss [De-embedded]	Transmit operation		0.5-0.7		dB
Switch Isolation in RX mode	PD=BP=V1=0 V		>25		dB

Table 8.2 3300 – 4200MHz EVB B [HG only]

Parameter		Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency			3.3 G		4.2 G	Hz
Gain		LNAs on Bypass off (High gain)		29.5-32.4		dB
Noise Figure	(De-embedded)	LNAs on Bypass off (High gain)		1.3-1.4		dB
	[SMA-SMA]	LNAs on Bypass off (High gain)		1.5-1.6		dB
Input Return Loss		LNAs on Bypass off (High gain)		< -10.5		dB
Output Return Loss		LNAs on Bypass off (High gain)		< -7.5		dB
OP1dB		LNAs on Bypass off (High gain)		19-21		dBm
OIP3		LNAs on Bypass off (High gain) 0dBm/tone, Tone Spacing 1MHz		31-37		dBm
Current, Id		LNAs on Bypass off (High gain)		93		mA
		PD mode ON (Both LNAs OFF)		4-5		
Insertion Loss	[SMA-SMA]	Transmit operation at 3.6 GHz		0.7		dB
	[De-embedded]	Transmit operation at 3.6 GHz		0.5		dB
Switch Isolation in RX		PD=BP=V1=0 V		>19.7		dB

Table 8.3 3300 – 4200MHz EVB C

Parameter		Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency			3.3 G		4.2 G	Hz
Gain		LNAs on Bypass off (High gain)		29.5-32.4		dB
		LNA1 on Bypass on (Low gain)		12.5-14		dB
Noise Figure	(De-embedded)	LNAs on Bypass off (High gain)		1.4		dB
		LNA1 on Bypass on (Low gain)		1.3		dB
	[SMA-SMA]	LNAs on Bypass off (High gain)		1.6		dB
		LNA1 on Bypass on (Low gain)		1.5		dB
Input Return Loss		LNAs on Bypass off (High gain)		< -10.5		dB
		LNA1 on Bypass on (Low gain)		< -13		dB
Output Return Loss		LNAs on Bypass off (High gain)		< -7		dB
		LNA1 on Bypass on (Low gain)		< -7		dBm
OP1dB		LNAs on Bypass off (High gain)		19-21		dBm
		LNA1 on Bypass on (Low gain)		11-12.5		dBm
OIP3		LNAs on Bypass off (High gain) 0dBm/tone, Tone Spacing 1MHz		31-37		dBm
		LNA1 on Bypass on (Low gain) -2dBm/tone, Tone Spacing 1MHz		20-22		dBm
Current, Id		LNAs on Bypass off (High gain)		93		mA
		LNA1 on Bypass on (Low gain)		55		
		PD mode ON (Both LNAs OFF)		4		
Insertion Loss	[SMA-SMA]	Transmit operation		0.7-0.75		dB
	[De-embedded]	Transmit operation		0.4-0.5		dB
Switch Isolation in RX mode		PD=BP=V1=0 V		>18.5		dB

Table 8.4 3300 – 3800MHz EVB D [HG only]

Parameter		Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency			3.3 G		3.8 G	Hz
Gain		LNAs on Bypass off (High gain)		30.5-31		dB
Noise Figure	(De-embedded)	LNAs on Bypass off (High gain)		1.2-1.3		dB
	[SMA-SMA]	LNAs on Bypass off (High gain)		1.4-1.5		dB
Input Return Loss		LNAs on Bypass off (High gain)		< -17		dB
Output Return Loss		LNAs on Bypass off (High gain)		< -16		dB
OP1dB		LNAs on Bypass off (High gain)		20-22		dBm
OIP3		LNAs on Bypass off (High gain) -2dBm/tone, Tone Spacing 1MHz		29-34		dBm
Current, Id		LNAs on Bypass off (High gain)		108		mA
		PD mode ON (Both LNAs OFF)		4-5		
Insertion Loss	[SMA-SMA]	Transmit operation at 3.6 GHz		0.7		dB
	[De-embedded]	Transmit operation at 3.6 GHz		0.4		dB
Switch Isolation in RX		PD=BP=V1=0 V		>25.7		dB

Table 8.5 2900 – 3300MHz EVB E

Parameter		Test Condition	Minimum	Typical	Maximum	Unit
Operational frequency			2.9 G		3.3 G	Hz
Gain		LNAs on Bypass off (High gain)		31-33		dB
		LNA1 on Bypass on (Low gain)		13.5-13.8		dB
Noise Figure	(De-embedded)	LNAs on Bypass off (High gain)		1.2-1.3		dB
		LNA1 on Bypass on (Low gain)		1.2-1.3		dB
	[SMA-SMA]	LNAs on Bypass off (High gain)		1.4-1.5		dB
		LNA1 on Bypass on (Low gain)		1.4-1.5		dB
Input Return Loss		LNAs on Bypass off (High gain)		< -10.5		dB
		LNA1 on Bypass on (Low gain)		< -11.2		dB
Output Return Loss		LNAs on Bypass off (High gain)		< -10.2		dB
		LNA1 on Bypass on (Low gain)		< -6		dBm
OP1dB		LNAs on Bypass off (High gain)		20-21		dBm
		LNA1 on Bypass on (Low gain)		12-13.5		dBm
OIP3		LNAs on Bypass off (High gain) 0dBm/tone, Tone Spacing 1MHz		30.5-32		dBm
		LNA1 on Bypass on (Low gain) -1dBm/tone, Tone Spacing 1MHz		22-30		dBm
Current, Id		LNAs on Bypass off (High gain)		90		mA
		LNA1 on Bypass on (Low gain)		50		
		PD mode ON (Both LNAs OFF)		4		
Insertion Loss	[SMA-SMA]	Transmit operation at 3.6 GHz		0.7-0.8		dB
	[De-embedded]	Transmit operation at 3.6 GHz		0.4-0.5		dB
Switch Isolation in RX mode		PD=BP=V1=0 V		>19		dB

Table 8.6 TX Switching Speed

Parameter	Test Condition	Switching time[ns]	Mode
SWITCHING CHARACTERISTICS (tON, tOFF)	50% control voltage[V1] to 90%, 10% of RX_out in receive operation (Tx to Rx)	1200ns	TX/RX mode
	50% control voltage[V1] to 90%, 10% of TX_out in transmit operation (Rx to Tx)	1200ns	

Table 8.7 RX Switching Speed

Pin toggle	State		Switching time[ns]	Mode	DC Condition
BP	LG to HG		200ns	RX mode	VDD2_SWVDD=5V, V1=5V, VDD1=5V, PD=0V
	HG to LG		450ns		
PD	Low Gain	On to Off	360ns	RX-LG mode	VDD2_SWVDD=5V, V1=5V, VDD1=5V, PD=0V & BP=0V
		Off to on	450ns		
	High Gain	On to Off	360ns	RX-HG mode	VDD2_SWVDD=5V, V1=5V, VDD1=5V, PD=0V & BP=5V
		Off to on	720ns		

9.0 Typical performance characteristics of TSL8029N EVB C

9.1 Receive Operation, Low Gain Mode 3.3-4.2GHz tuned EVB C, **25degreeC** **-40degreeC** **85degreeC** **105degreeC.**

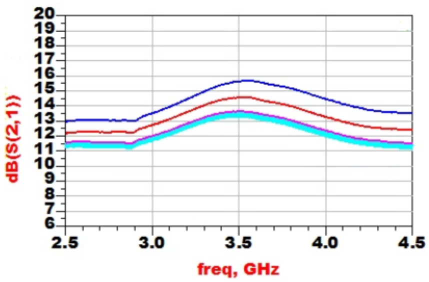


Figure 9.1.1 S21 vs Freq

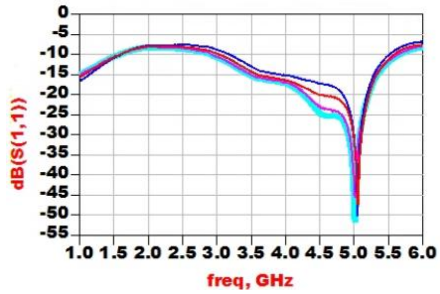


Figure 9.1.2 S11 vs Freq

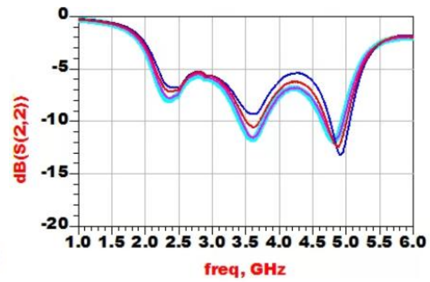


Figure 9.1.3 S22 vs Freq

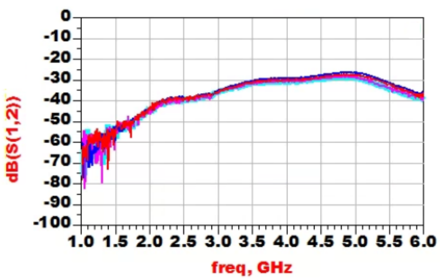


Figure 9.1.4 S12 vs Freq

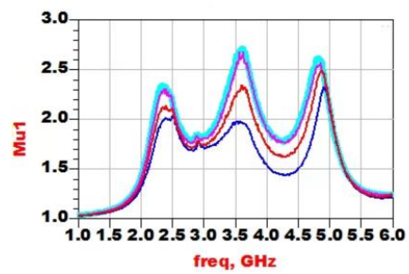


Figure 9.1.5 Stability vs Freq

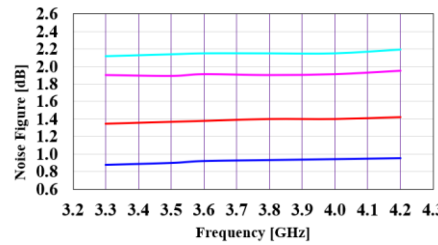


Figure 9.1.6 NF vs Freq SMA to SMA

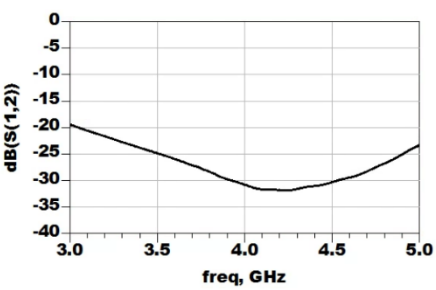


Figure 9.1.7 ANT-TX ISO vs Freq When BP=5V and PD=0V

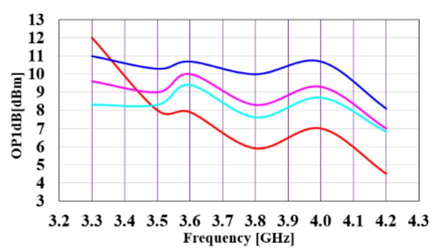


Figure 9.1.8 OP1 vs Freq

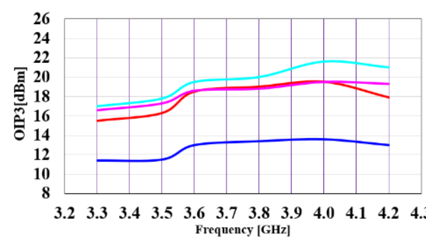


Figure 9.1.9 OIP3 vs Freq

9.2 Receive Operation, High Gain Mode 3.3-4.2GHz tuned EVB C, **25degreeC** **-40degreeC** **85degreeC** **105degreeC.**

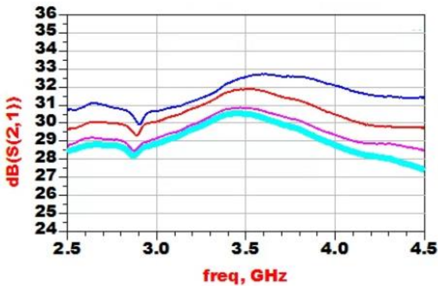


Figure 9.2.1 S21 vs Freq

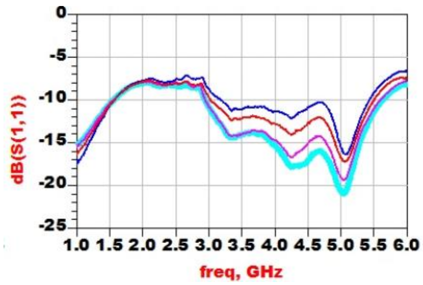


Figure 9.2.2 S11 vs Freq

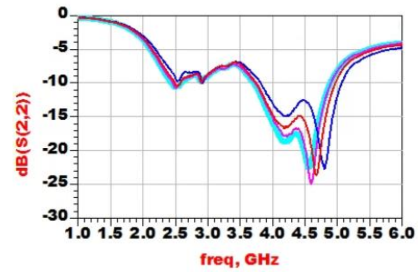


Figure 9.2.3 S22 vs Freq

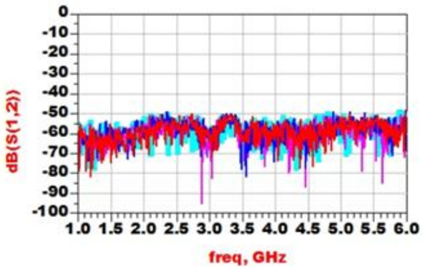


Figure 9.2.4 S12 vs Freq

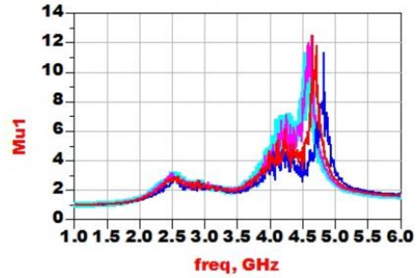


Figure 9.2.5 Stability vs Freq [10MHz to 8.5GHz]

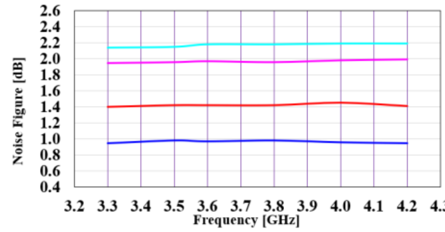


Figure 9.2.6 NF vs Freq SMA to SMA

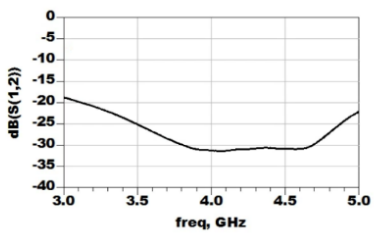


Figure 9.2.7 ANT-TX ISO vs Freq When BP=0V and PD=5V

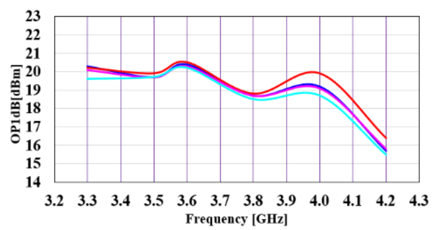


Figure 9.1.8 OP1 vs Freq

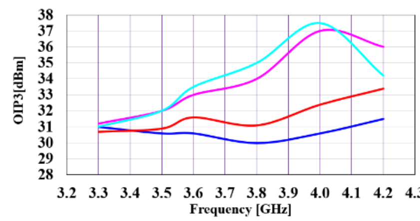


Figure 9.1.9 OIP3 vs Freq

9.3 Transmit Mode 3.3-4.2GHz tuned EVB C, **25degreeC** **-40degreeC** **85degreeC** **105degreeC.**

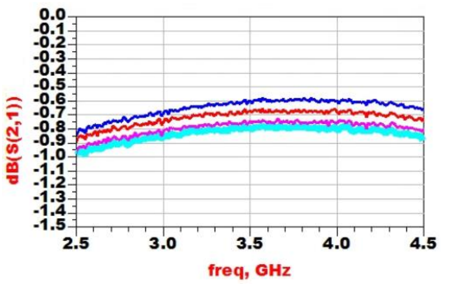


Figure 9.3.1 S21 vs Freq

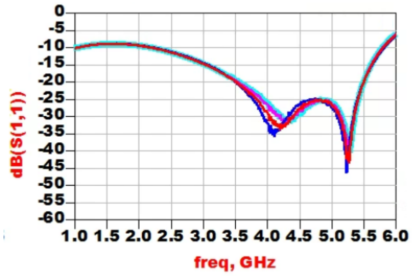


Figure 9.3.2 S11 vs Freq

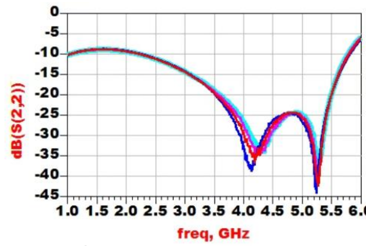


Figure 9.3.3 S22 vs Freq

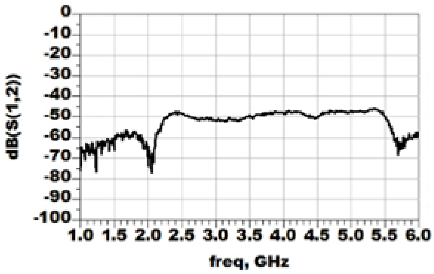


Figure 9.3.4 ANT-RX Isolation when PD=5V and BP=0V vs Freq

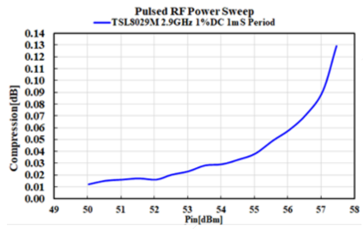


Figure 9.3.5 Compression Vs Peak Power [2.9GHz 1% DC 1mS Period]

10.0 Evaluation Boards

10.1.1 2300-2700MHz EVB A Schematic

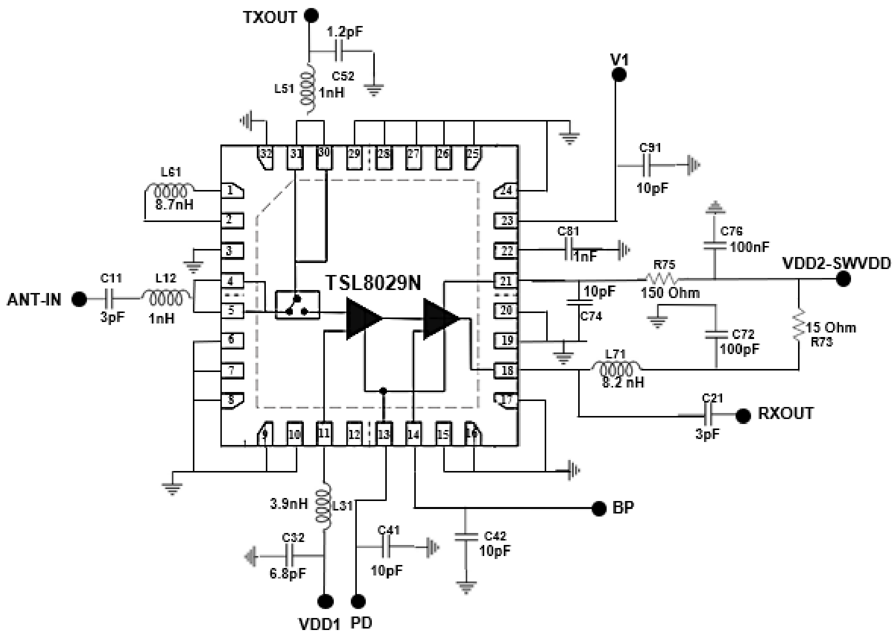


Figure 10.1.1 Schematic of the 2300-2700MHz EVB A

Table 10.1.1 BOM of the 2300-2700MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number	Qty
C11, C21	3 pF	Murata	600S3R0BT250XT	2
L12, L51	1 nH	Coil craft	0402DC-1N0XJRW	2
L31	3.9 nH	Coil craft	0402DC-3N9XGRW	1
C32	6.8 pF	Murata	GJM1555C1H6R8BB01D	1
C41, C42, C74, C91	10pF	Murata	GJM1555C1H100JB01D	4
C52	1.2pF	Murata	600S1R2BT250XT	1
L61	8.7nH	Coil craft	0402HP-8N7XGRW	1
L71	8.2nH	Coil craft	0402HP-8N2XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
R73	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R75	150 Ω	Panasonic	ERJ-2RHD1500X	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.1.2 2300-2700MHz EVB A Layout

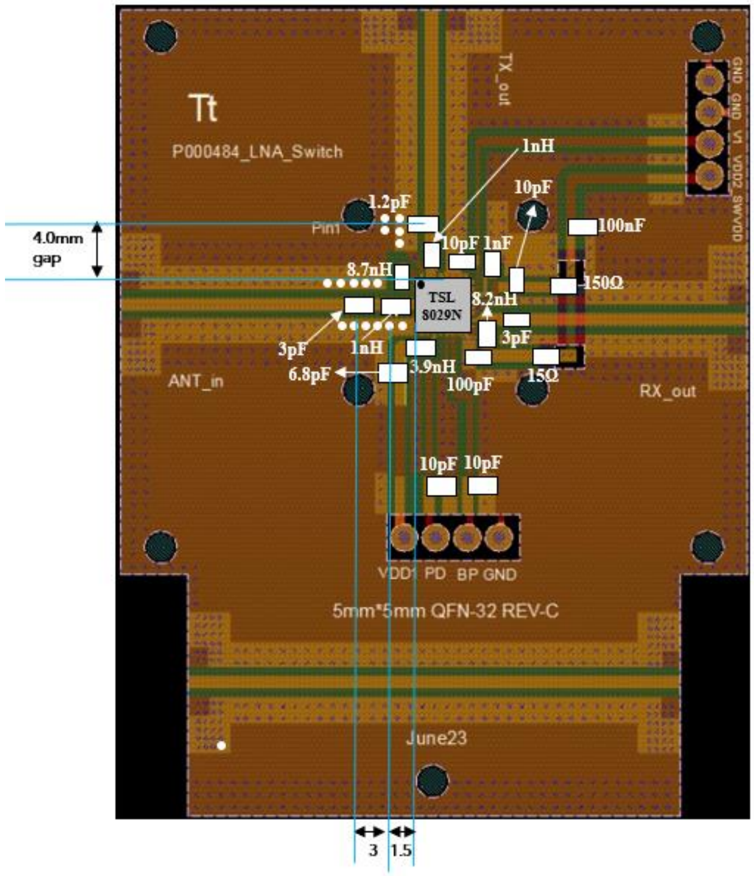


Figure 10.1.2 EVB Layout of the 2300-2700MHz EVB A

Note: Series cap on ANT and TX ports should have 250V voltage ratings to handle 100W power. The heatsink needs to be added at bottom of this board for proper power spreading.

10.1.3 3300-4200MHz EVB B [HG only] Schematic

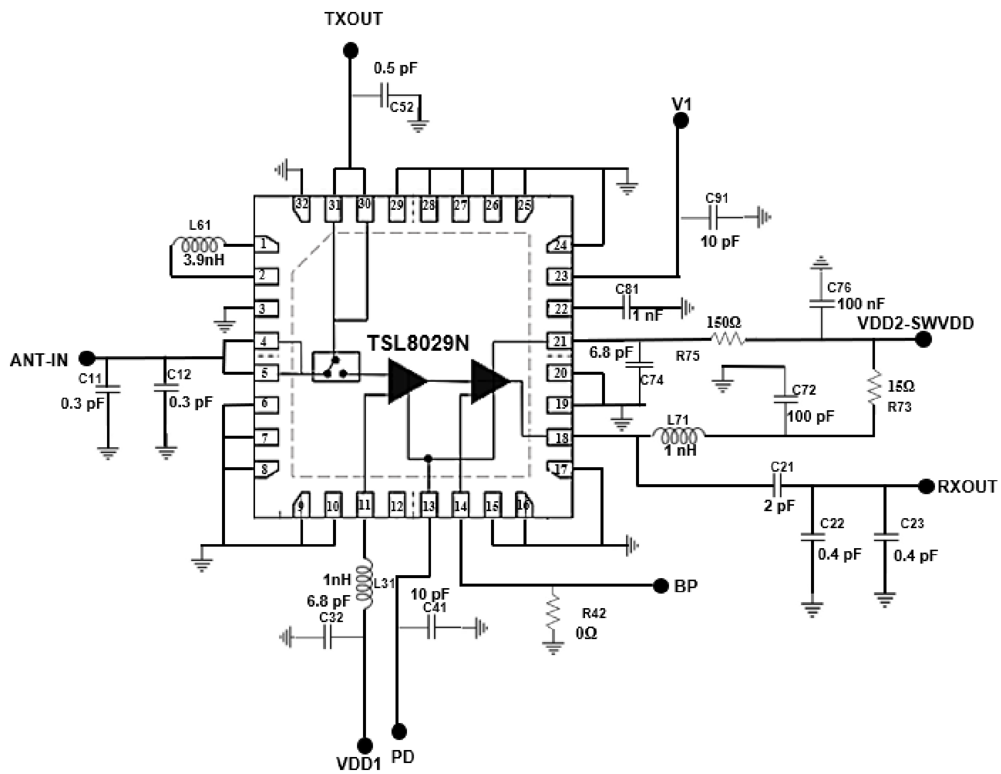


Figure 10.1.3 Schematic of the 3300-4200MHz EVB B [HG only]

Table 10.1.3 BOM of the 3300-4200MHz EVB B [HG only]

Component ID	Value	Manufacturer	Recommended Part Number	Qty
C11, C12	0.3 pF	Murata	600S0R3BT250XT	2
C21	2 pF	Murata	GJM1555C1H2R0BB01D	1
C22, C23	0.4 pF	Murata	GJM1555C1HR40BB01J	2
L31, L71	1 nH	Coil craft	0402DC-1N0XJRW	2
C32, C74	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C41, C91	10pF	Murata	GJM1555C1H100JB01D	2
R42	0 Ω	Panasonic	ERJ-2GE0R00X	1
C52	0.5pF	Murata	600S0R5BT250XT	1
L61	3.9 nH	Coil craft	0402DC-3N9XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
R73	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R75	150 Ω	Panasonic	ERJ-2RHD1500X	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.1.4 3300-4200MHz EVB B [HG only] Layout

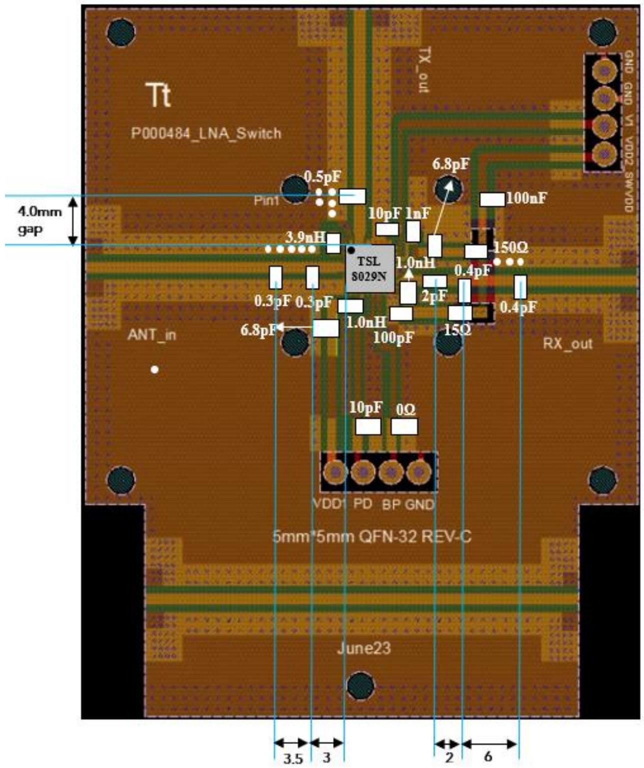


Figure 10.1.4 EVB Layout of the 3300-4200MHz EVB B [HG only]

Note: Series cap on ANT and TX ports should have 250V voltage ratings to handle 100W power. The heatsink needs to be added at bottom of this board for proper power spreading.

10.1.5 3300-4200MHz EVB C Schematic

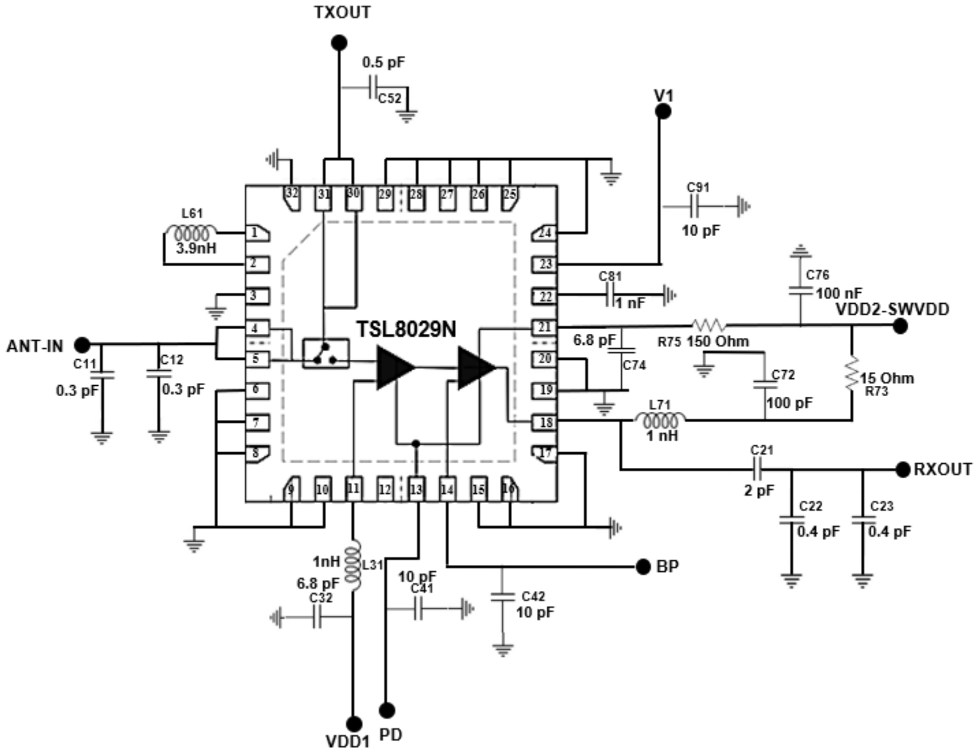


Figure 10.1.5 Schematic of the 3300-4200MHz EVB C

Table 10.1.5 BOM of the 3300-4200MHz EVB C

Component ID	Value	Manufacturer	Recommended Part Number	Qty
C11, C12	0.3 pF	Murata	600S0R3BT250XT	2
C21	2 pF	Murata	GJM1555C1H2R0BB01D	1
C22, C23	0.4 pF	Murata	GJM1555C1HR40BB01J	2
L31, L71	1 nH	Coil craft	0402DC-1N0XJRW	2
C32, C74	6.8 pF	Murata	GJM1555C1H6R8BB01D	2
C41, C42, C91	10pF	Murata	GJM1555C1H100JB01D	3
C52	0.5pF	Murata	600S0R5BT250XT	1
L61	3.9 nH	Coil craft	0402DC-3N9XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
R73	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R75	150 Ω	Panasonic	ERJ-2RHD1500X	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.1.6 3300-4200MHz EVB C Layout

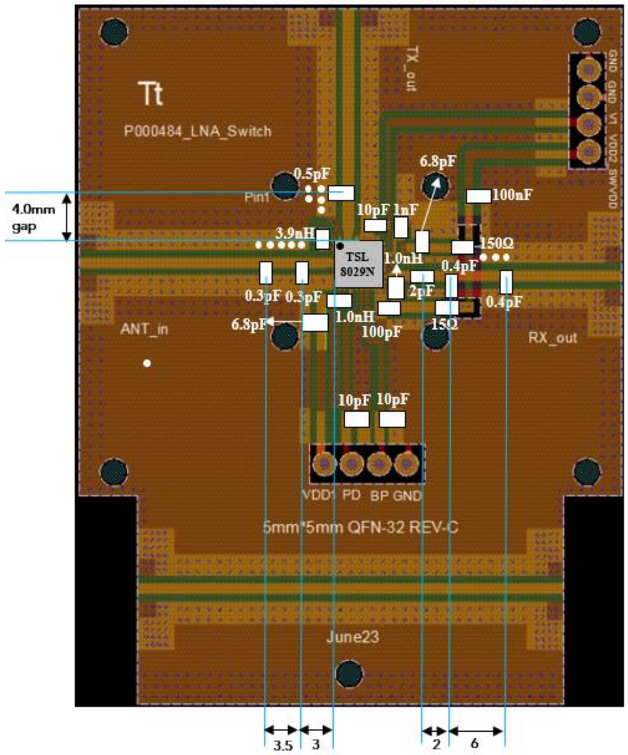


Figure 10.1.6 EVB Layout of the 3300-4200MHz EVB C

Note: Series cap on ANT and TX ports should have 250V voltage ratings to handle 100W power. The heatsink needs to be added at bottom of this board for proper power spreading.

10.1.7 3300-3800MHz EVB D [HG only] Schematic

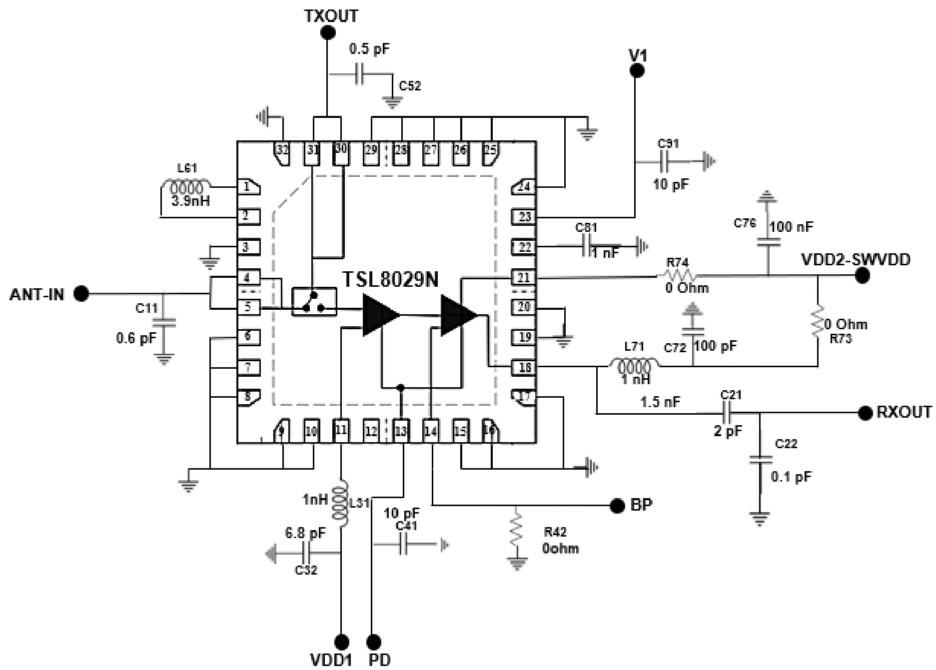


Figure 10.1.7 Schematic of the 3300-3800MHz EVB D [HG only]

Table 10.1.7 BOM of the 3300-3800MHz EVB D [HG only]

Component ID	Value	Manufacturer	Recommended Part Number	Qty
C11	0.6 pF	Murata	600S0R6BT250XT	1
C21	2 pF	Murata	GJM1555C1H2R0BB01D	1
C22	0.1 pF	Murata	GJM1555C1HR10BB01J	1
L31, L71	1 nH	Coil craft	0402DC-1N0XJRW	2
C32	6.8 pF	Murata	GJM1555C1H6R8BB01D	1
C41, C91	10pF	Murata	GJM1555C1H100JB01D	2
R42, R73, R74	0 Ω	Panasonic	ERJ-2GE0R00X	3
C52	0.5pF	Murata	600S0R5BT250XT	1
L61	3.9 nH	Coil craft	0402DC-3N9XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.1.8 3300-3800MHz EVB D [HG only] Layout

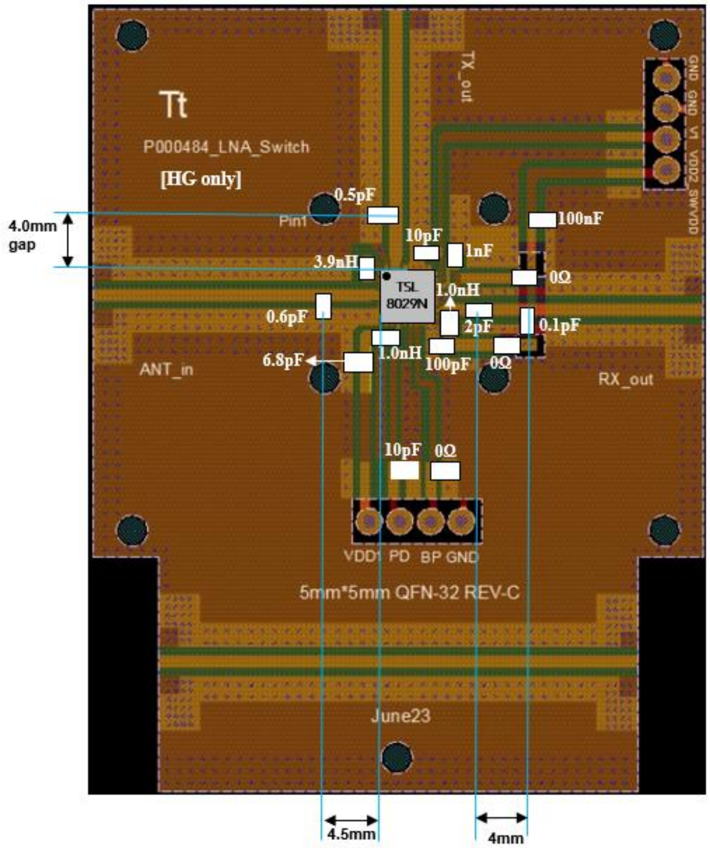


Figure 10.1.8 EVB Layout of the 3300-3800MHz EVB D [HG only]

Note: Series cap on ANT and TX ports should have 250V voltage ratings to handle 100W power. The heatsink needs to be added at bottom of this board for proper power spreading.

10.1.9 2900-3300MHz EVB E Schematic

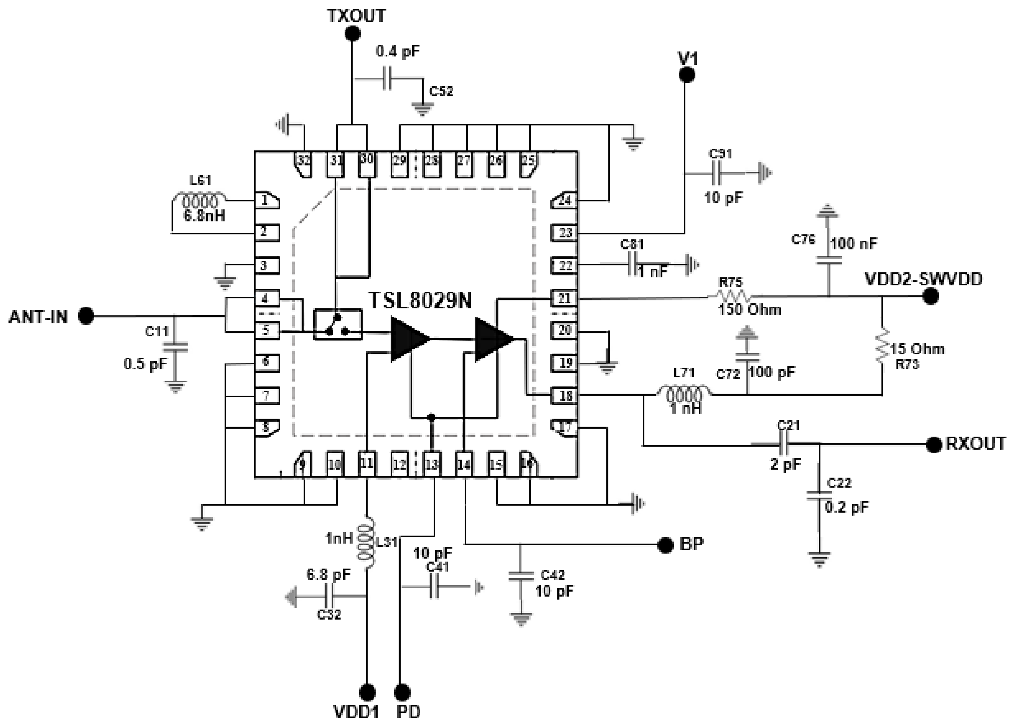


Figure 10.1.9 Schematic of the 2900-3300MHz EVB E

Table 10.1.9 BOM of the 2900-3300MHz EVB E

Component ID	Value	Manufacturer	Recommended Part Number	Qty
C11	0.5 pF	Murata	600S0R5BT250XT	1
C21	2 pF	Murata	GJM1555C1H2R0BB01D	1
C22	0.2 pF	Murata	GJM1555C1HR20BB01J	1
L31, L71	1 nH	Coil craft	0402DC-1N0XJRW	2
C32	6.8 pF	Murata	GJM1555C1H6R8BB01D	1
C41, C42, C91	10pF	Murata	GJM1555C1H100JB01D	3
C52	0.4pF	Murata	600S0R4BT250XT	1
L61	3.9 nH	Coil craft	0402DC-3N9XGRW	1
C72	100 pF	AVX	04025A101JAT4A	1
R73	15 Ω	Panasonic	ERJ-H2RD15R0X	1
R75	150 Ω	Panasonic	ERJ-2RHD1500X	1
C76	100 nF	TDK	C1005X7R1H104K050BE	1
C81	1 nF	Murata	04025C102JAT2A	1
PCB	Rogers RO4350B, 20 mils, 1 oz copper			1

10.1.10 2900-3300MHz EVB E Layout

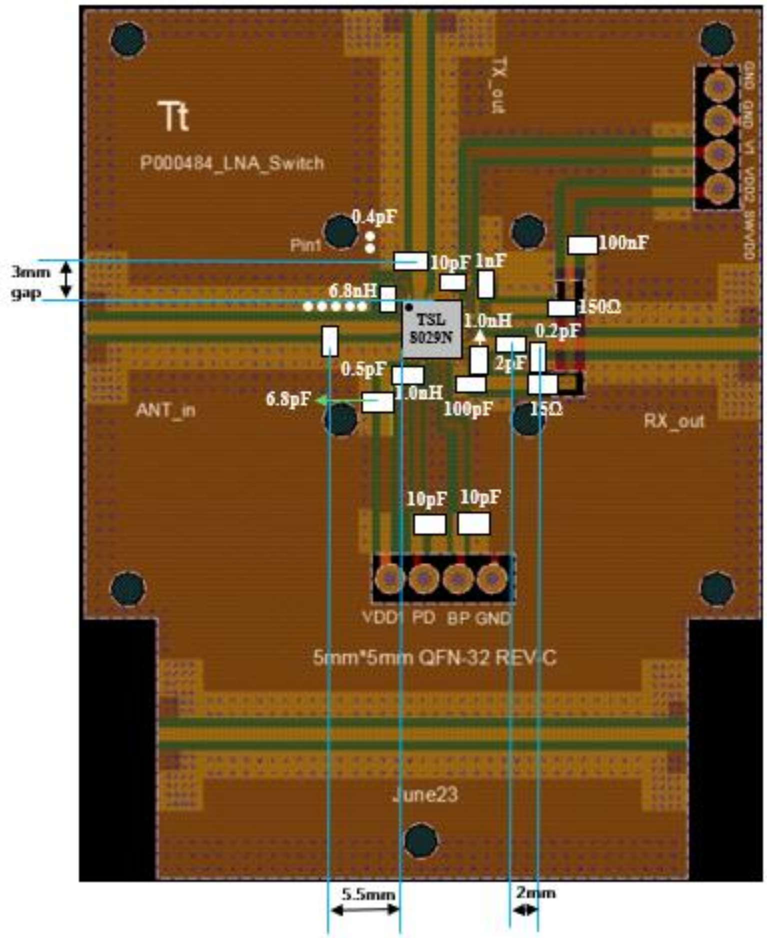


Figure 10.1.10 EVB Layout of the 2900-3300MHz EVB H

Note: Series cap on ANT and TX ports should have 250V voltage ratings to handle 100W power. The heatsink needs to be added at bottom of this board for proper power spreading.

11. TEST PROCEDURE

Biasing sequence

To properly bias the TSL8029N-EVB-C, follow these steps:
Ground the Gnd test point.

- Apply bias to the VDD2_SWVDD and VDD1=5V test points.
- Apply bias to the V1 test point.
- Apply bias to the Vdd1 test point.
- Apply bias to the BP test points.
- Apply bias to the PD test point.
- Apply an RF input signal.

The TSL8029N-EVB-C is shipped fully assembled and tested. Figure 11.1 illustrates a basic test setup diagram for evaluating s-parameters in RX mode, including receive gain, transmit insertion loss and isolation, and RF input and output return losses using a network analyzer. Follow these steps to complete the test setup and verify the operation of the TSL8029N-EVB-C:

1. Connect the Gnd test point to the ground terminal of the power supply.
2. Connect the Vdd1, SWVDD and Vdd2 test points to the voltage output terminal of a 5 V supply that sources a current of approximately 90 mA in receive operation for high gain mode or 4-5 mA for power-down mode.
3. Connect the BP, PD, and V1 test points to the ground terminal of the power supply for high gain receive operation. The TSL8029-EVB-C can be configured in different modes by connecting the control test points to 5 V or ground, as shown in Table 7.2 and Table 7.3.
4. Connect a calibrated network analyzer to the ANT_in, TX_out, and RX_out SMA connectors. Sweep the frequency from 1 GHz to 6 GHz and set the power to -25 dBm.

The TSL8029N-EVB-C is expected to have a high and low receive gain of 33 dB and 14.5 dB respectively at 3.6 GHz. Refer Figure 9.2.1 to Figure 9.1.1 for the expected results.
Additional test equipment is required for a comprehensive evaluation of the device's functions and performance.
For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with a noise option. It is recommended to use a low excess noise ratio (ENR) noise source.
For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.
For power compression and power handling evaluations, use a two-channel power meter and a signal generator. Ensure that the input power amplifier has sufficient power capacity. Test accessories such as couplers and attenuators must also have adequate power handling capabilities.
The TSL8029N-EVB-C is equipped with a support plate attached to the bottom side. To ensure optimal heat dissipation and minimize thermal rise during high power evaluations, attach this support plate to a heat sink using thermal grease.

Please note that measurements conducted at the SMA connectors of the TSL8029N-EVB-C include the losses of the SMA connectors and the PCB. The through line should be measured to calibrate the effects of the TSL8029N-EVB-C. The through line consists of an RF input line and an RF output line that are connected to the device and have equal lengths. The through line information is provided in the EVB.

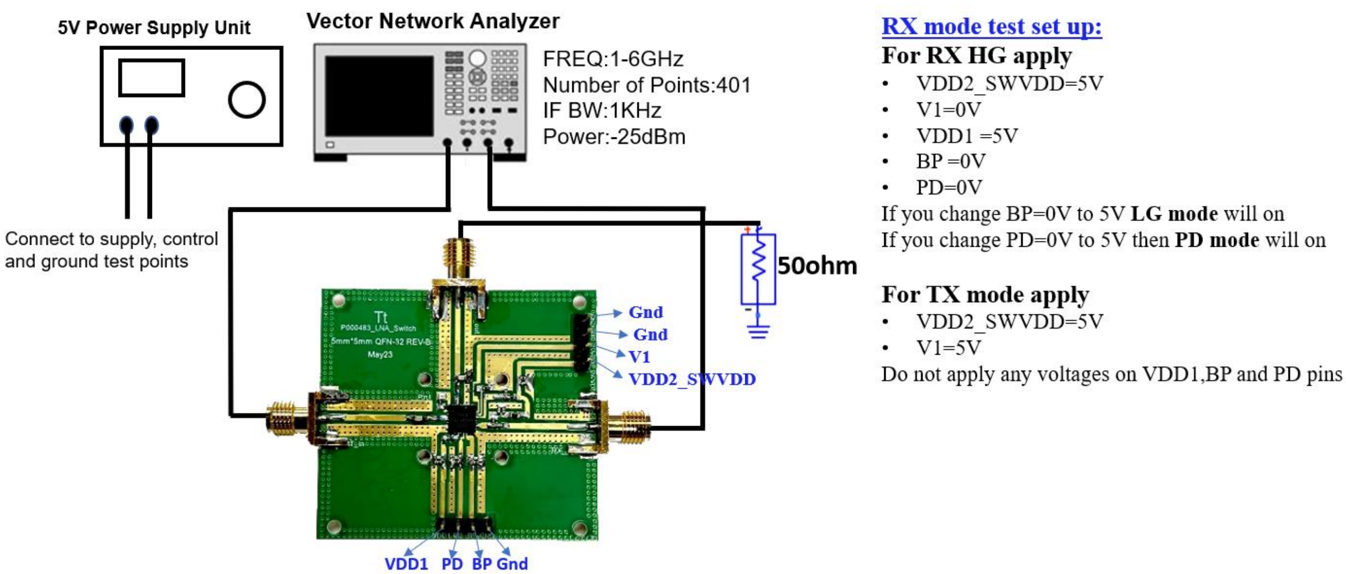


Figure 11.1 TEST Set Up Diagram for RX-mode.

12.0 Device Package Information

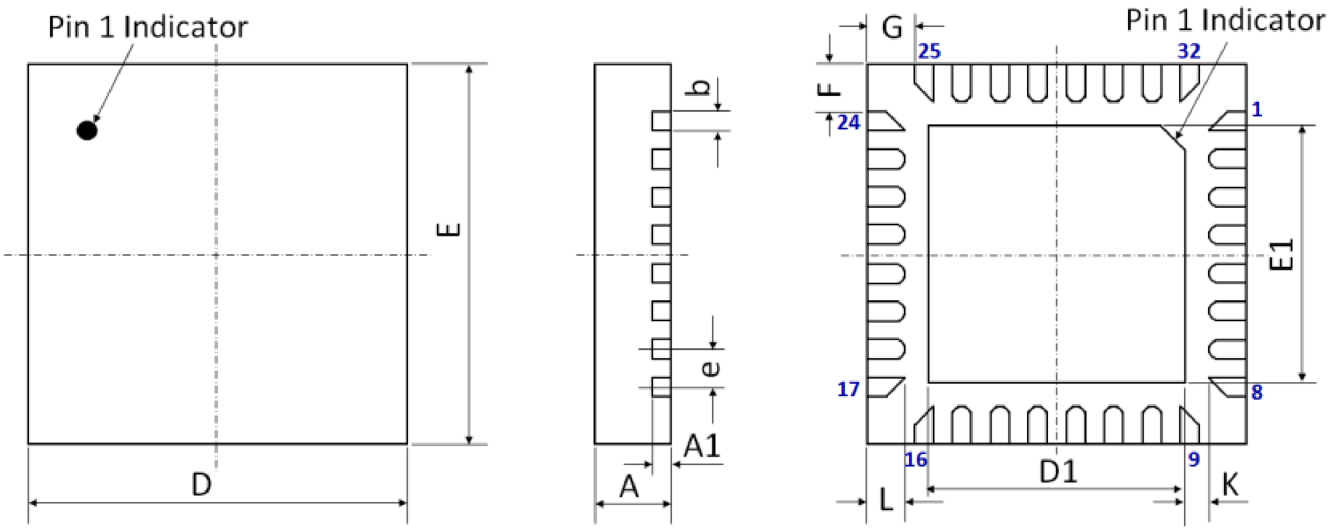


Figure 12.1 Device Package Drawing
(All dimensions are in mm)

Table 12.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.85	±0.05	E	5.00 BSC	±0.05
A1	0.203	±0.02	E1	3.2	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	5.00 BSC	±0.05	G	0.625	±0.05
D1	3.2	±0.06	L	0.40	±0.05
e	0.5 BSC	±0.05	K	0.5	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:
Please refer to application notes *TN-001* and *TN-003* at http://www.tagoretech.com for PCB and soldering related guidelines.

13.0 PCB Land Design

Guidelines:
[1] 4-layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall be placed on the center pad and should be filled/plugged with solder or copper.
[4] The maximum via number for the center pad is 5(X)×5(Y)=25.

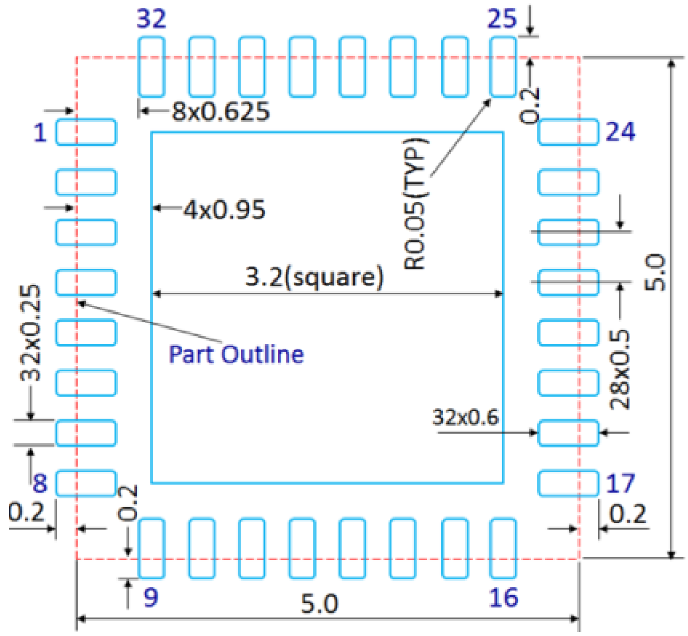


Figure 13.1 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined (Preferred)   Solder Mask Defined

Figure 13.2 Solder Mask Pattern
(Dimensions are in mm)

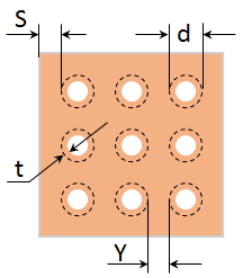


Figure 13.3 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.3mm; Plating Thickness t=25µm or 50µm)

14.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

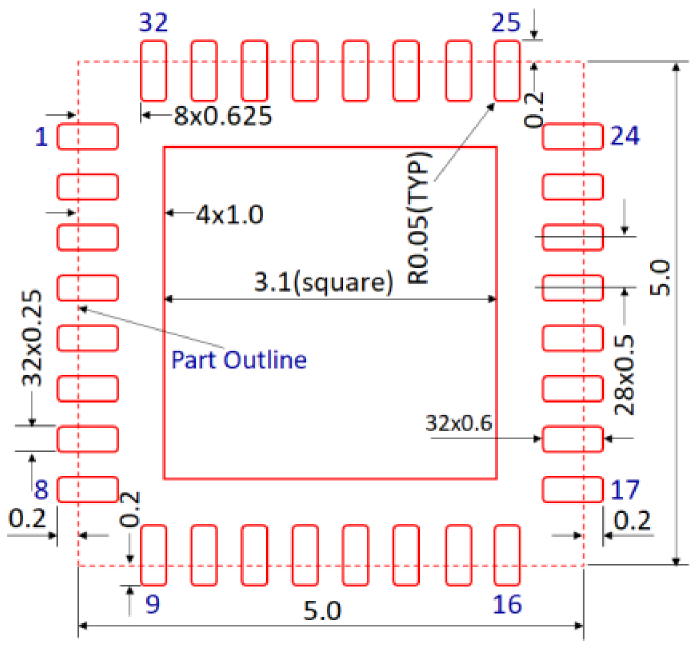


Figure 14.1 Stencil Openings
(Dimensions are in mm)

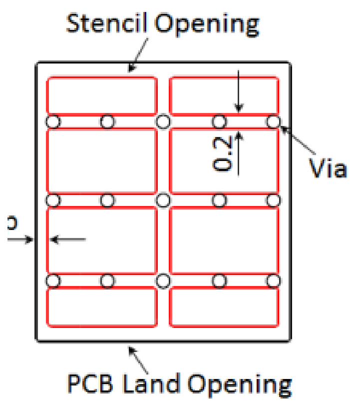


Figure 14.2 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

15.0 Tape and Reel Information

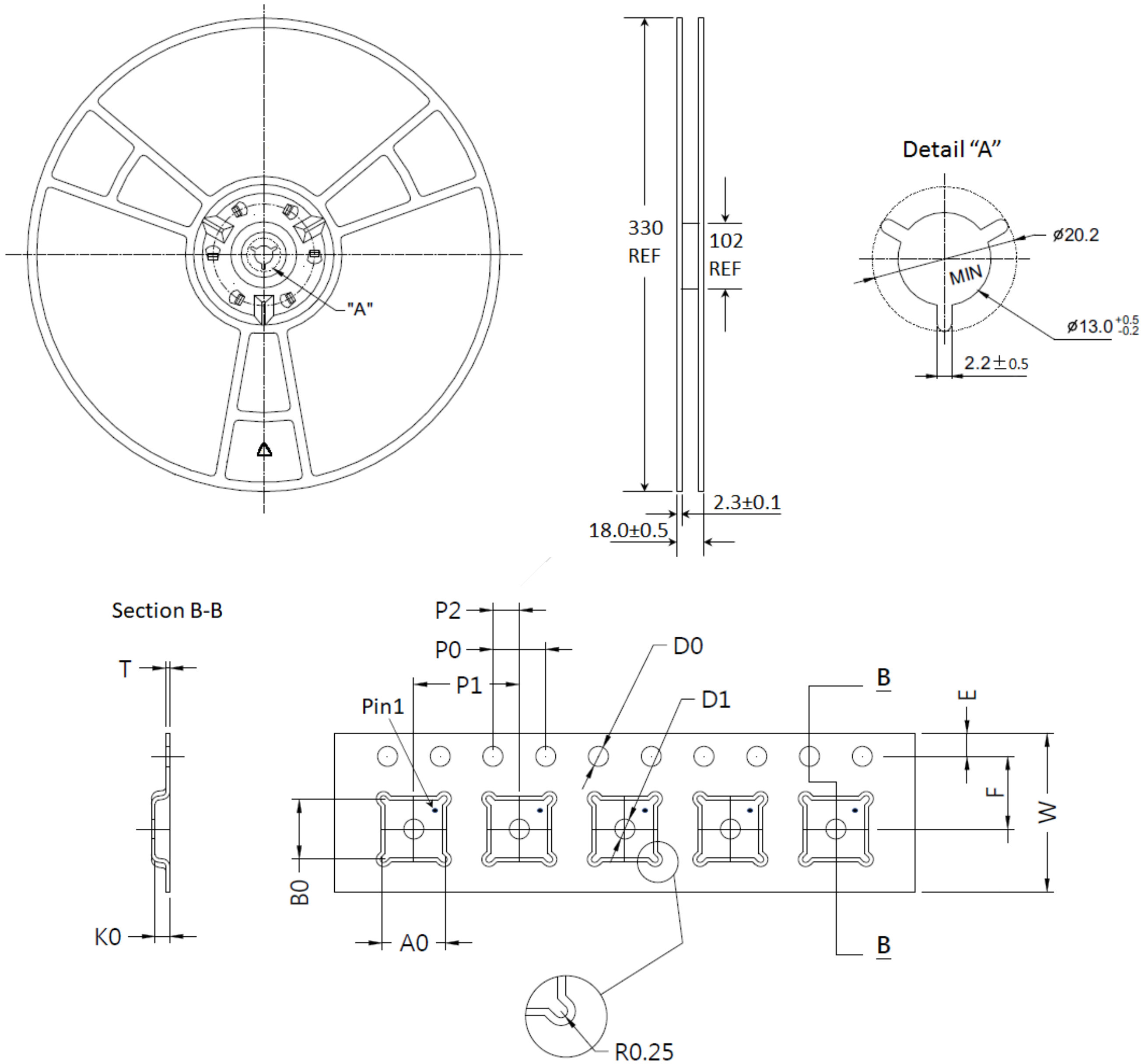


Figure 15.1 Tape and Reel Drawing

Table 14.1 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	5.35	±0.10	K0	1.10	±0.10
B0	5.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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