

PDFN56



Pin Definition:1. Source8. Drain2. Source7. Drain3. Source6. Drain4. Gate5. Drain

Key Parameter Performance

Parameter	Value	Unit
V _{DS}	75	V
R _{DS(on)} (max)	9	mΩ
Qg	125	nC

Block Diagram

Features

- Low On-Resistance
- Low Input Capacitance
- Low Gate Charge

Ordering Information

Part No.	Package	Packing		
TSM090N08PQ56 RLG	PDFN56	2.5kpcs / 13" Reel		

Note: "G" denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



N-Channel MOSFET

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	75	V	
Gate-Source Voltage		V_{GS}	±25	V	
Continuous Drain Current (Note 3)	T _C =25°C	1	80	A	
Continuous Drain Current	T _A =25°C	ID	18		
Drain Current-Pulsed (Note 1)		I _{DM}	300	А	
Single Pulse Avalanche Energy L=0.5mH		E _{AS}	200	mJ	
Movie Douge Discipation (Note 2)	T _C =25°C	D	104	W	
	T _A =25°C	PD	5.7		
Storage Temperature Range		T _{STG}	-55 to +150	°C	
Operating Junction Temperature Range		TJ	-55 to +150	°C	

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	R _{eJC}	1.2	°C/W
Thermal Resistance - Junction to Ambient	R _{OJA}	62	°C/W



Electrical Specifications (T_J=25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV _{DSS}	75			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 30A$	R _{DS(ON)}		7	9	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V _{GS(TH)}	2	3	4	V
Zero Gate Voltage Drain Current	$V_{DS} = 60V, V_{GS} = 0V$	I _{DSS}			1	μA
Gate Body Leakage	$V_{GS} = \pm 25V, V_{DS} = 0V$	I _{GSS}			±100	nA
Dynamic						
Total Gate Charge		Qg		125		nC
Gate-Source Charge	$V_{DS} = 30V, I_D = 30A,$	Q _{gs}		35		
Gate-Drain Charge	- V _{GS} = 10V	Q _{gd}		48		
Input Capacitance		C _{iss}		4800		
Output Capacitance	$V_{DS} = 30V, V_{GS} = 0V,$	C _{oss}		650		pF
Reverse Transfer Capacitance		C _{rss}		340		
Switching						
Turn-On Delay Time		t _{d(on)}		25		
Turn-On Rise Time	$V_{GS} = 10V, V_{DS} = 30V,$	t _r		21		
Turn-Off Delay Time	$R_G = 3\Omega$, $I_D = 30A$	t _{d(off)}		85		ns
Turn-Off Fall Time		t _f		42		
Drain-Source Diode Characteristics and Maximum Rating						
Drain-Source Diode Forward Voltage	V _{GS} =0V, I _S =30A	V_{SD}			1.3	V
Reverse Recovery Time		t _{rr}		32		ns
Reverse Recovery Charge	$I_{\rm S} = 30$ A, $ul/ul = 100$ A/µS	Q _{rr}		47		nC

1. Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2%.

2. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.

3. The maximum current is limited by package.



Electrical Characteristics Curves



Gate Source On Resistance



Drain-Source On-Resistance



Gate Threshold Voltage



2.0 1.8 1.6 Normalized On Resistance 1.4 1.2 1.0 0.8 0.6 V_{GS}=10V I_{DS}=30A 0.4 R_{DS(ON)}=7mΩ @ T_i=25°C 0.2 └─ -50 -25 100 125 150 175 0 25 50 75 T_i - Junction Temperature (°C)

Source-Drain Diode Forward Voltage





Electrical Characteristics Curves





Transient Thermal Impedance



Gate Charge







PDFN56 Mechanical Drawing



Marking Diagram



- Y = Year Code
- M = Month Code for Halogen Free Product
 (O=Jan, P=Feb, Q=Mar, R=Apl, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
- L = Lot Code



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