



TSM103/A

DUAL OPERATIONAL AMPLIFIER AND VOLTAGE REFERENCE

NOT FOR NEW DESIGN - REPLACED BY TSM103W

OPERATIONAL AMPLIFIER

- LOW INPUT OFFSET VOLTAGE : 0.5mV
typ. for TSM103A
- LOW SUPPLY CURRENT : 350 μ A/op.
(@ $V_{CC} = 5V$)
- MEDIUM BANDWIDTH (unity gain) : 0.9MHz
- LARGE OUTPUT VOLTAGE SWING : 0V to
($V_{CC} - 1.5V$)
- INPUT COMMON MODE VOLTAGE RANGE
INCLUDES GROUND
- WIDE POWER SUPPLY RANGE : 3 to 32V
 ± 1.5 TO $\pm 16V$

VOLTAGE REFERENCE

- FIXED OUTPUT VOLTAGE REFERENCE 2.5V
- 0.4% AND 1% VOLTAGE PRECISION
- SINK CURRENT CAPABILITY : 1 to 100mA
- TYPICAL OUTPUT IMPEDANCE : 0.2 Ω

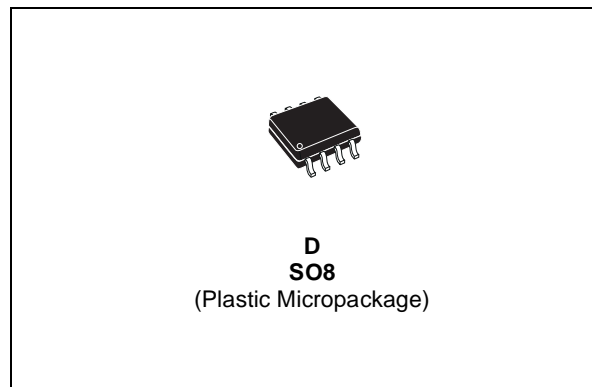
DESCRIPTION

The TSM103 is a monolithic IC that includes one independent op-amp and another op-amp for which the non inverting input is wired to a 2.5V fixed Voltage Reference. This device is offering space and cost saving in many applications like power supply management or data acquisition systems.

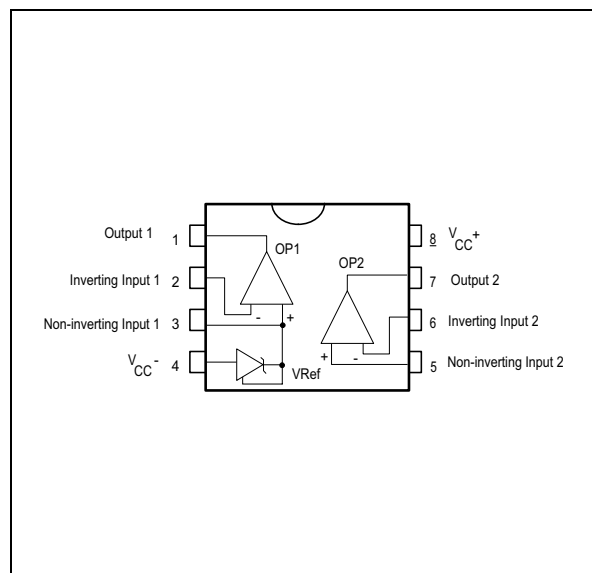
ORDER CODE

Part Number	Temperature Range	Package
		D
TSM103I/AI	-40°C, +105°C	•

D = Small Outline Package (SO) - also available in Tape & Reel (DT)



PIN CONNECTIONS (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	36	V
V_{id}	Differential Input Voltage	36	V
V_i	Input Voltage	-03. to +36	V
T_{oper}	Operating Free-air Temperature Range	-55 to +125	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient (SO package)	175	°C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Total Supply Current, excluding Current in the Voltage Reference VCC+ = 5V, no load Tmin. < Tamb < Tmax. VCC+ = 30V, no load Tmin. < Tamb < Tmax		0.7	1.2 2	mA

OPERATOR 2 (independent op-amp)
 $V_{CC}^+ = +5V$, $V_{CC} = \text{Ground}$, $V_o = 1.4V$, $T_{amb} = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage TSM103, $T_{amb} = 25^\circ\text{C}$ $T_{min.} \leq T_{amb} \leq T_{max.}$ TSM103A, $T_{amb} = 25^\circ\text{C}$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1 0.5	4 5 2 3	mV
DV_{io}	Input Offset Voltage Drift		7		$\mu\text{V}/^\circ\text{C}$
I_{io}	Input Offset Current $T_{min.} \leq T_{amb} \leq T_{max.}$		2	30 50	nA
I_{ib}	Input Bias Current $T_{min.} \leq T_{amb} \leq T_{max.}$		20	150 200	nA
Avd	Large Signal Voltage Gain $V_{CC} = 15V$, $R_L = 2k$, $V_o = 1.4V$ to $11.4V$ $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio $V_{CC} = 5V$ to $30V$	65	100		dB
Vicm	Input Common Mode Voltage Range $V_{CC} = +30V$ - see note ¹⁾ $T_{min.} \leq T_{amb} \leq T_{max.}$	0 0		$(V_{CC}^+) - 1.5$ $(V_{CC}^+) - 2$	V
CMR	Common Mode Rejection Ratio $T_{min.} \leq T_{amb} \leq T_{max.}$	70 60	85		dB
I_{source}	Output Current Source $V_{CC} = +15V$, $V_o = 2V$, $V_{id} = +1V$	20	40		mA
I_o	Short Circuit to Ground $V_{CC} = +15V$		40	60	mA
I_{sink}	Output Current Sink $V_{id} = -1V$, $V_{CC} = +15V$, $V_o = 2V$	10	20		mA
V_{OH}	High Level Output Voltage $V_{CC}^+ = 30V$ $T_{amb} = 25^\circ\text{C}$, $R_L = 10k$ $T_{min.} \leq T_{amb} \leq T_{max.}$	27 27	28		V
V_{OL}	Low Level Output Voltage $R_L = 10k$ $T_{min.} \leq T_{amb} \leq T_{max.}$		5	20 20	mV
SR	Slew Rate at Unity Gain $V_i = 0.5$ to $3V$, $V_{CC} = 15V$ $R_L = 2k$, $C_L = 100\text{pF}$, unity gain	0.2	0.4		$\text{V}/\mu\text{s}$
GBP	Gain Bandwidth Product $V_{CC} = 30V$, $R_L = 2k$, $C_L = 100\text{pF}$ $f = 100\text{kHz}$, $V_{in} = 10\text{mV}$	0.5	0.9		MHz
THD	Total Harmonic Distortion $f = 1\text{kHz}$ $A_V = 20\text{dB}$, $R_L = 2k$, $V_{CC} = 30V$ $C_L = 100\text{pF}$, $V_o = 2V_{pp}$		0.02		%

1. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5V$. But either of both inputs can go to +36V without damage.

OPERATOR 1 (op-amp with non-inverting input connected to the internal Vref)

 $V_{CC}^+ = +5V$, $V_{CC}^- = \text{Ground}$, $T_{amb} = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $V_{icm} = 0V$ TSM103, $T_{amb} = 25^\circ\text{C}$ $T_{min.} \leq T_{amb} \leq T_{max.}$ TSM103A, $T_{amb} = 25^\circ\text{C}$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1 0.5	4 5 2 3	mV
DV_{io}	Input Offset Voltage Drift		7		$\mu\text{V}/^\circ\text{C}$
I_{ib}	Input Bias Current negative input		20		nA
Avd	Large Signal Voltage Gain $V_{icm} = 0V$ $V_{CC} = 15V$, $R_L = 2k$		100		V/mV
SVR	Supply Voltage Rejection Ratio $V_{icm} = 0V$ $V_{CC}^+ = 5V$ to $30V$	65	100		dB
I_{source}	Output Current Source $V_o = 2V$ $V_{CC} = +15V$, $V_{id} = +1V$	20	40		mA
I_o	Short Circuit to Ground $V_{CC} = +15V$		40	60	mA
I_{sink}	Output Current Sink $V_{id} = -1V$, $V_{CC} = +15V$, $V_o = 2V$	10	20		mA
V_{OH}	High Level Output Voltage $V_{CC}^+ = 30V$ $T_{amb} = 25^\circ\text{C}$, $R_L = 10k$ $T_{min.} \leq T_{amb} \leq T_{max.}$	27 27	28		V
V_{OL}	Low Level Output Voltage $R_L = 10k$ $T_{min.} \leq T_{amb} \leq T_{max.}$		5	20 20	mV
SR	Slew Rate at Unity Gain $V_i = 0.5$ to $2V$, $V_{CC} = 15V$ $R_L = 2k$, $C_L = 100\text{pF}$, unity gain	0.2	0.4		$\text{V}/\mu\text{s}$
GBP	Gain Bandwidth Product $V_{CC} = 30V$, $R_L = 2k$, $C_L = 100\text{pF}$ $f = 100\text{kHz}$, $V_{in} = 10\text{mV}$	0.5	0.9		MHz
THD	Total Harmonic Distortion $f = 1\text{kHz}$ $A_V = 20\text{dB}$, $R_L = 2k$, $V_{CC} = 30V$ $C_L = 100\text{pF}$, $V_o = 2V_{pp}$		0.02		%

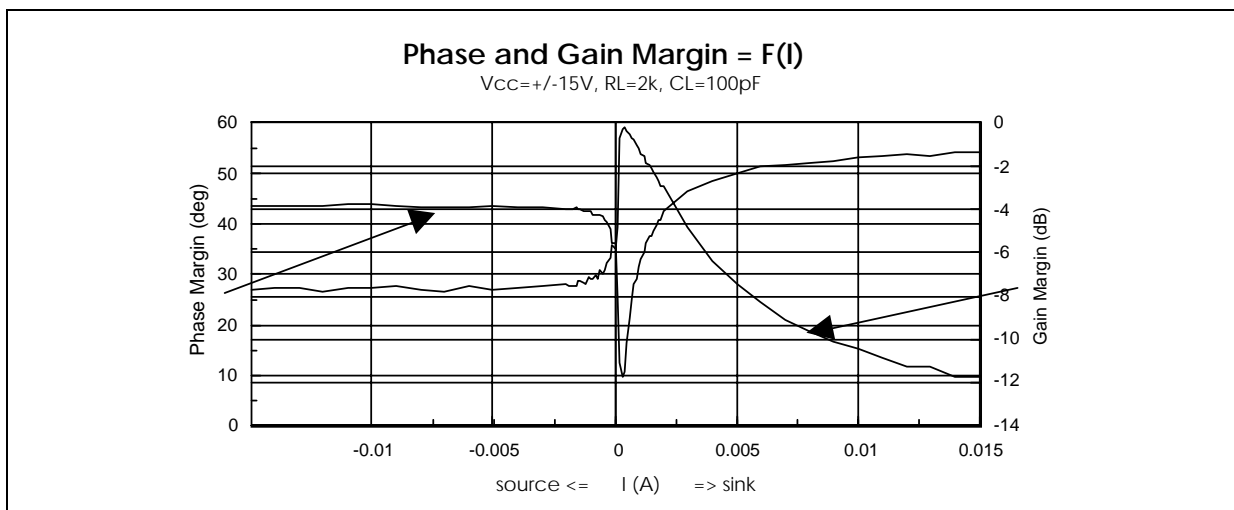
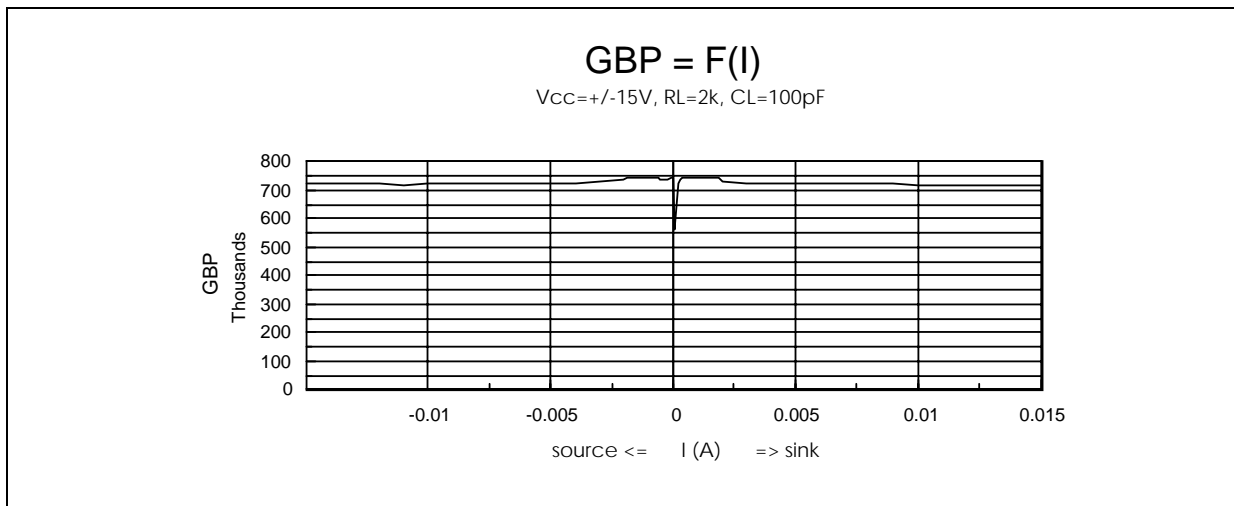
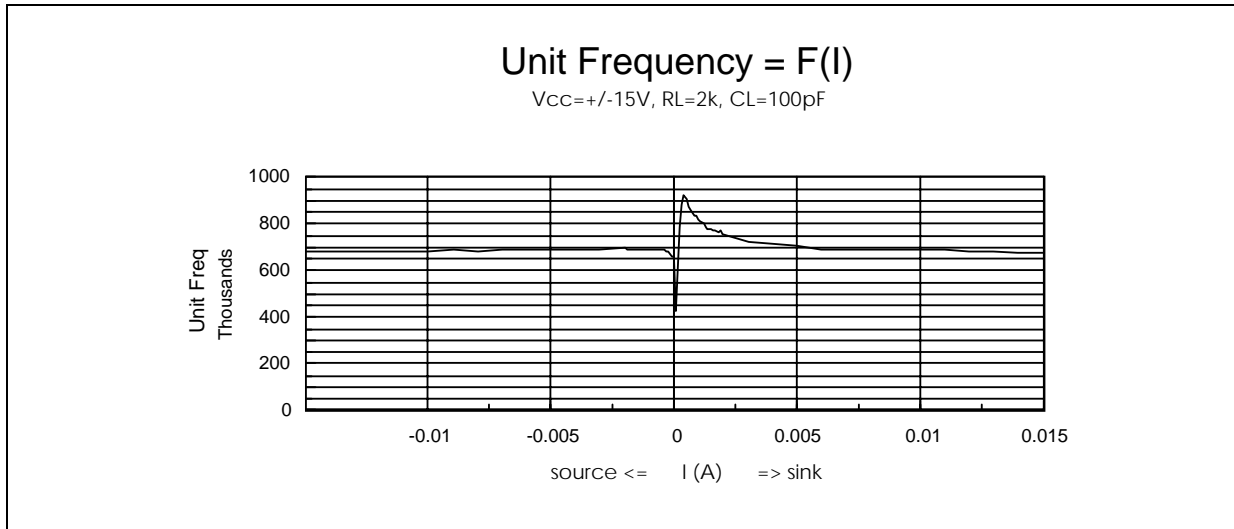
VOLTAGE REFERENCE

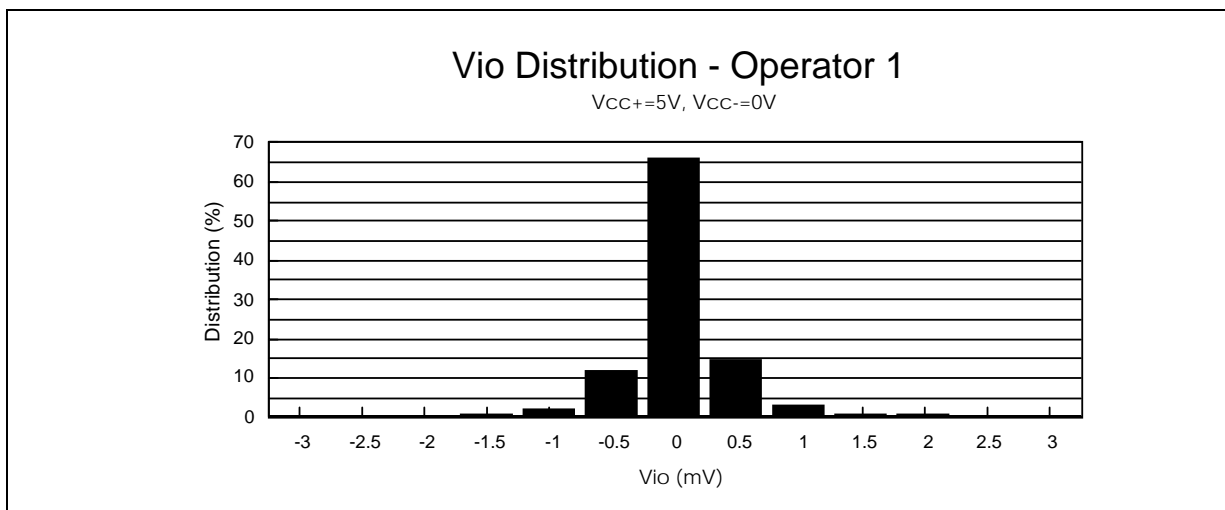
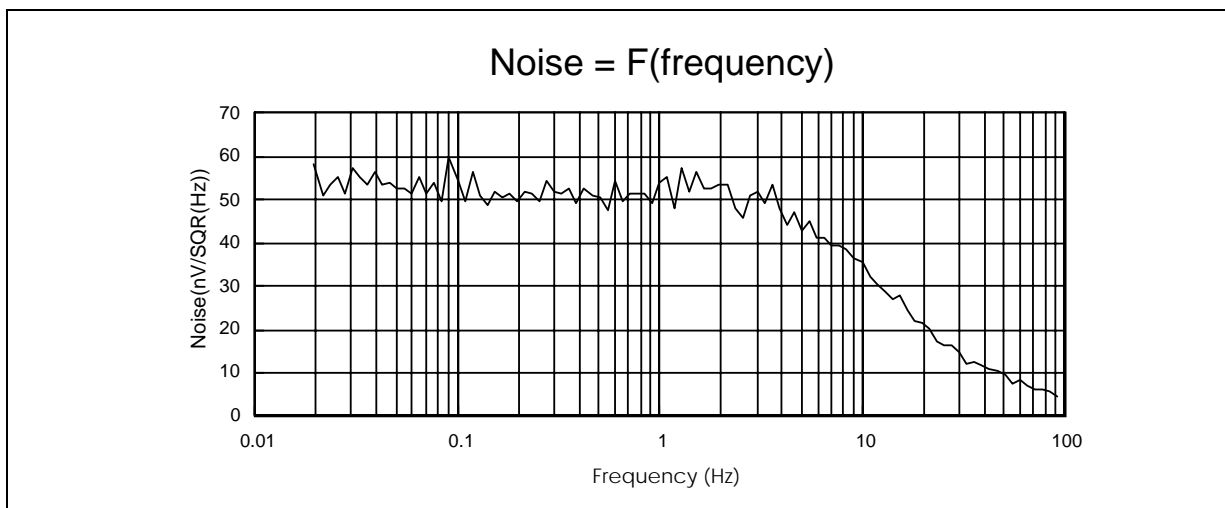
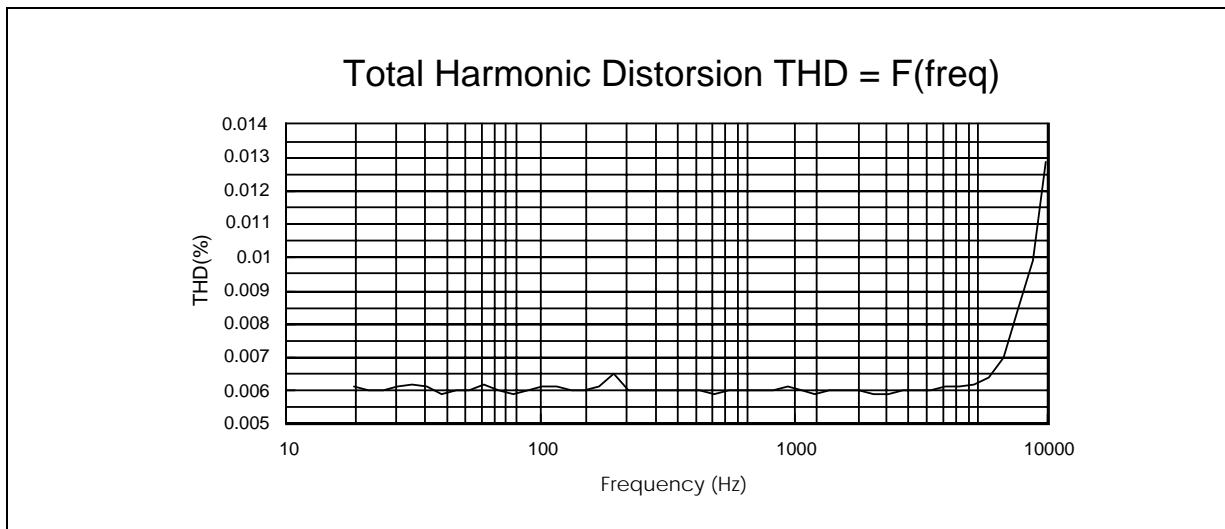
Symbol	Parameter	Value	Unit
I_k	Cathode Current	1 to 100	mA

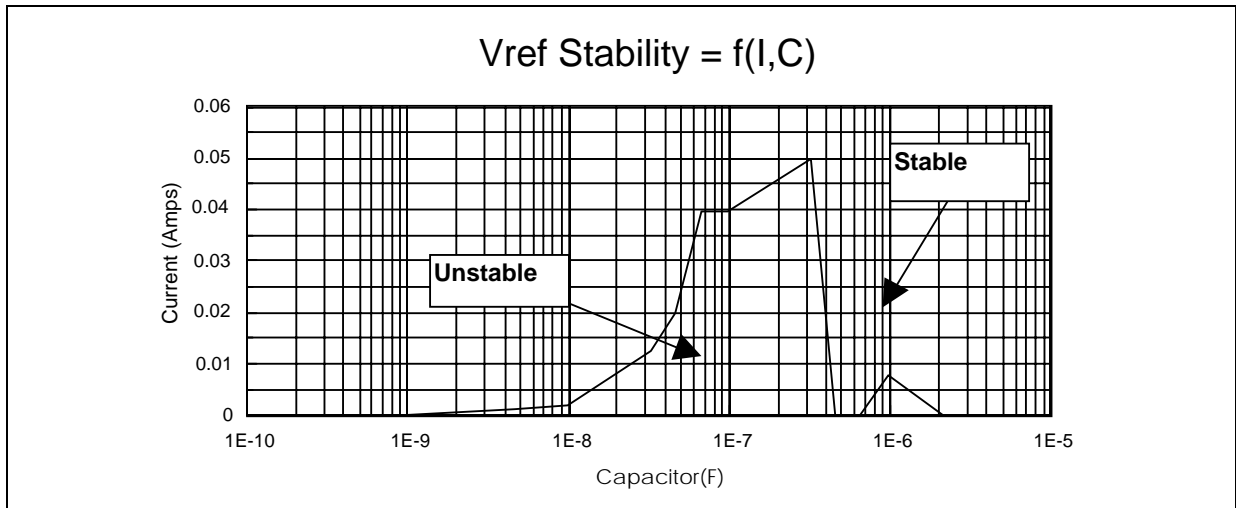
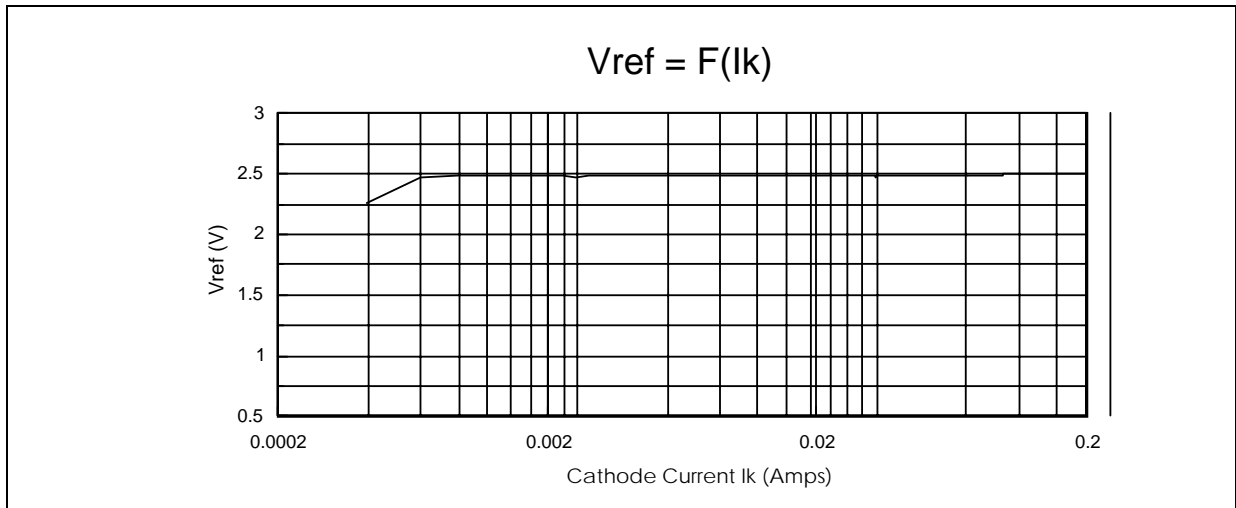
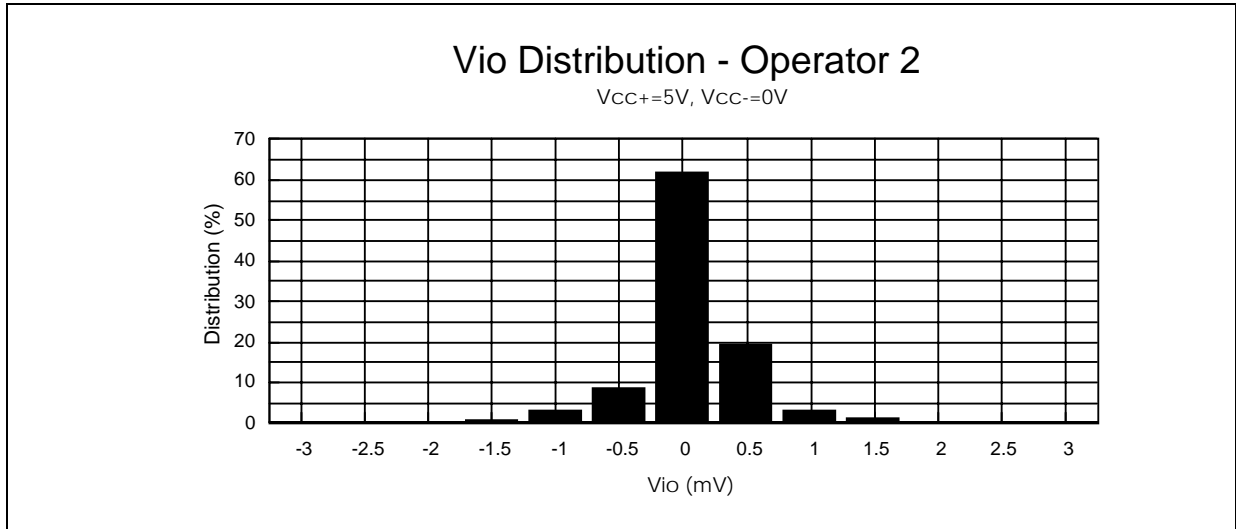
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ref}	Reference Input Voltage TSM103, $T_{amb} = 25^{\circ}\text{C}$ $T_{min.} \leq T_{amb} \leq T_{max.}$ TSM103A, $T_{amb} = 25^{\circ}\text{C}$ $T_{min.} \leq T_{amb} \leq T_{max.}$	2.475 2.45 2.49 2.48	2.5 2.5	2.525 2.55 2.51 2.52	V
ΔV_{ref}	Reference Input Voltage Deviation Over Temperature Range $V_{KA} = V_{ref}$; $I_k = 10\text{mA}$ $T_{min.} \leq T_{amb} \leq T_{max.}$		7	30	mV
I_{min}	Minimum Cathode Current for Regulation $V_{KA} = V_{ref}$		0.5	1	mA
$ Z_{KA} $	Dynamic Impedance - note 1) $V_{KA} = V_{ref}$, $\Delta I_K = 1$ to 100mA, $f < 1\text{kHz}$		0.2	0.5	Ω

1. The dynamic impedance is defined as $|Z_{KA}| = \Delta V_{KA} / \Delta I_K$

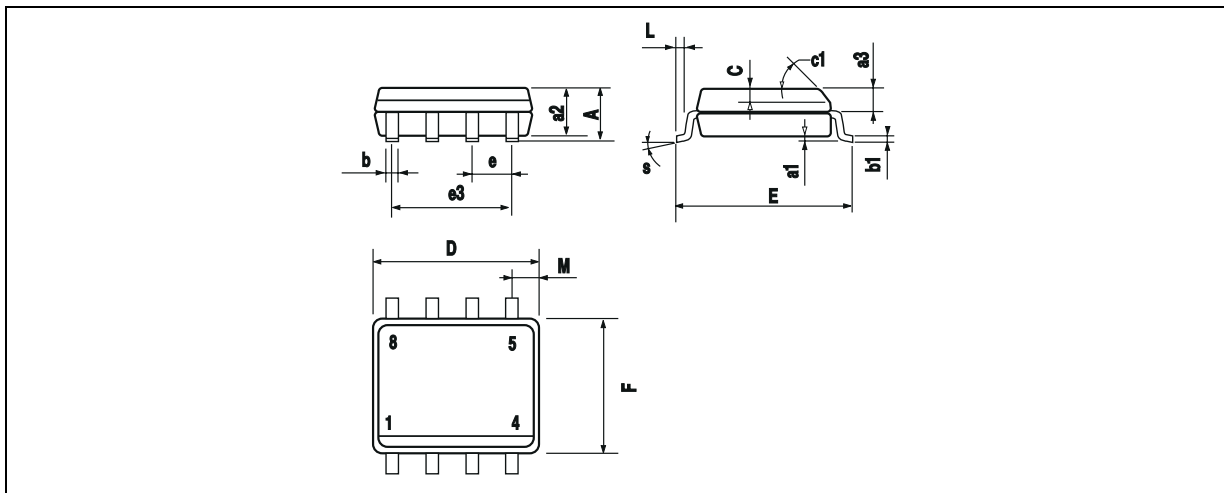
OPERATIONAL AMPLIFIERS







PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

<http://www.st.com>

