

P-Channel Power MOSFET

-30V, -30A, 15mΩ

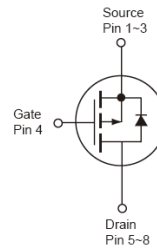
Features

- Fast Switching
- Suitable for 4.5V drive applications
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

Application

- Load Switch
- Networking

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	-30	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	15
	$V_{GS} = -4.5V$	30
Q_g	4.1	nC


Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	-30
		$T_C = 100^\circ\text{C}$	-19
Pulsed Drain Current (Note 2)	I_{DM}	-120	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	23	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	5.4	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 3)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	BV _{DSS}	-30	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	V _{GS(TH)}	-1.2	-1.6	-2.5	V
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} = 0V	I _{DSS}	--	--	-1	μA
Drain-Source On-State Resistance	V _{GS} = -10V, I _D = -8A	R _{DS(ON)}	--	13	15	mΩ
	V _{GS} = -4.5V, I _D = -6A			22	30	
Dynamic (Note 4)						
Total Gate Charge	V _{DS} = -15V, I _D = -8A, V _{GS} = -4.5V	Q _g	--	14.6	--	nC
Gate-Source Charge		Q _{gs}	--	4.1	--	
Gate-Drain Charge		Q _{gd}	--	6.3	--	
Input Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	1730	--	pF
Output Capacitance		C _{oss}	--	180	--	
Reverse Transfer Capacitance		C _{rss}		125		
Switching (Note 5)						
Turn-On Delay Time	V _{DD} = -15V, R _{GEN} = 6Ω, I _D = -1A, V _{GS} = -10V,	t _{d(on)}	--	9	--	ns
Turn-On Rise Time		t _r	--	21.8	--	
Turn-Off Delay Time		t _{d(off)}	--	59.8	--	
Turn-Off Fall Time		t _f	--	14.4	--	
Source-Drain Diode (Note 3)						
Forward On Voltage	I _S = -1 A, V _{GS} = 0V	V _{SD}	--	--	-1	V

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
4. For DESIGN AID ONLY, not subject to production testing.
5. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

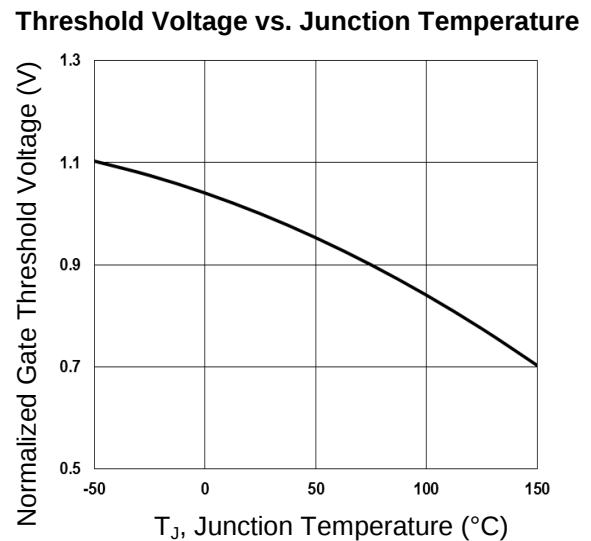
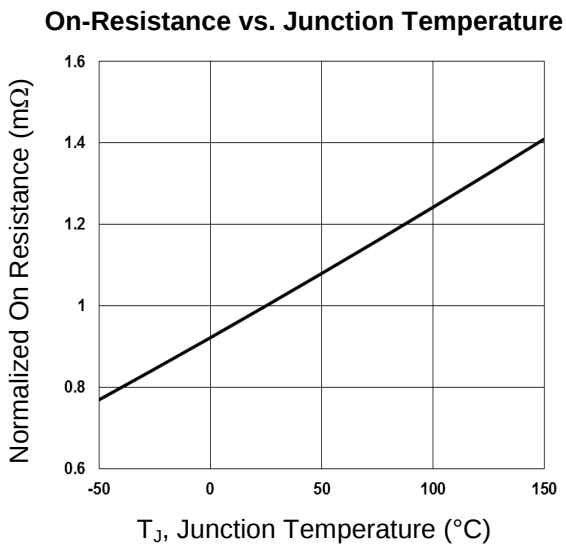
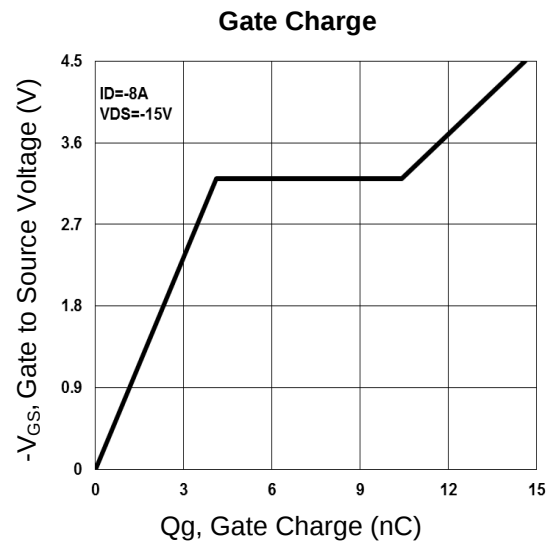
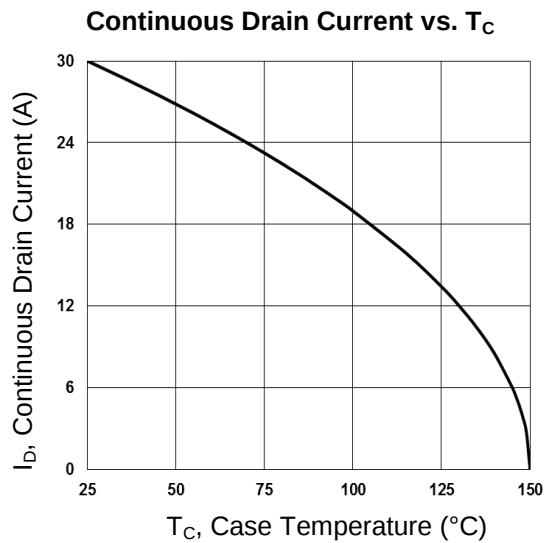
PART NO.	PACKAGE	PACKING
TSM150P03PQ33 RGG	PDFN33	5,000pcs / 13"Reel

Note:

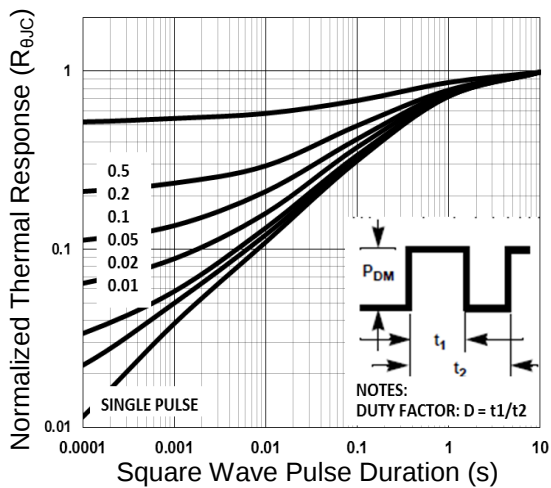
1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

CHARACTERISTICS CURVES

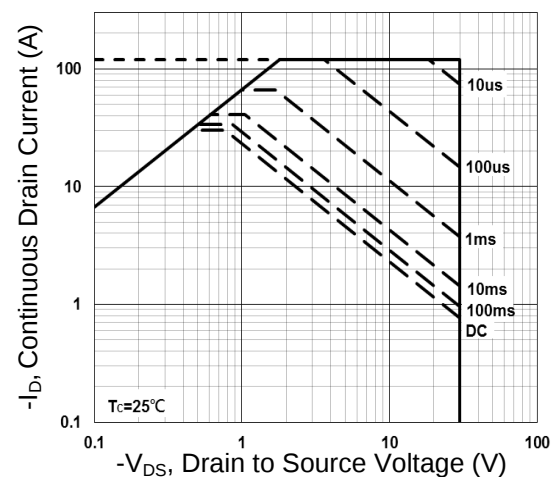
($T_C = 25^\circ\text{C}$ unless otherwise noted)



Normalized Thermal Transient Impedance Curve

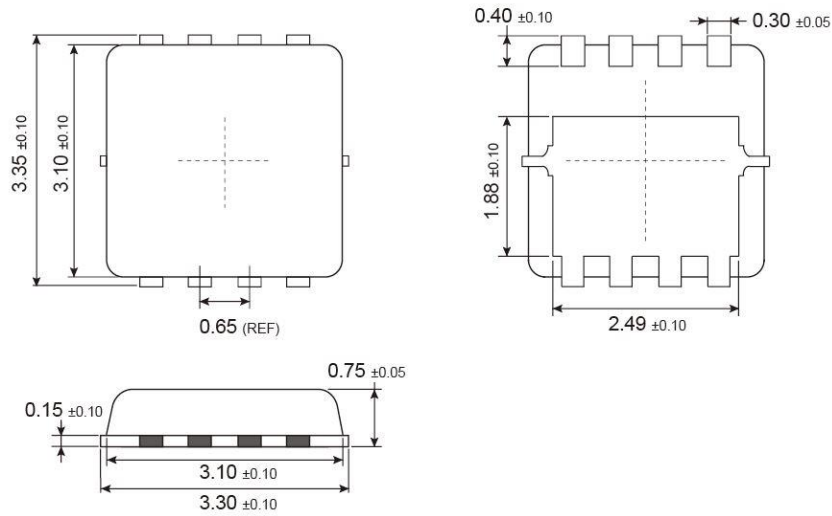


Maximum Safe Operating Area

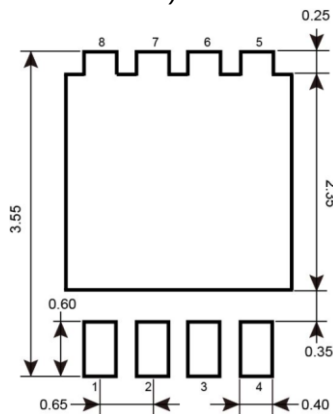


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

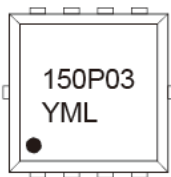
PDFN33



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code for Halogen Free Product
 - O** =Jan **P** =Feb **Q** =Mar **R** =Apr
 - S** =May **T** =Jun **U** =Jul **V** =Aug
 - W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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