

N-Channel Power MOSFET

100V, 160A, 5.5mΩ

FEATURES

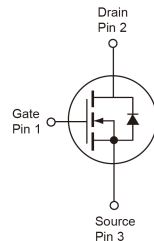
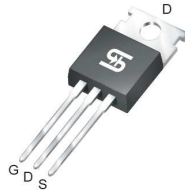
- Advanced Trench Technology
- Low $R_{DS(ON)}$ 5.5mΩ (Max.)
- Low gate charge typical @ 154nC (Typ.)
- Low Crss typical @ 260pF (Typ.)

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	100	V
$R_{DS(on)}$ (max)	5.5	mΩ
Q_g	154	nC



TO-220



Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	160	A
	$T_C = 70^\circ\text{C}$		127	
	$T_A = 25^\circ\text{C}$		14.2	A
	$T_A = 70^\circ\text{C}$		11.4	
Pulsed Drain Current (Note 2)		I_{DM}	620	A
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_{DTOT}	300	W
	$T_C = 70^\circ\text{C}$		210	
	$T_A = 25^\circ\text{C}$		2.4	W
	$T_A = 70^\circ\text{C}$		1.68	
Single Pulsed Avalanche Energy (Note 3)		E_{AS}, E_{AR}	400	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}, I_{AR}	40	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +175	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.5	$^{\circ}\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62.5	$^{\circ}\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 4)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250uA	BV _{DSS}	100	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2	3	4	V
Zero Gate Voltage Drain Current	V _{DS} = 80V, V _{GS} = 0V	I _{DSS}	--	--	1	uA
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 30A	R _{DS(on)}	--	4.5	5.5	mΩ
Dynamic ^(Note 5)						
Total Gate Charge	V _{DS} = 30V, I _D = 30A, V _{GS} = 10V	Q _g	--	154	--	nC
Gate-Source Charge		Q _{gs}	--	35	--	
Gate-Drain Charge		Q _{gd}	--	40	--	
Input Capacitance	V _{DS} = 30V, V _{GS} = 0V, F = 1.0MHz	C _{iss}	--	9840	--	pF
Output Capacitance		C _{oss}	--	750	--	
Reverse Transfer Capacitance		C _{rss}	--	260	--	
Switching ^(Note 6)						
Turn-On Delay Time	V _{GS} = 10V, V _{DS} = 30V, R _G = 3.3Ω	t _{d(on)}	--	25	--	ns
Turn-On Rise Time		t _r	--	40	--	
Turn-Off Delay Time		t _{d(off)}	--	85	--	
Turn-Off Fall Time		t _f	--	45	--	
Source-Drain Diode ^(Note 4)						
Forward Voltage	V _{GS} =0V, I _S =30A	V _{SD}	-	0.8	1.3	V
Reverse Recovery Time	I _S = 30A , T _J = 25°C	t _{rr}		120		nS
Reverse Recovery Charge	dI/dt = 100A/us	Q _{rr}		160		nC

Notes:

- Current limited by package.
- Pulse width limited by the maximum junction temperature.
- $L = 0.5\text{mH}, I_{AS} = 40\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$
- Pulse test: $PW \leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM160N10CZ C0G	TO-220	50pcs / Tube

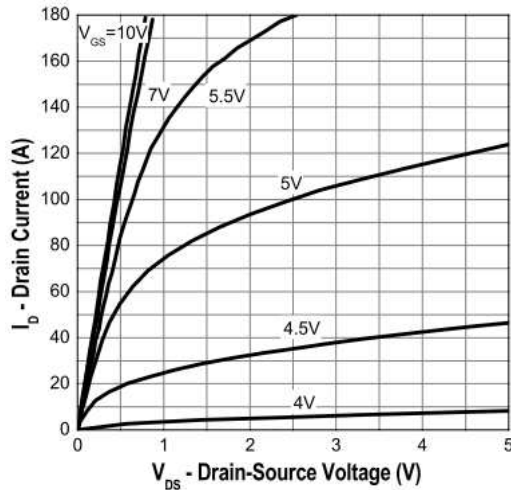
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

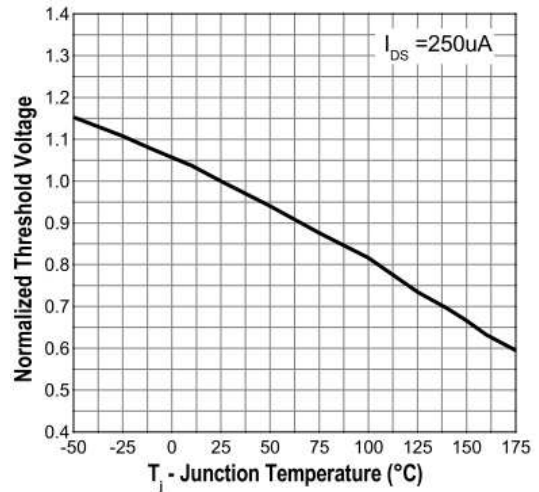
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

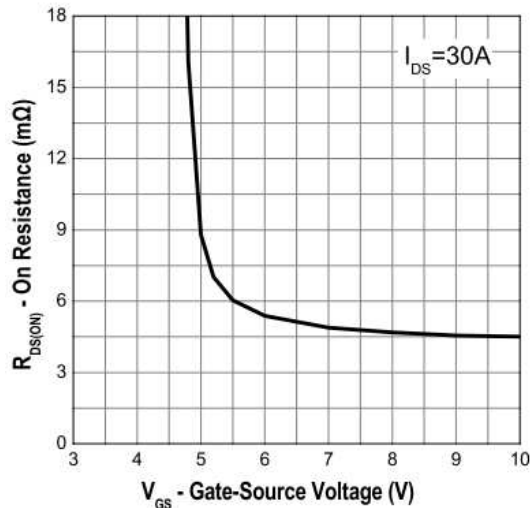
Output Characteristics



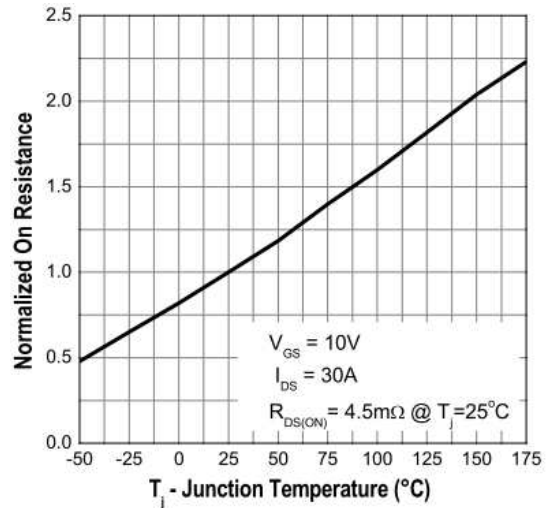
Gate Threshold Voltage



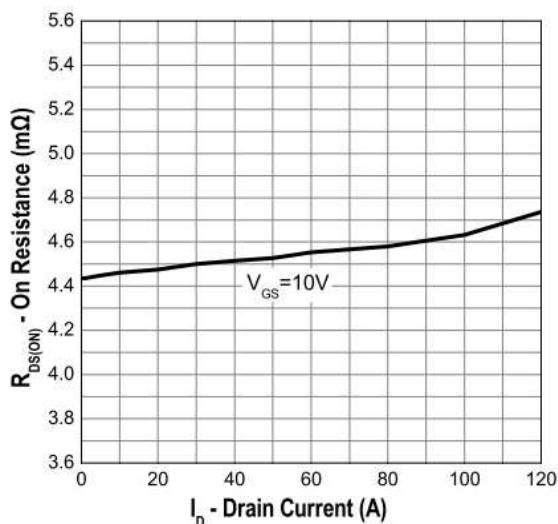
Gate Source On Resistance



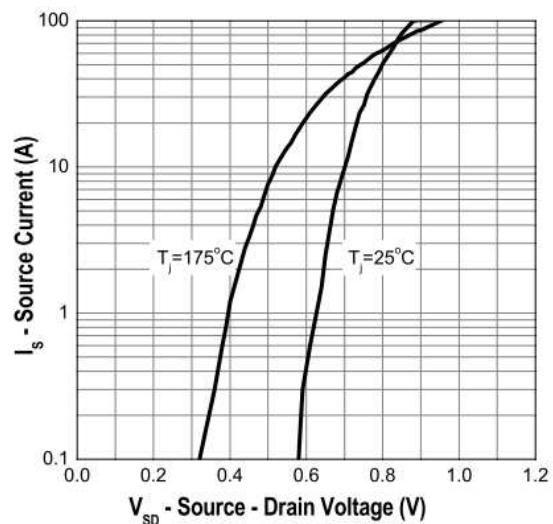
Drain-Source On Resistance



Drain-Source On-Resistance



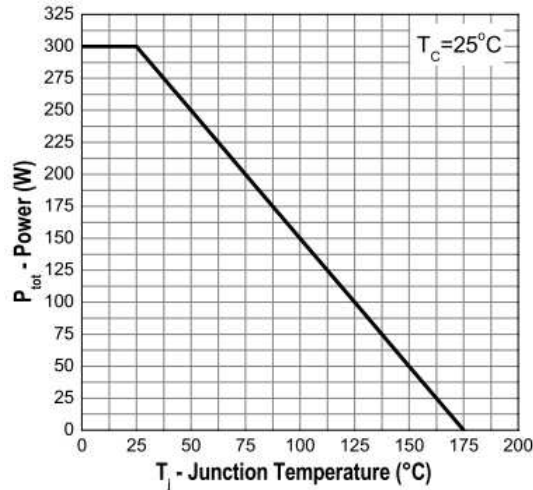
Source-Drain Diode Forward Voltage



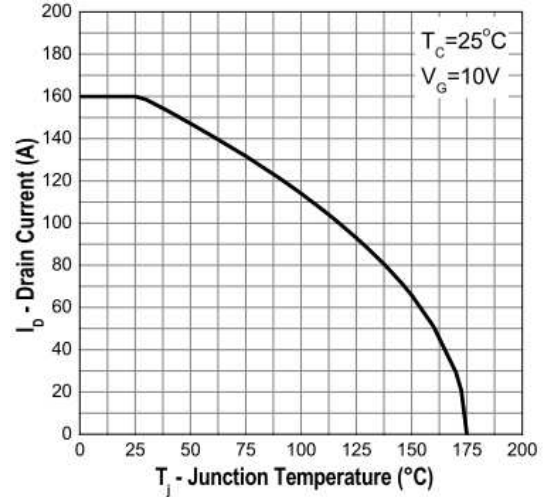
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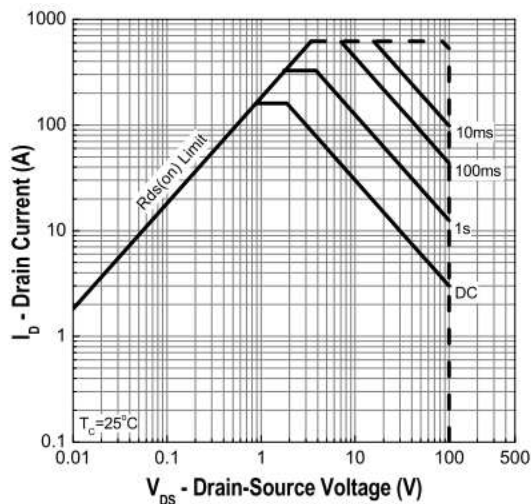
Power Derating



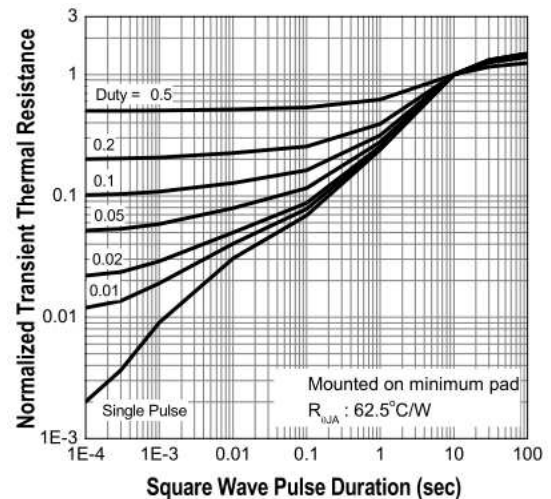
Drain Current vs. Junction Temperature



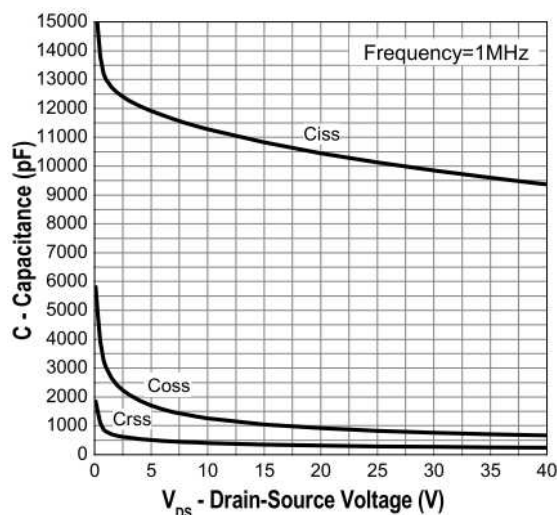
Safe Operation Area



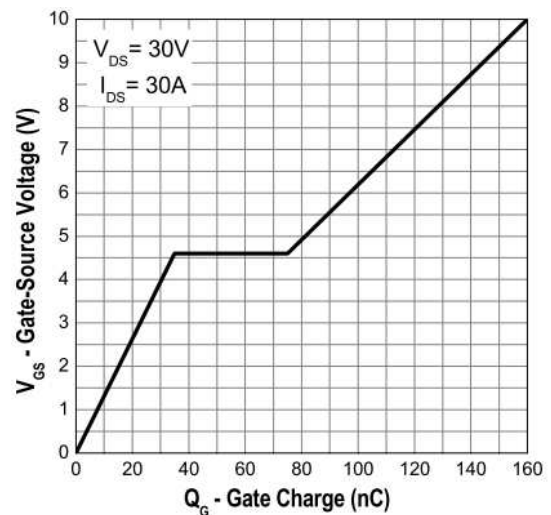
Transient Thermal Impedance



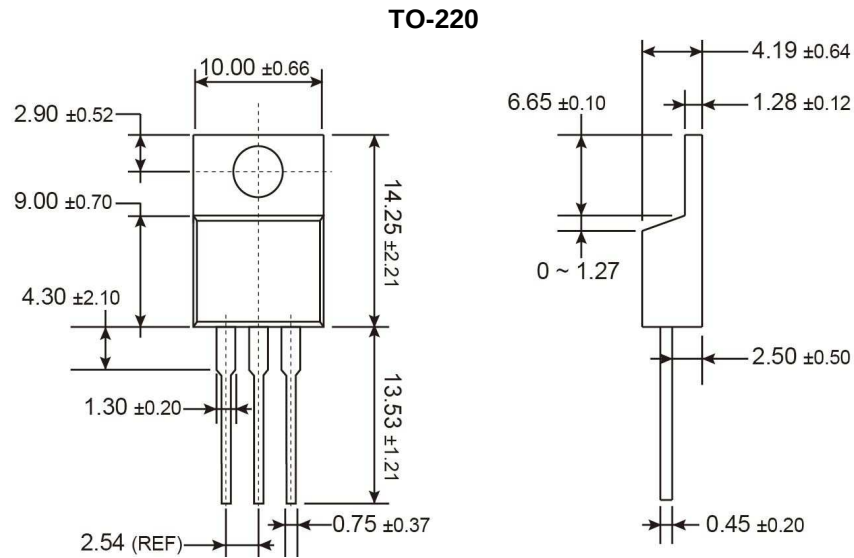
Capacitance



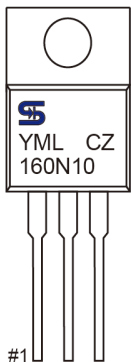
Gate Charge



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



Marking Diagram



Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
W =Sep **X** =Oct **Y** =Nov **Z** =Dec
L = Lot Code (1~9, A~Z)

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