N-Channel Power MOSFET

60V, 42A, 17mΩ

FEATURES

- 100% avalanche tested
- Suitable for 5V drive applications
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

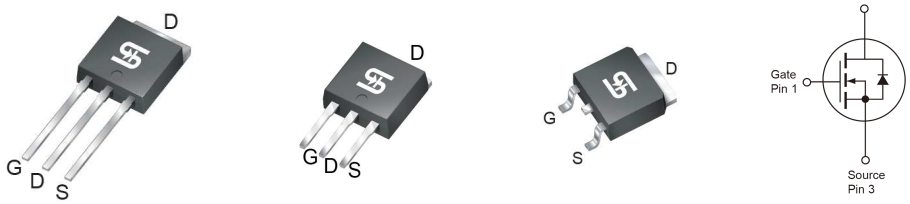
APPLICATION

- SMPS Synchronous Rectification
- Networking DC-DC Power System

KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		60	V
$R_{DS(on)}$ (max)	V_{GS} =10V	17	mΩ
	V_{GS} =4.5V	20	
Q_g		15	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

TO-251 (IPAK) **TO-251S (IPAK SL)** **TO-252 (DPAK)**



Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	38	A
	T_C = 100°C		24	
Pulsed Drain Current (Note 2)		I_{DM}	152	A
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	20	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}	20	A
Total Power Dissipation @ T_C = 25°C		P_{DTOT}	46	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	2.7	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 4)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(TH)}$	1.2	1.7	2.5	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 60V, V_{GS} = 0V	I_{DSS}	--	--	1	μA
	V_{DS} = 48V, V_{GS} = 0V, T_J = 125°C		--	--	10	
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 20A	$R_{DS(ON)}$	--	15	17	mΩ
	V_{GS} = 4.5V, I_D = 10A		--	17.5	20	
Dynamic (Note 5)						
Total Gate Charge	V_{DS} = 30V, I_D = 10A, V_{GS} = 4.5V	Q_g	--	15	--	nC
Gate-Source Charge		Q_{gs}	--	5.5	--	
Gate-Drain Charge		Q_{gd}	--	5	--	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	900	--	pF
Output Capacitance		C_{oss}	--	130	--	
Reverse Transfer Capacitance		C_{rss}	--	90	--	
Gate Resistance	F = 1MHz, open drain	R_g	--	2.2	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 15V, R_G = 6Ω, I_D = 1A	$t_{d(on)}$	--	8.6	--	ns
Turn-On Rise Time		t_r	--	24.2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	32.3	--	
Turn-Off Fall Time		t_f	--	7.9	--	
Source-Drain Diode (Note 4)						
Diode Forward Voltage	V_{GS}=0V, I_S=10A	V_{SD}	--	--	1	V
Reverse Recovery Time	V_{GS} = 0V, I_S = 10A dI$_F$/dt = 100A/μs	t_{rr}	--	18	--	ns
Reverse Recovery Charge		Q_{rr}	--	10	--	nC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. L = 0.1mH, I_{AS} = 20A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM170N06CP ROG	TO-252(D-PAK)	2,500pcs / 13” Reel
TSM170N06CH C5G	TO-251(I-PAK)	75pcs / Tube
TSM170N06CH X0G	TO-251S(I-PAK SL)	75pcs / Tube

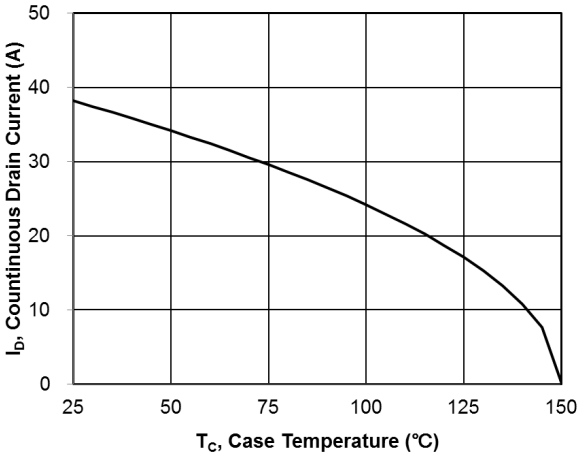
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

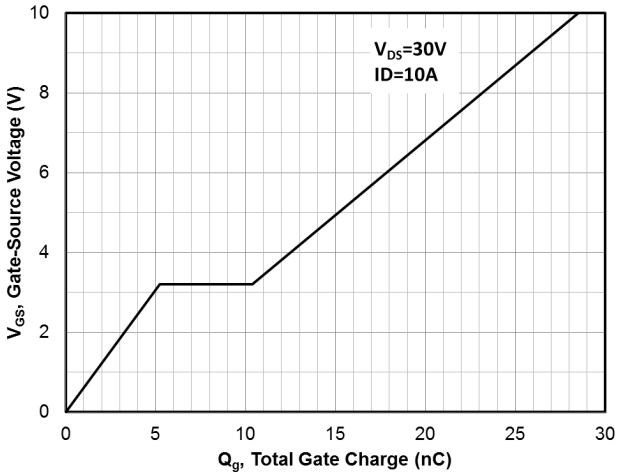
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

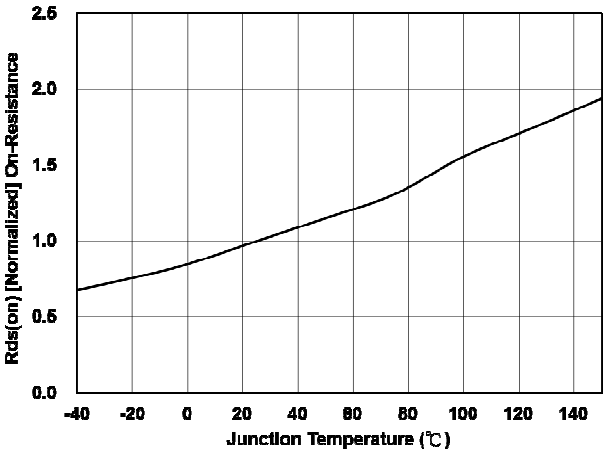
Continuous Drain Current vs. T_C



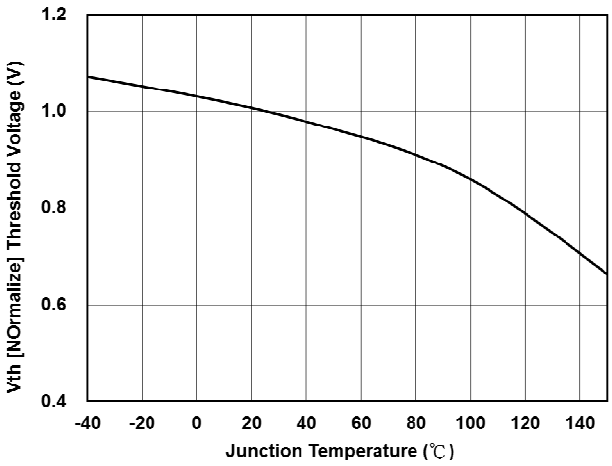
Gate Charge



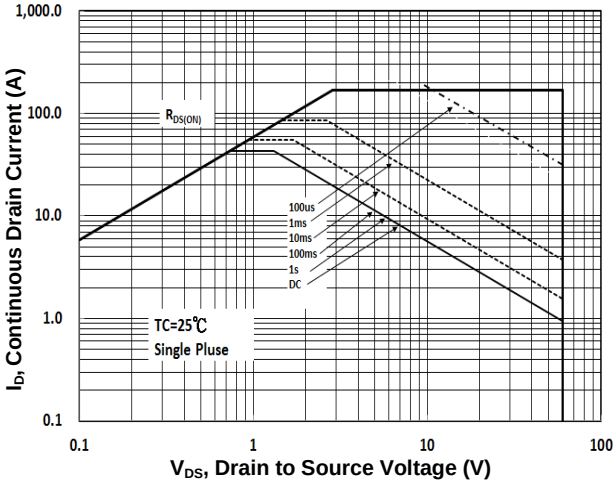
On-Resistance vs. Junction Temperature



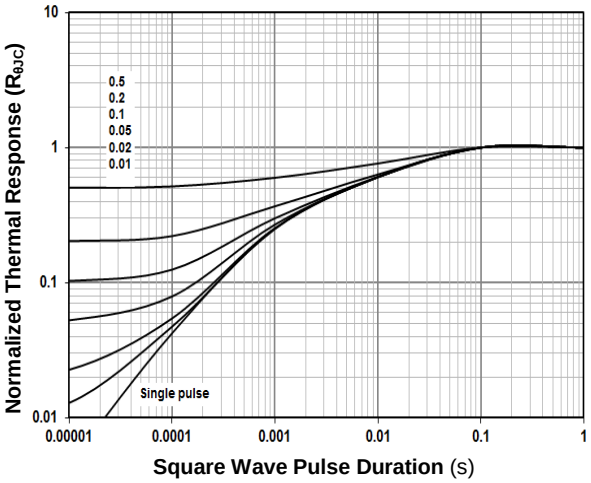
Threshold Voltage vs. Junction Temperature



Maximum Safe Operating Area

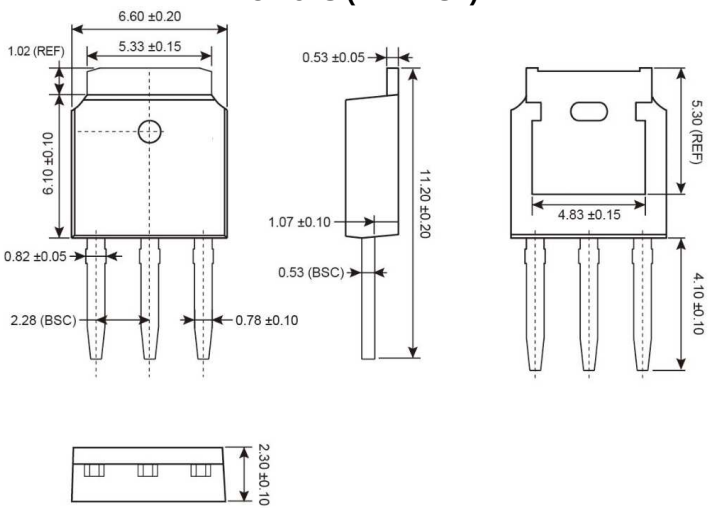


Normalized Thermal Transient Impedance Curve

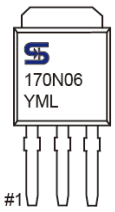


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251S (I-PAK SL)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
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L = Lot Code (1~9, A~Z)

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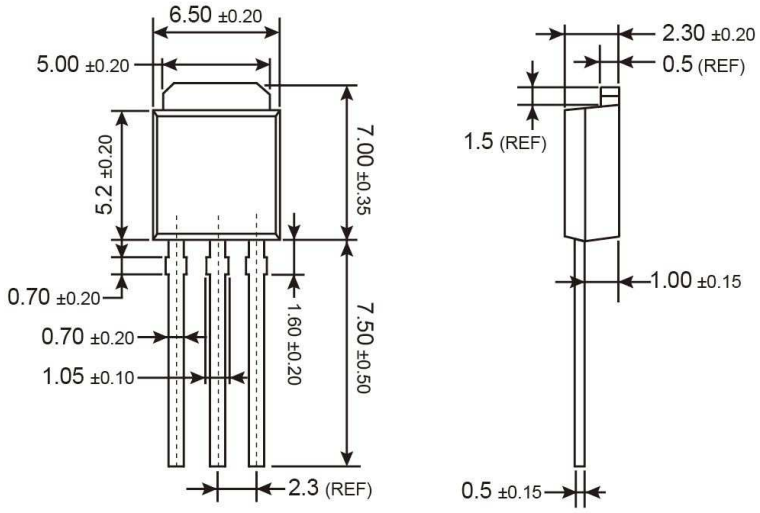
TO-251 (I-PAK)



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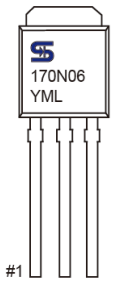

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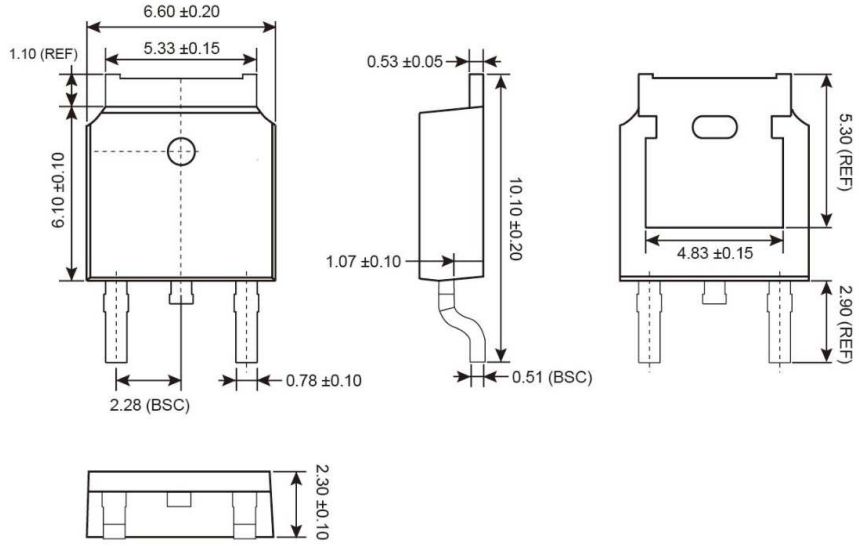
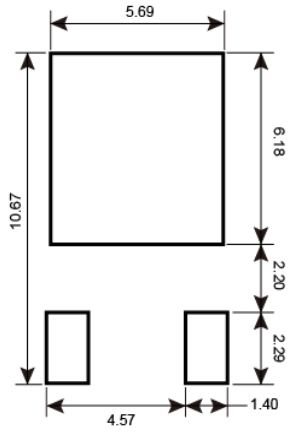
TO-252 (D-PAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



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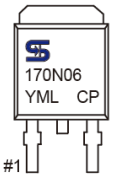

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