

Pin Definition:

1. Gate
2. Source
3. Drain

Key Parameter Performance

Parameter	Value	Unit
V_{DS}	20	V
$R_{DS(on)}$ (max)	$V_{GS} = 4.5V$	65
	$V_{GS} = 2.5V$	95
Q_g	5.4	nC

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

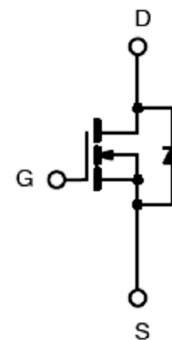
- Load Switch
- PA Switch

Ordering Information

Part No.	Package	Packing
TSM2302CX RF	SOT-23	3kpcs / 7+Reel
TSM2302CX RFG	SOT-23	3kpcs / 7+Reel

Note: %G+denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds

Block Diagram



N-Channel MOSFET

Absolute Maximum Ratings ($T_C = 25^\circ C$, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current	I_D	2.8	A
Pulsed Drain Current ^(Note 1)	I_{DM}	8	A
Continuous Source Current (Diode Conduction) ^(Note 2)	I_S	1.6	A
Maximum Power Dissipation	P_D	$T_a = 25^\circ C$	1.25
		$T_a = 75^\circ C$	0.8
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Thermal Performance

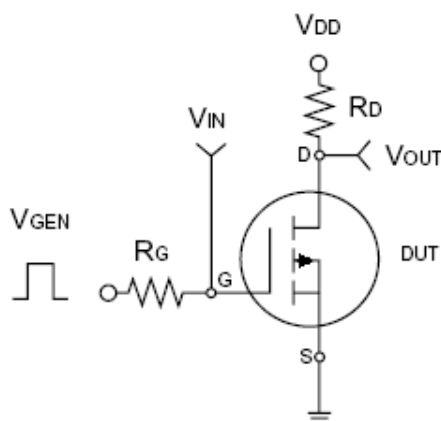
Parameter	Symbol	Limit	Unit
Thermal Resistance Junction to Foot	R_{JF}	75	$^\circ C/W$
Thermal Resistance Junction to Ambient	R_{JA}	145	$^\circ C/W$

Electrical Specifications

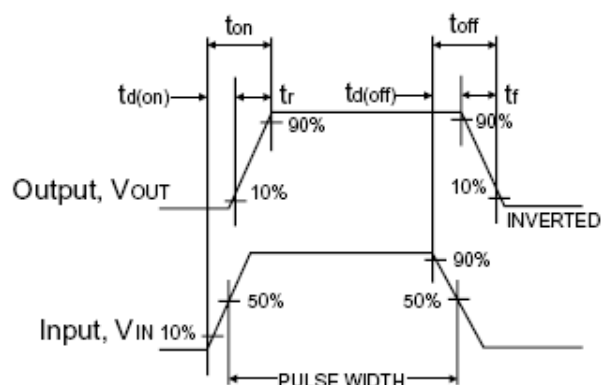
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static ^(Note 3)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	0.65	0.95	1.2	V
Gate Body Leakage	$V_{GS} = \pm 8V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 16V, V_{GS} = 0V$	I_{DSS}	--	--	1.0	μA
On-State Drain Current	$V_{DS} = 5V, V_{GS} = 4.5V$	$I_{D(ON)}$	6	--	--	A
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 2.8A$	$R_{DS(ON)}$	--	40	65	m
	$V_{GS} = 2.5V, I_D = 2.0A$		--	50	95	
Forward Transconductance	$V_{DS} = 5V, I_D = 2.8A$	g_{fs}	--	10	--	S
Diode Forward Voltage	$I_S = 1.6A, V_{GS} = 0V$	V_{SD}	--	0.76	1.2	V
Dynamic ^(Note 4)						
Total Gate Charge	$V_{DS} = 10V, I_D = 2.8A, V_{GS} = 4.5V$	Q_g	--	5.4	10	nC
Gate-Source Charge		Q_{gs}	--	0.65	--	
Gate-Drain Charge		Q_{gd}	--	1.4	--	
Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz$	C_{iss}	--	340	--	pF
Output Capacitance		C_{oss}	--	115	--	
Reverse Transfer Capacitance		C_{rss}	--	33	--	
Switching ^(Note 5)						
Turn-On Delay Time	$V_{DD} = 6V, R_L = 10\ \Omega, I_D = 1A, V_{GEN} = 4.5V, R_G = 6\ \Omega$	$t_{d(on)}$	--	12	25	ns
Turn-On Rise Time		t_r	--	36	60	
Turn-Off Delay Time		$t_{d(off)}$	--	34	60	
Turn-Off Fall Time		t_f	--	10	25	

Notes:

1. Pulse width limited by the maximum junction temperature
2. Surface Mounted on FR4 Board t m5 sec.
3. Pulse test: PW m300 μs , duty cycle m2%
4. For DESIGN AID ONLY, not subject to production testing.
5. Switching time is essentially independent of operating temperature.



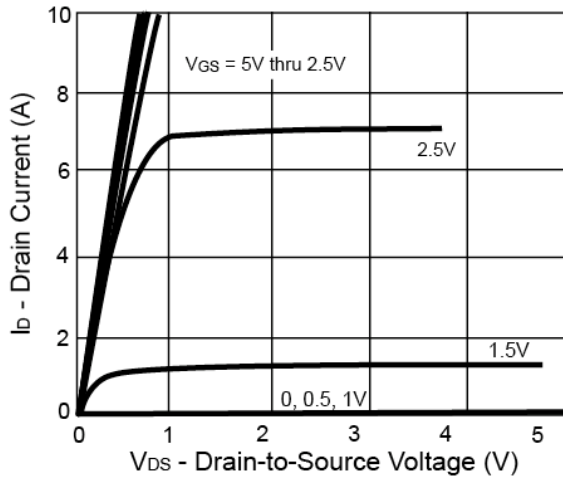
Switching Test Circuit



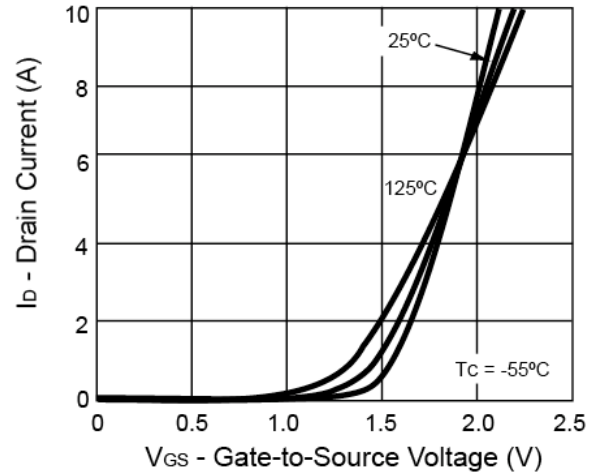
Switchin Waveforms

Electrical Characteristics Curve

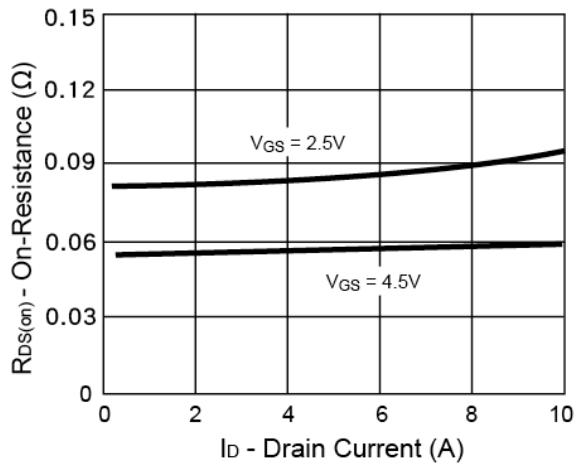
Output Characteristics



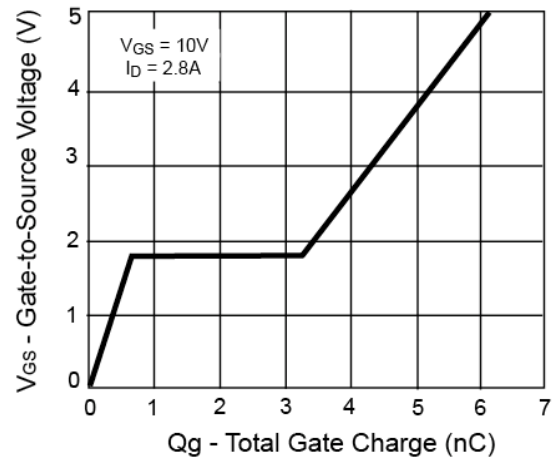
Transfer Characteristics



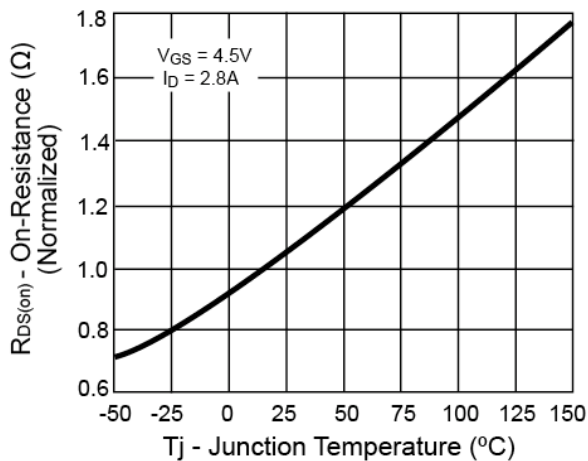
On-Resistance vs. Drain Current



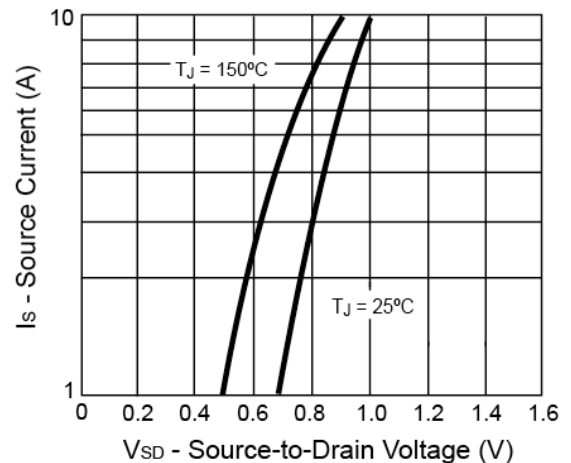
Gate Charge



On-Resistance vs. Junction Temperature

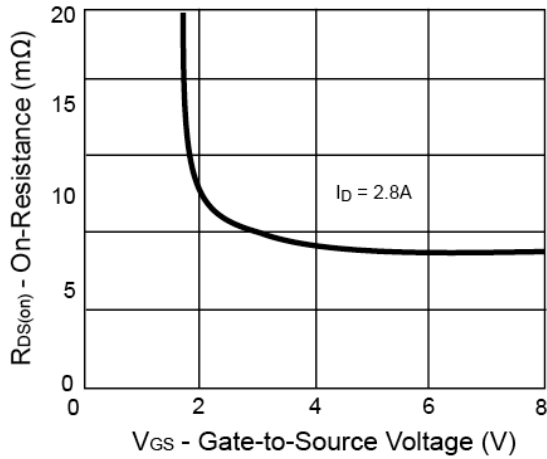


Source-Drain Diode Forward Voltage

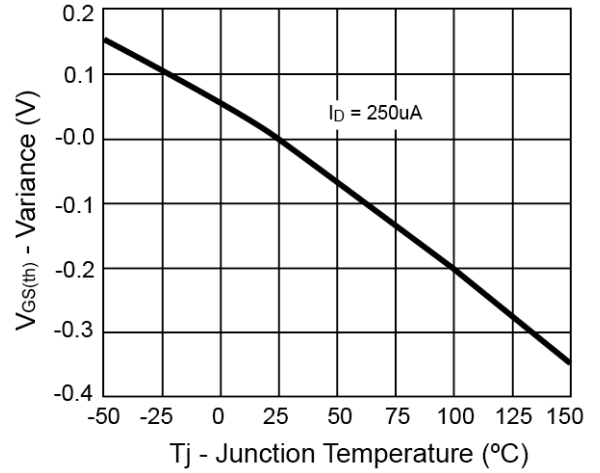


Electrical Characteristics Curve

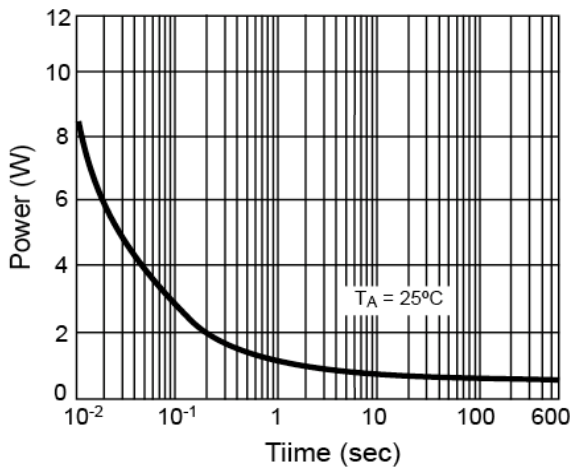
On-Resistance vs. Gate-Source Voltage



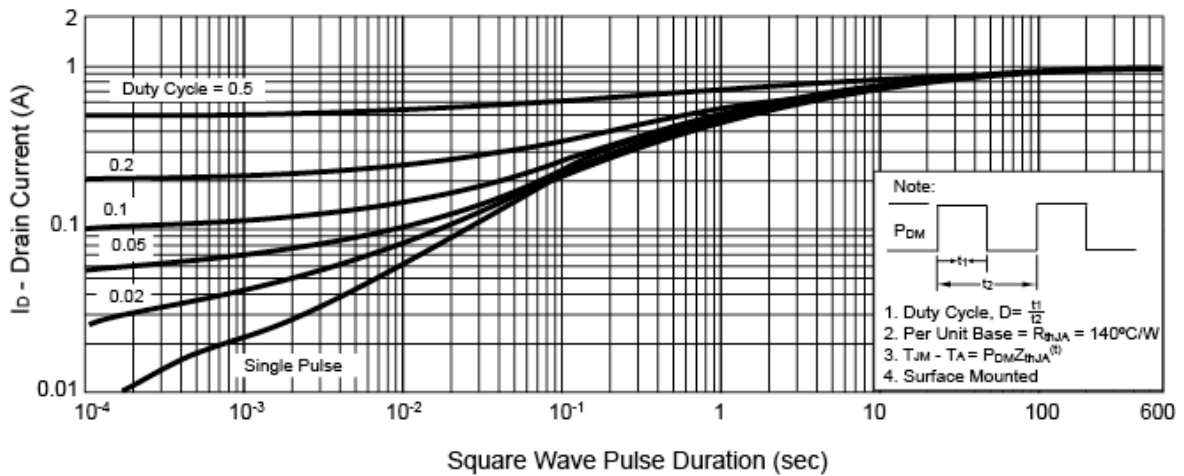
Threshold Voltage



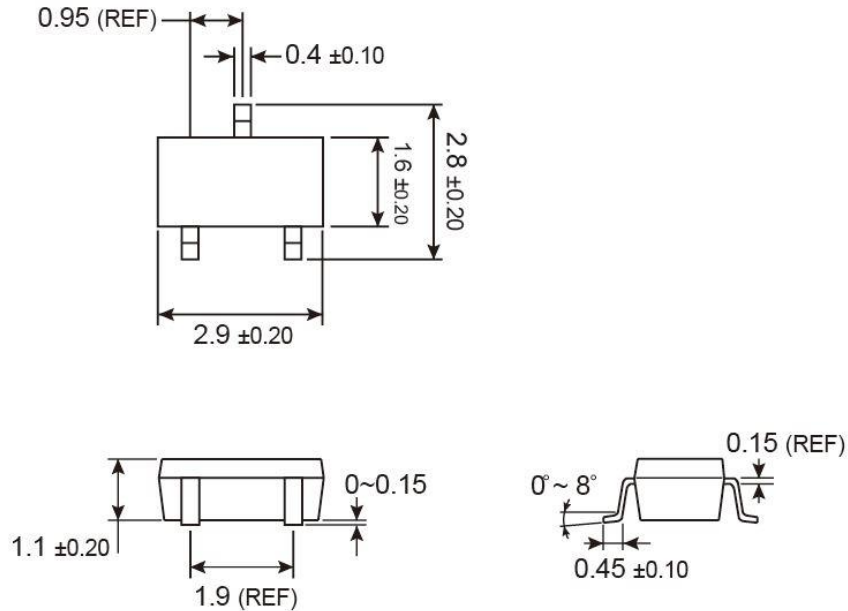
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

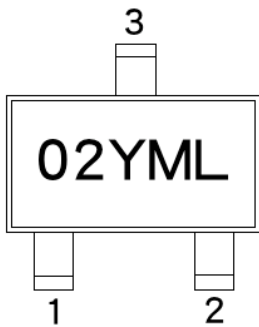


SOT-23 Mechanical Drawing



Unit: Millimeters

Marking Diagram



- 02** = Device Code
- Y** = Year Code
- M** = Month Code
 - (**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apr, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
 - = Month Code for Halogen Free Product
 - (**O**=Jan, **P**=Feb, **Q**=Mar, **R**=Apr, **S**=May, **T**=Jun, **U**=Jul, **V**=Aug, **W**=Sep, **X**=Oct, **Y**=Nov, **Z**=Dec)
- L** = Lot Code

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