TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM2N7002KD

60V N-Channel MOSFET

SOT-363

Pin Definition:

1. Source 2
2. Gate 2
3. Drain 1
6. Drain 2
5. Gate 1
4. Source 1

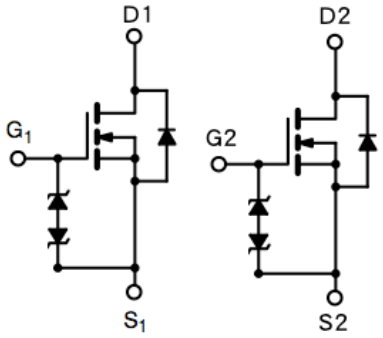
PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(Ω)	I_D (mA)
60	2 @ V_{GS} = 10V	300
	4 @ V_{GS} = 4.5V	200

Features

- Low On-Resistance
- ESD Protection
- High Speed Switching
- Low Voltage Drive

Block Diagram



Dual N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM2N7002KDCU6 RF	SOT-363	3Kpcs / 7” Reel

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous @ T_A=25°C	I_D	300	mA
	Pulsed	I_{DM}	800	
Drain Reverse Current	Continuous @ T_A=25°C	I_{DR}	300	mA
	Pulsed	I_{DMR}	800	
Maximum Power Dissipation		P_D	300	mW
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8” from case)	T_L	5	S
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	625	°C/W

Notes:

a. Pulse width ≤300us, Duty cycle ≤2%

b. When the device is mounted on a glass epoxy board with area measuring 1 x 0.75 x 0.62 inch.

c. The power dissipation of the package may result in a continuous drain current.

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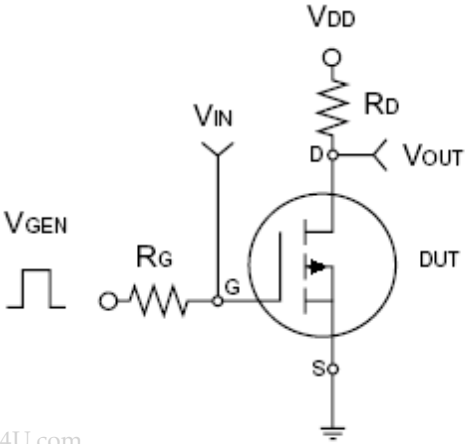
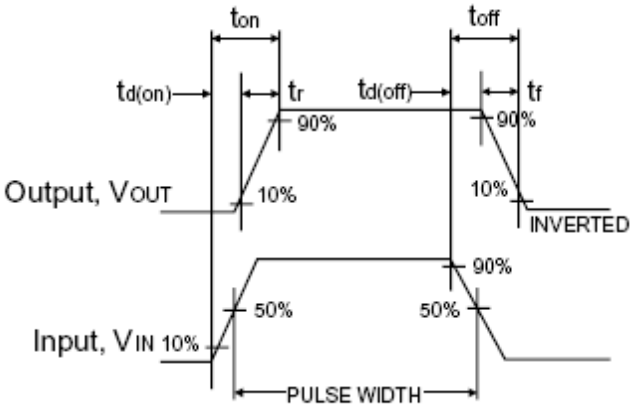
Electrical Specifications (Ta = 25°C, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =250μA	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	V_{DS} =V_{GS}, I_D =250μA	$V_{GS(TH)}$	1.0	1.5	2.5	V
Gate Body Leakage	V_{GS} =±20V, V_{DS} =0V	I_{GSS}	--	--	±10	uA
Zero Gate Voltage Drain Current	V_{DS} =60V, V_{GS} =0V	I_{DSS}	--	--	1.0	uA
Drain-Source On-State Resistance	V_{GS} =10V, I_D =300mA	$R_{DS(ON)}$	--	1.2	2	Ω
	V_{GS} =4.5V, I_D =100mA		--	2	4	
Forward Transconductance	V_{DS} =10V, I_D =200mA	g_{fs}	100	--	--	mS
Diode Forward Voltage	I_S =300mA, V_{GS} =0V	V_{SD}	--	0.8	1.4	V
Dynamic[b]						
Total Gate Charge	V_{DS} =10V, I_D = 250mA, V_{GS} =4.5V	Q_g	--	0.4	0.6	nC
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	30	--	pF
Output Capacitance		C_{oss}	--	6	--	
Reverse Transfer Capacitance		C_{rss}	--	2.5	--	
Switching[c]						
Turn-On Delay Time	V_{DD} =30V, R_G =10Ω	$t_{d(on)}$	--	--	25	nS
Turn-Off Delay Time	I_D =200mA, V_{GEN} =10V,	$t_{d(off)}$	--	--	35	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



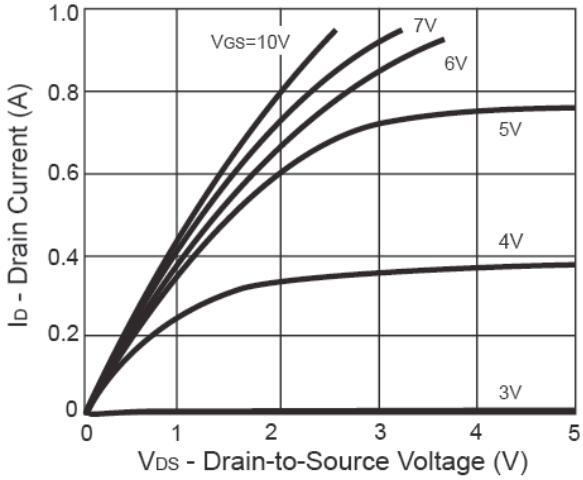
Switching Test Circuit



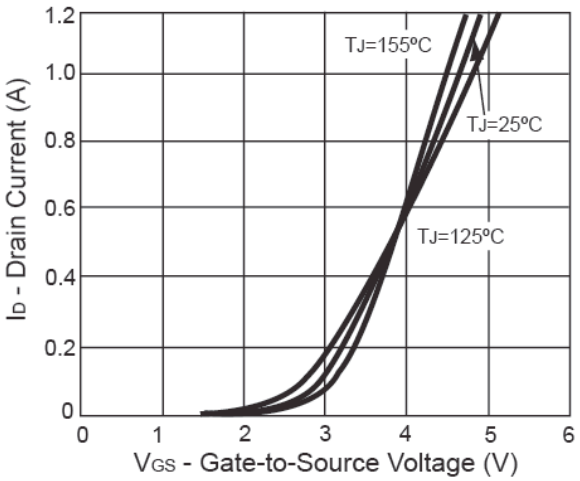
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

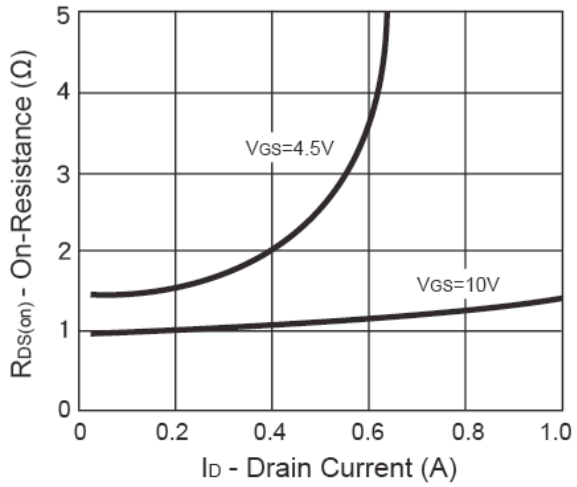
Output Characteristics



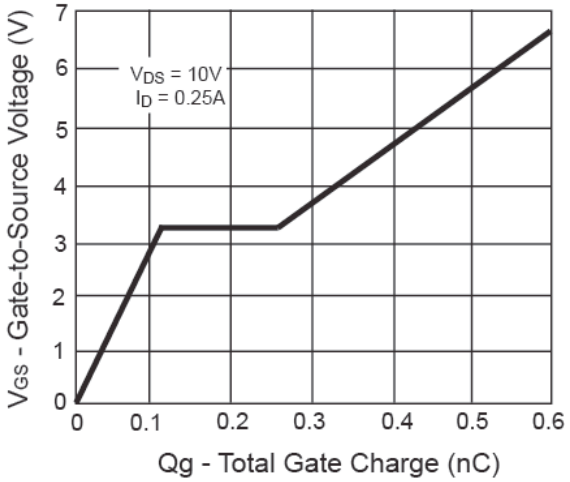
Transfer Characteristics



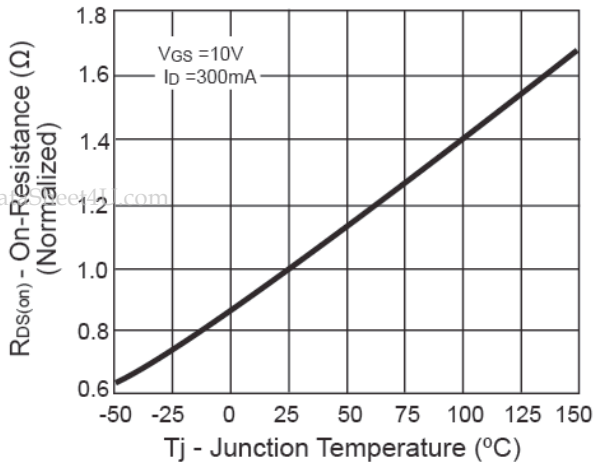
On-Resistance vs. Drain Current



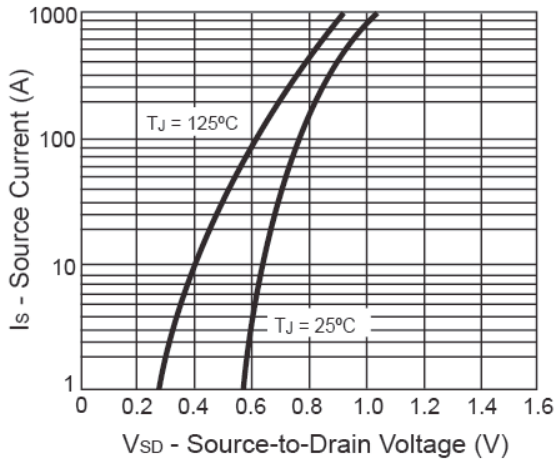
Gate Charge



On-Resistance vs. Junction Temperature

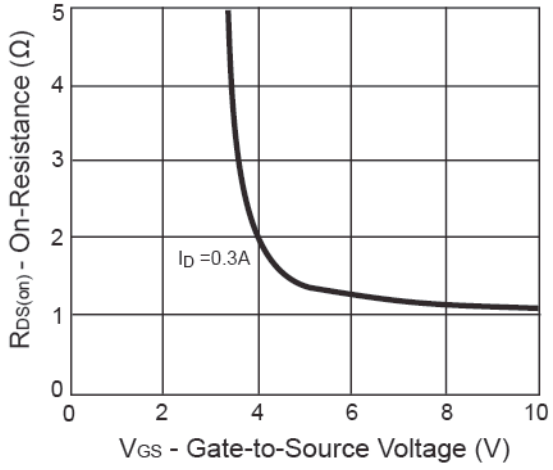


Source-Drain Diode Forward Voltage

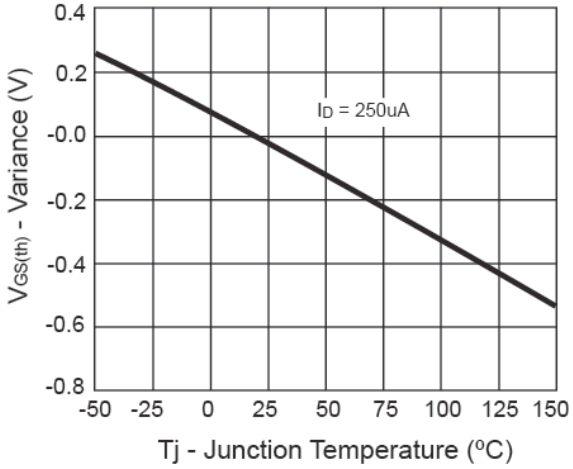


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

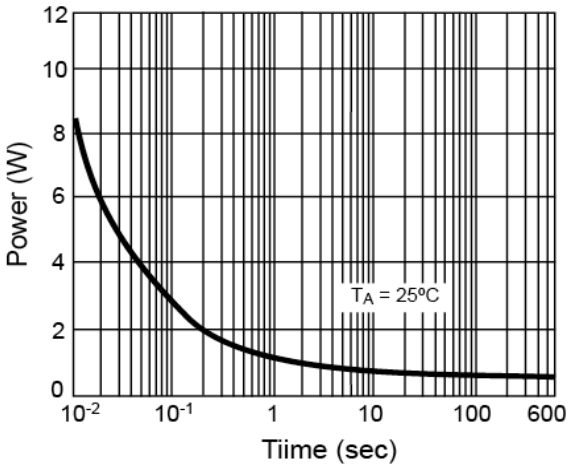
On-Resistance vs. Gate-Source Voltage



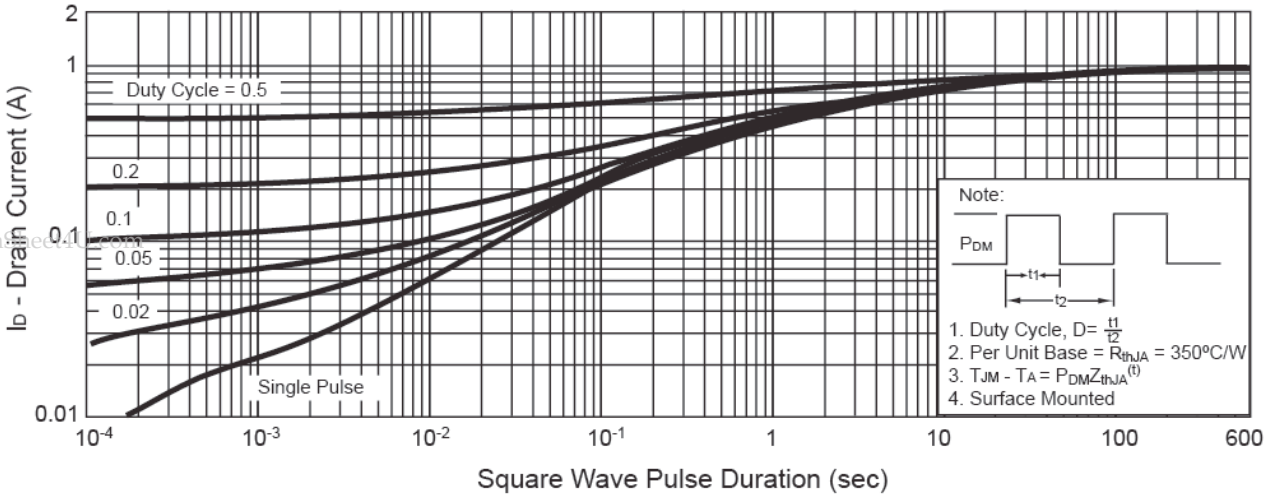
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



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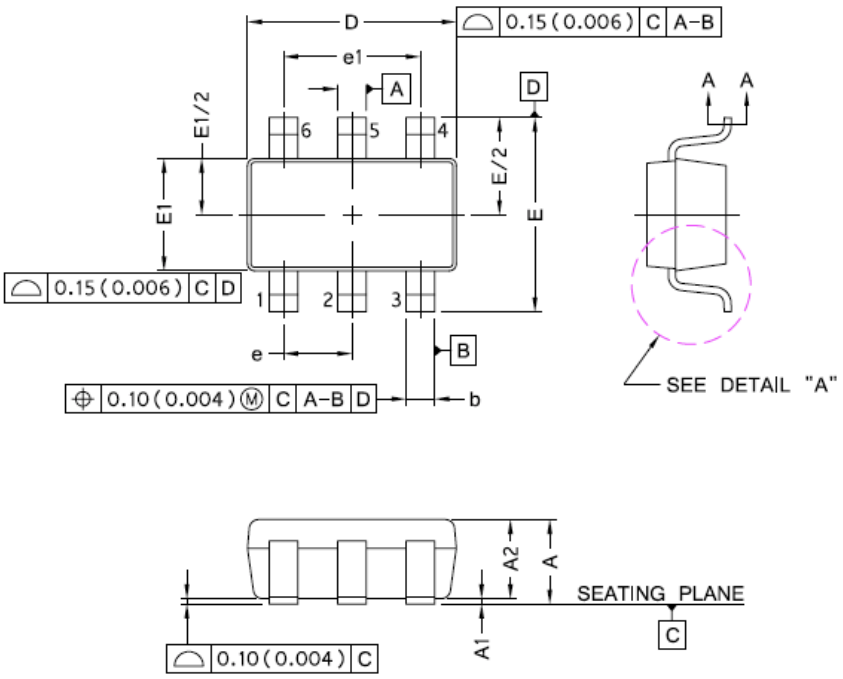
SOT-363 Mechanical Drawing



SOT-363 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	0.80	1.10	0.031	0.043
A1	0	0.10	0	0.004
A2	0.80	1.00	0.031	0.040
b	0.15	0.30	0.006	0.012
b1	0.15	0.25	0.006	0.010
c	0.08	0.22	0.003	0.009
c1	0.08	0.20	0.003	0.008
D	1.90	2.10	0.074	0.084
E	2.00	2.20	0.078	0.086
E1	1.15	1.35	0.045	0.055
e	0.65 BSC		0.025 BSC	
e1	1.30 BSC		0.051 BSC	
L	0.26	0.46	0.010	0.018
θ	0°	8°	0°	8°
θ1	4°	10°	4°	10°

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