

N-Channel Power MOSFET

800V, 3A, 4.2Ω

FEATURES

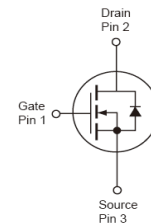
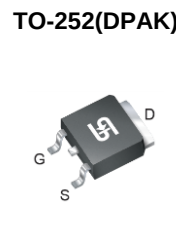
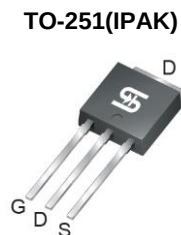
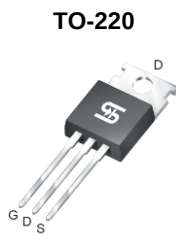
- Low $R_{DS(ON)}$ 3.3Ω (Typ.)
- Low gate charge typical @ 19nC (Typ.)
- Low C_{rss} typical @ 10.2pF (Typ.)
- Improved dv/dt capability

APPLICATION

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	800	V
$R_{DS(on)}$ (max)	4.2	Ω
Q_g	19	nC



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT			UNIT
			IPAK/DPAK	ITO-220	TO-220	
Drain-Source Voltage		V _{DS}	800			V
Gate-Source Voltage		V _{GS}	±30			V
Continuous Drain Current ^(Note 1)	T _C = 25°C	I _D	3			A
	T _C = 100°C		1.83			
Pulsed Drain Current ^(Note 2)		I _{DM}	12			A
Single Pulsed Avalanche Energy ^(Note 3)		E _{AS}	48			mJ
Single Pulsed Avalanche Current ^(Note 3)		I _{AS}	3			A
Repetitive Avalanche Energy ^(Note 3)		E _{AR}	9.4			mJ
Repetitive Avalanche Energy ^(Note 4)		dV/dt	4.5			V/ns
Total Power Dissipation @ T _C = 25°C		P _{DTOT}	94	32	94	W
Operating Junction and Storage Temperature Range		T _J , T _{STG}	- 55 to +150			°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT			UNIT
		IPAK/DPAK	ITO-220	TO-220	
Junction to Case Thermal Resistance	$R_{\theta Jc}$	1.33	3.9	1.33	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	110	62.5		°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 5)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	800	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2	--	4	V
Gate Body Leakage	V _{GS} = ±30V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 800V, V _{GS} = 0V	I _{DSS}	--	--	10	μA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 1.5A	R _{DS(ON)}	--	3.3	4.2	Ω
Forward Transfer Conductance	V _{DS} = 30V, I _D = 1.5A	g _{fs}	--	3.7	--	S
Dynamic ^(Note 6)						
Total Gate Charge	V _{DS} = 640V, I _D = 3A, V _{GS} = 10V	Q _g	--	19	--	nC
Gate-Source Charge		Q _{gs}	--	4	--	
Gate-Drain Charge		Q _{gd}	--	7.6	--	
Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	696	--	pF
Output Capacitance		C _{oss}	--	65	--	
Reverse Transfer Capacitance		C _{rss}	--	10.2	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	3.2	--	Ω
Switching ^(Note 7)						
Turn-On Delay Time	V _{GS} = 10V, I _D = 3A, V _{DD} = 400V, R _G =25Ω	t _{d(on)}	--	48	--	ns
Turn-On Rise Time		t _r	--	36	--	
Turn-Off Delay Time		t _{d(off)}	--	106	--	
Turn-Off Fall Time		t _f	--	41	--	
Source-Drain Diode ^(Note 5)						
Source Current	Integral reverse diode in the MOSFET	I _S	--	--	3	A
Source Current (Pulse)		I _{SM}	--	--	12	A
Diode Forward Voltage	I _S = 3A, V _{GS} = 0V	V _{SD}	--	--	1.5	V
Reverse Recovery Time	V _{GS} = 0V, I _S =3A,	t _{rr}	--	370	--	ns
Reverse Recovery Charge	dI _F /dt = 100A/us	Q _{rr}	--	1.8	--	μC

Notes:

- Current limited by package
- Pulse width limited by the maximum junction temperature
- $L = 10mH, I_{AS} = 3A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- $I_{SD} \leq 3A, dI/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
- Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM3N80CZ C0G	TO-220	50pcs / Tube
TSM3N80CI C0G	ITO-220	50pcs / Tube
TSM3N80CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM3N80CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

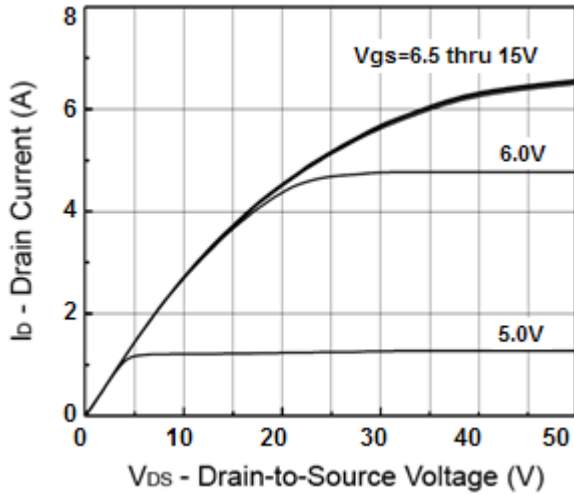
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

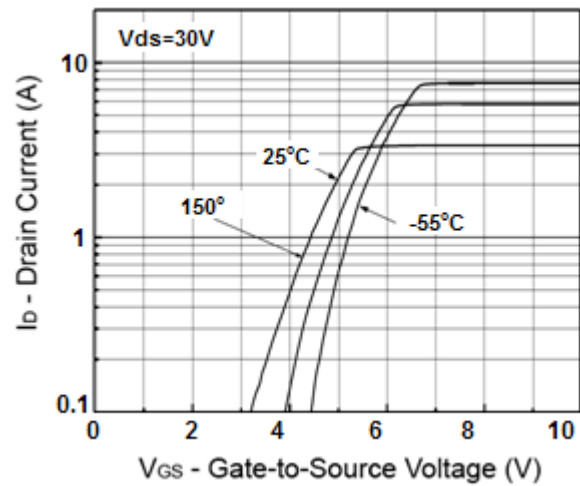
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

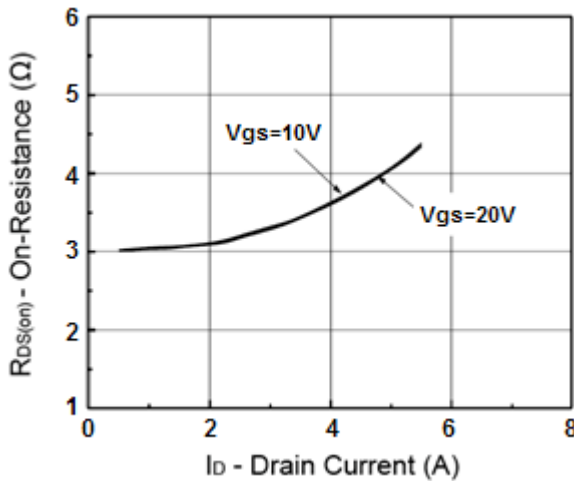
Output Characteristics



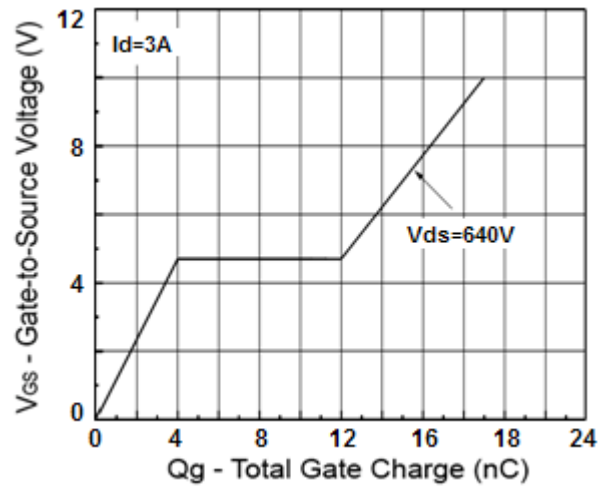
Transfer Characteristics



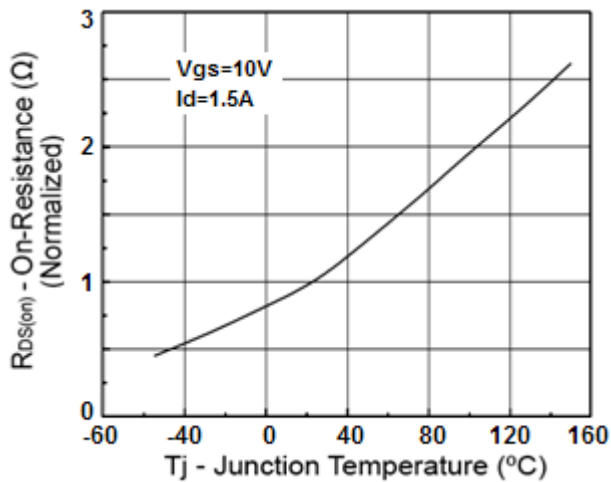
On-Resistance vs. Drain Current



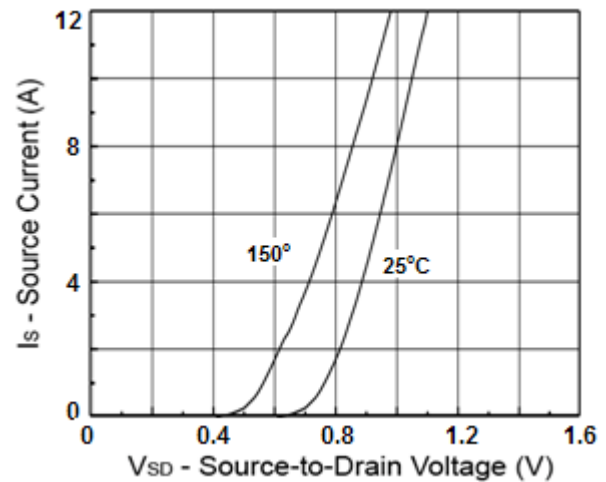
Gate Charge



On-Resistance vs. Junction Temperature



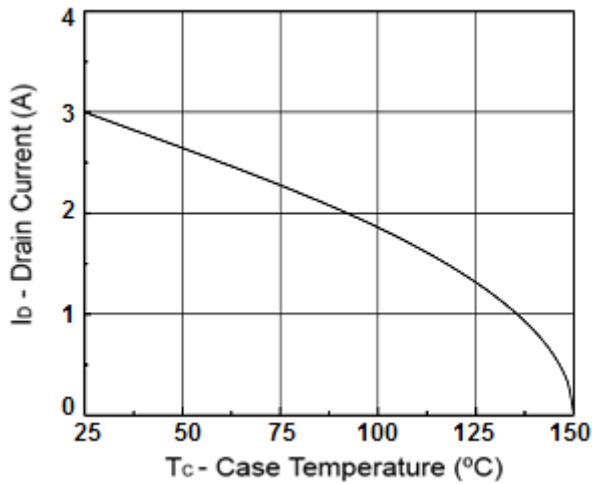
Source-Drain Diode Forward Voltage



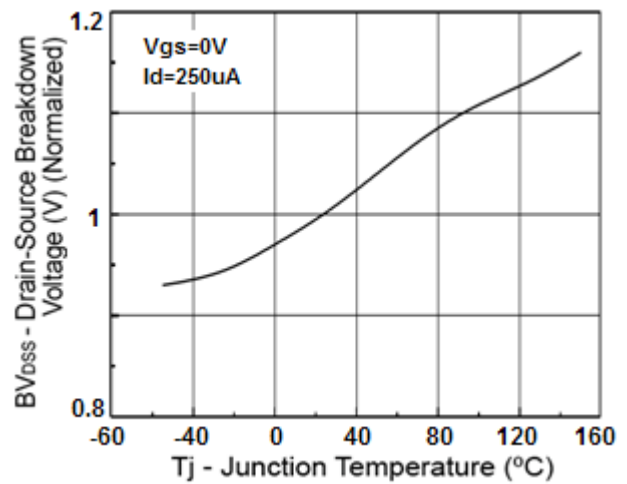
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

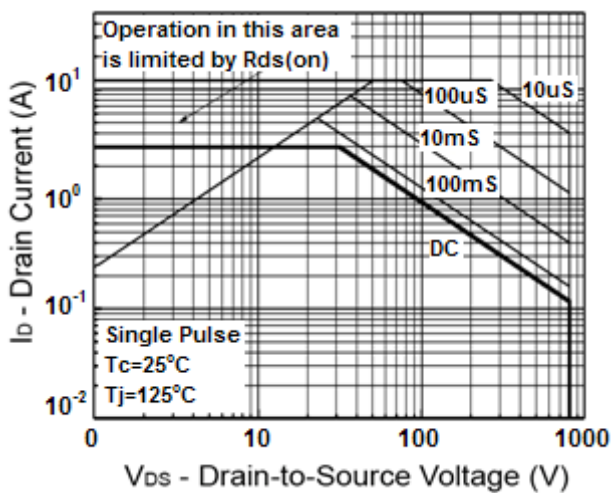
Drain Current vs. Case Temperature



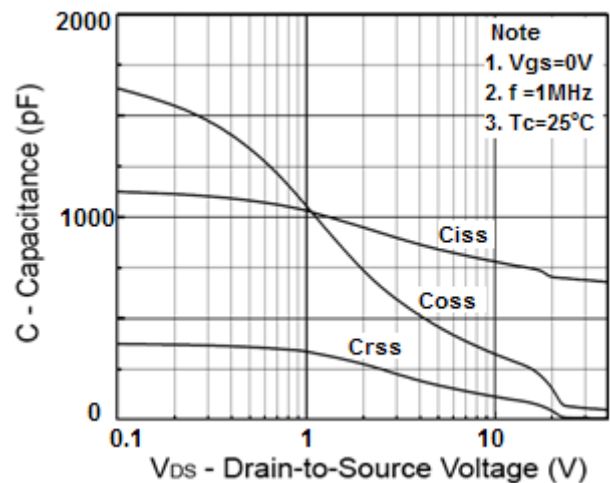
BV_{DSS} vs. Junction Temperature



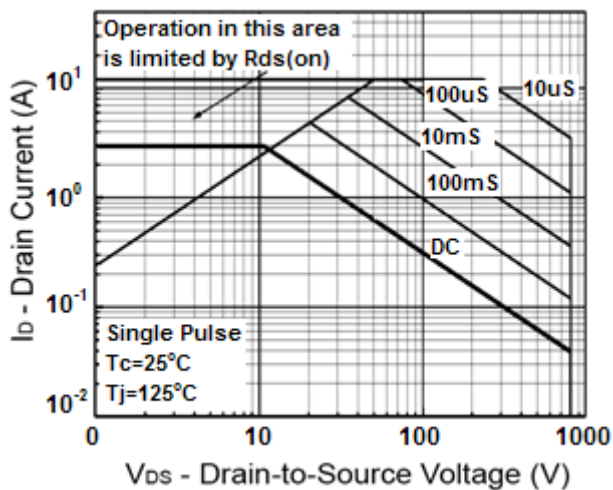
Maximum Safe Operating Area(TO-220, I/D-PAK)



Capacitance vs. Drain-Source Voltage



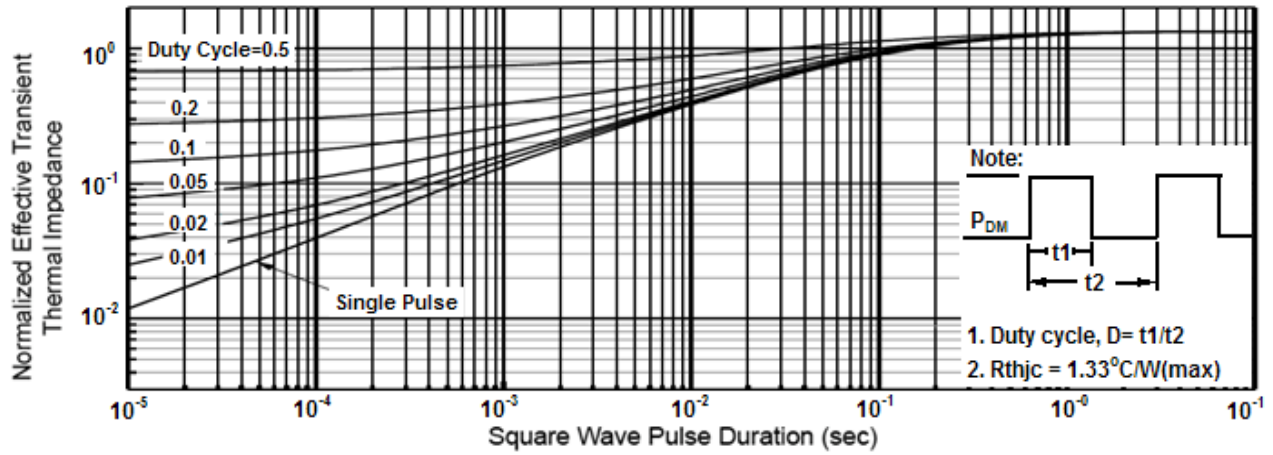
Maximum Safe Operating Area(ITO-220)



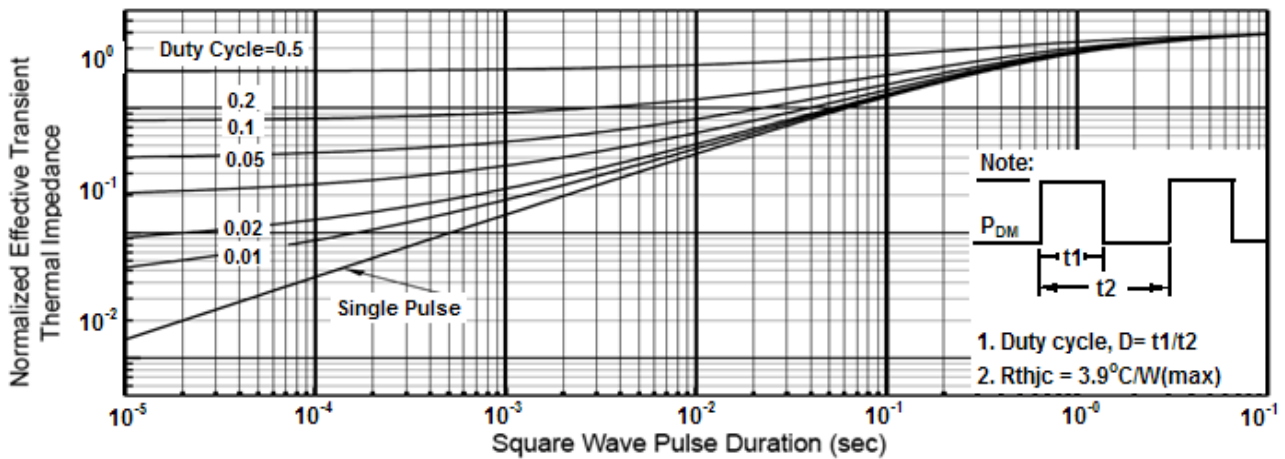
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient (TO-220, I/D-PAK)

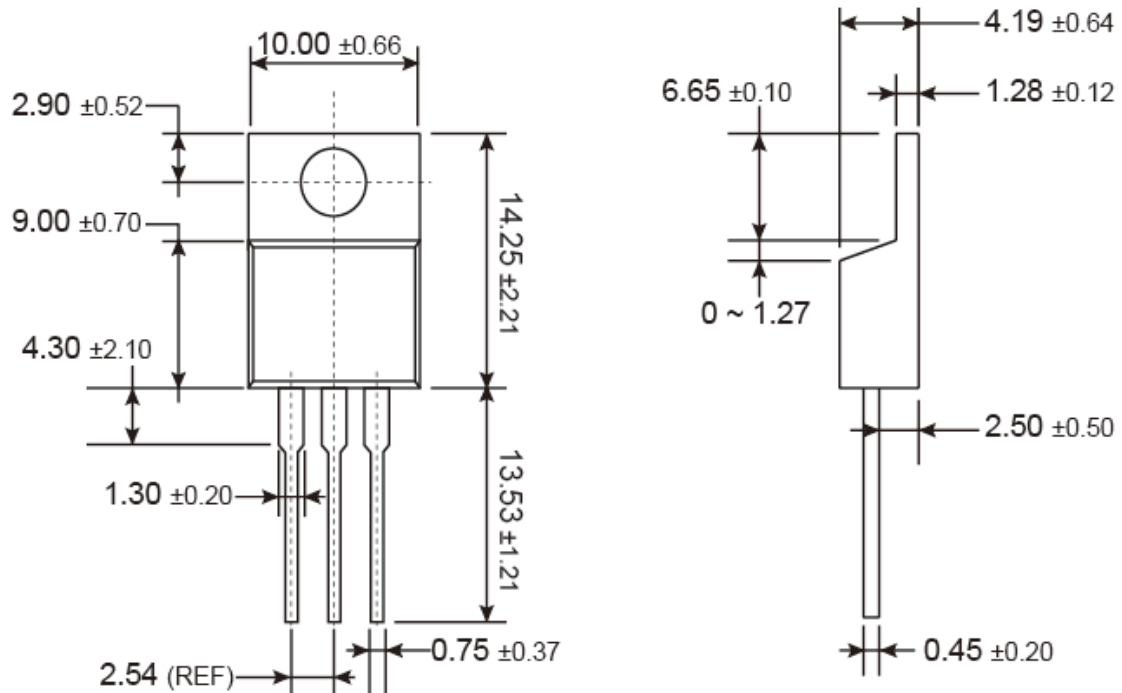


Normalized Thermal Transient Impedance, Junction-to-Ambient (ITO-220)

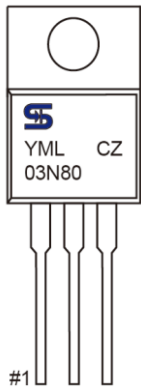


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-220



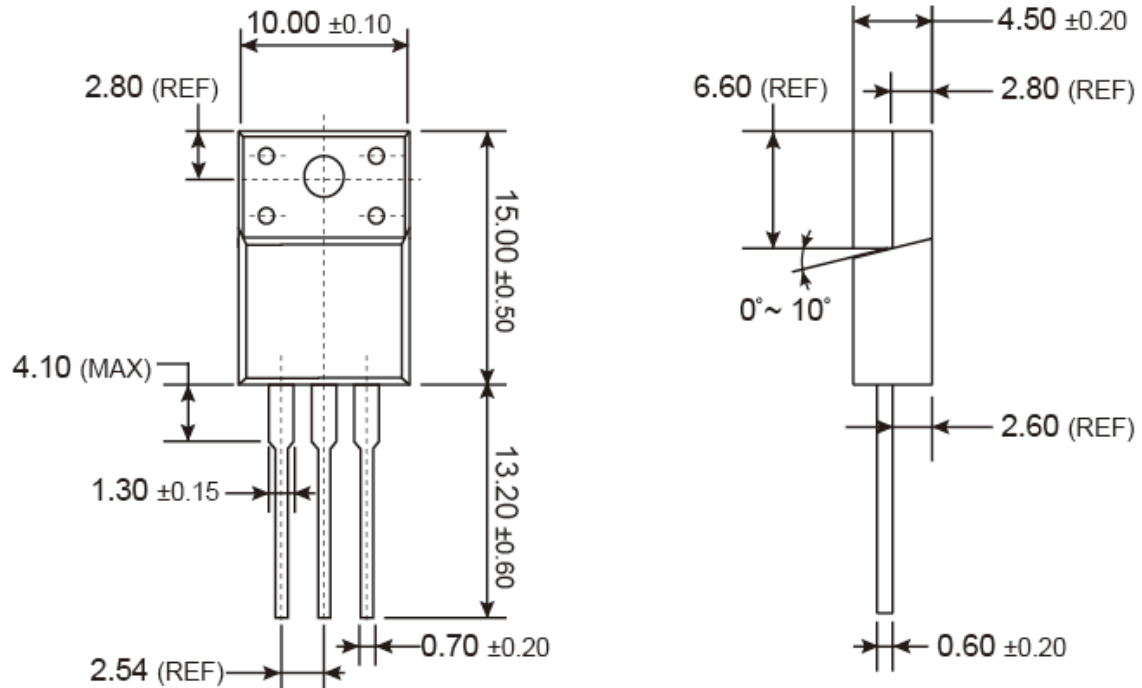
MARKING DIAGRAM



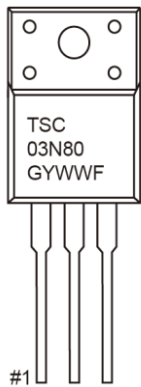
Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
W =Sep **X** =Oct **Y** =Nov **Z** =Dec
L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

ITO-220



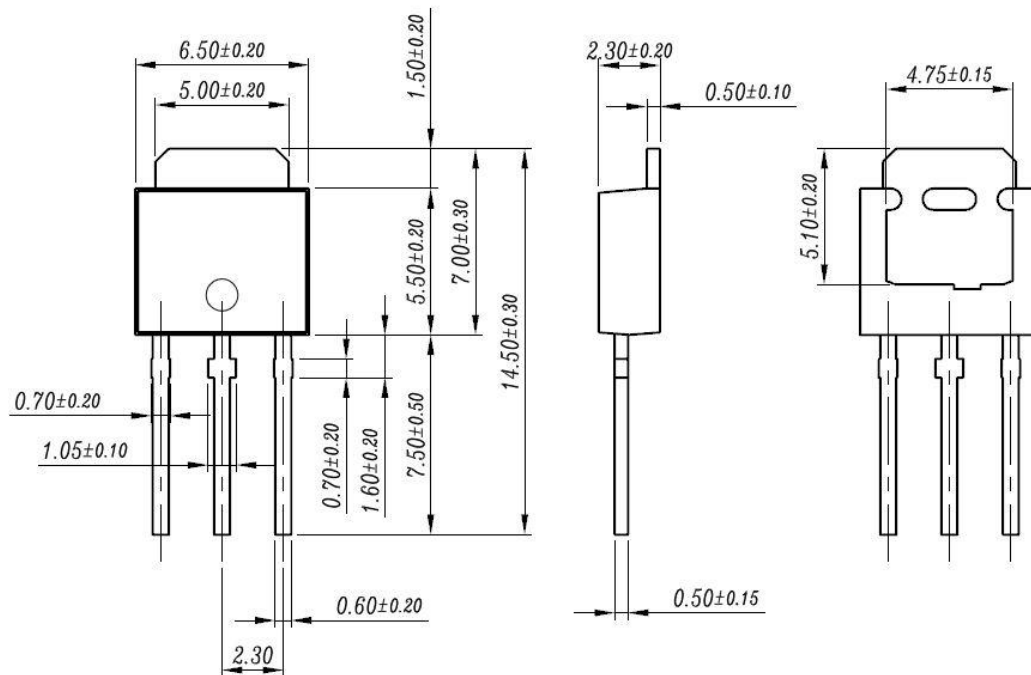
MARKING DIAGRAM



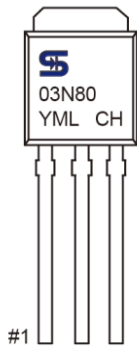
- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251(IPAK)



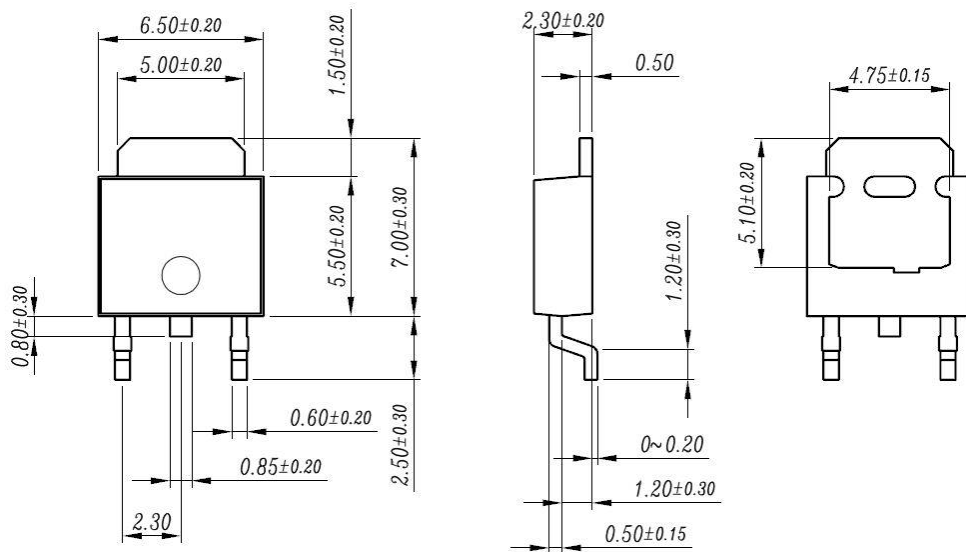
MARKING DIAGRAM



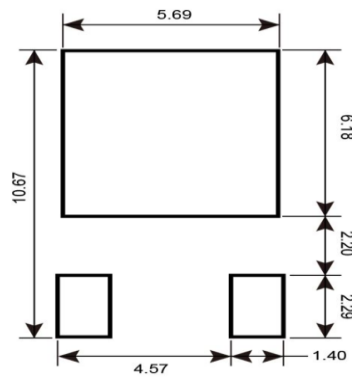
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PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

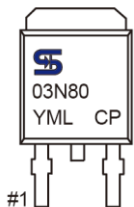
TO-252(DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



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