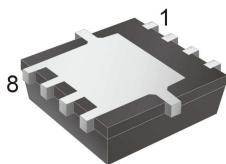


**PDFN33**



**Pin Definition:**

- |           |          |
|-----------|----------|
| 1. Source | 8. Drain |
| 2. Source | 7. Drain |
| 3. Source | 6. Drain |
| 4. Gate   | 5. Drain |

# TSM40N03PQ33

## 30V N-Channel Power MOSFET

**PRODUCT SUMMARY**

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
30	4.6 @ $V_{GS}=10V$	19
	5.9 @ $V_{GS}=4.5V$	16

**Features**

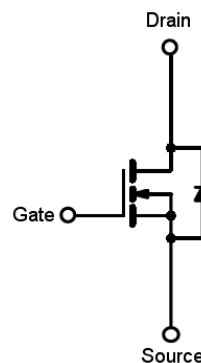
- Advanced Trench Technology
- Low On-Resistance
- Low gate charge typical @ 12nC (Typ.)
- Low Crss typical @ 140pF (Typ.)

**Ordering Information**

Part No.	Package	Packing
TSM40N03PQ33 RGG	PDFN33	5Kpcs / 13" Reel

**Note:** "G" denote for Halogen Free Product

**Block Diagram**



N-Channel MOSFET

**Absolute Maximum Rating** ( $T_a = 25^\circ C$  unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	40
		$T_C=70^\circ C$	40
		$T_A=25^\circ C$	25
		$T_A=70^\circ C$	20
Drain Current-Pulsed Note 1	$I_{DM}$	100	A
Avalanche Current, L=0.5mH	$I_{AS}, I_{AR}$	38	A
Avalanche Energy, L=0.5mH	$E_{AS}, E_{AR}$	72	mJ
Maximum Power Dissipation	$P_D$	$T_C=25^\circ C$	52
		$T_C=70^\circ C$	33
		$T_A=25^\circ C$	3.8
		$T_A=70^\circ C$	2.4
Storage Temperature Range	$T_{STG}$	-55 to +150	$^\circ C$
Operating Junction Temperature Range	$T_J$	-55 to +150	$^\circ C$

\* Limited by maximum junction temperature

**Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R\theta_{JC}$	2.4	$^\circ C/W$
Thermal Resistance - Junction to Ambient	$R\theta_{JA}$	33	$^\circ C/W$

Notes: Surface mounted on FR4 board  $t \leq 10sec$

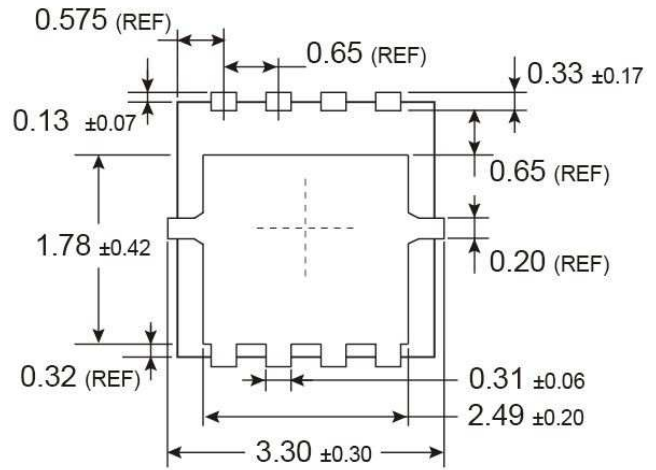
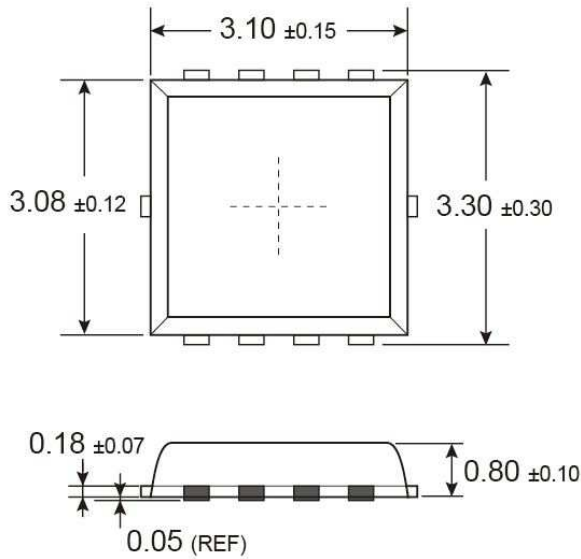
### Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	30	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 19A$	$R_{DS(ON)}$	--	3.6	4.6	mΩ
	$V_{GS} = 4.5V, I_D = 16A$		--	4.8	5.9	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.15	--	2.2	V
Zero Gate Voltage Drain Current	$V_{DS} = 30V, V_{GS} = 0V$	$I_{DSS}$	--	--	1	μA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	±100	nA
<b>Dynamic</b>						
Total Gate Charge	$V_{DS} = 15V, I_D = 19A,$ $V_{GS} = 4.5V$	$Q_g$	--	12	--	nC
Gate-Source Charge		$Q_{gs}$	--	5.4	--	
Gate-Drain Charge		$Q_{gd}$	--	4.6	--	
Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0MHz$	$C_{iss}$	--	1700	--	pF
Output Capacitance		$C_{oss}$	--	350	--	
Reverse Transfer Capacitance		$C_{rss}$	--	140	--	
<b>Switching</b>						
Turn-On Delay Time	$V_{GS} = 4.5V, V_{DS} = 15V,$ $R_G = 1\Omega$	$t_{d(on)}$	--	25	--	nS
Turn-On Rise Time		$t_r$	--	20	--	
Turn-Off Delay Time		$t_{d(off)}$	--	25	--	
Turn-Off Fall Time		$t_f$	--	15	--	
<b>Drain-Source Diode Characteristics and Maximum Rating</b>						
Drain-Source Diode Forward Voltage	$V_{GS}=0V, I_S=10A$	$V_{SD}$	--	0.8	1.2	V
Reverse Recovery Time	$I_S = 10A, T_J=25^\circ C$ $di/dt = 100A/\mu s$	$t_{fr}$	--	25	--	nS
Reverse Recovery Charge		$Q_{fr}$	--	17	--	nC

Notes:

1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
2.  $R\theta_{JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R\theta_{JC}$  is guaranteed by design while  $R\theta_{CA}$  is determined by the user's board design.  $R\theta_{JA}$  shown below for single device operation on FR-4 in still air
3. The maximum current rating is limited by package.

**PDFN33 Mechanical Drawing**



Unit: Millimeters

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