TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM4404

30V N-Channel MOSFET

SOP-8

Pin Definition:
1. Source
2. Source
3. Source
4. Gate
5, 6, 7, 8. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
30	30 @ V_{GS} = 10V	8.5
	33 @ V_{GS} = 4.5V	8.5
	48 @ V_{GS} = 2.5V	5

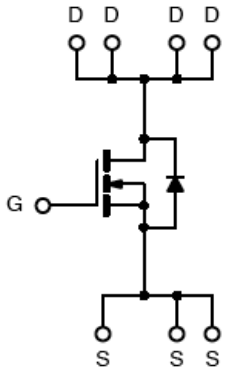
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- High-Side DC/DC Conversion
- Notebook
- Sever

Block Diagram



N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM4404CS RL	SOP-8	2.5Kpcs / 13” Reel

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current		I_D	8.5	A
Pulsed Drain Current		I_{DM}	60	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	4.3	A
Maximum Power Dissipation	Ta = 25°C	P_D	3.0	W
	Ta = 75°C		2.1	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JF}$	24	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	62.5	°C/W

Notes:

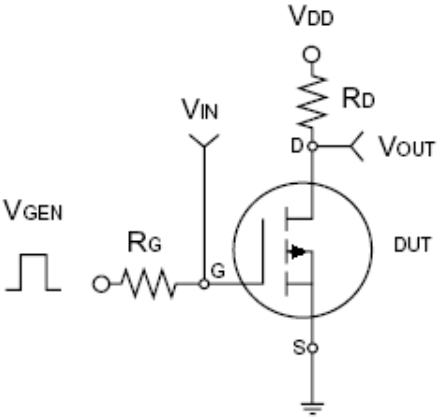
a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 10 sec.

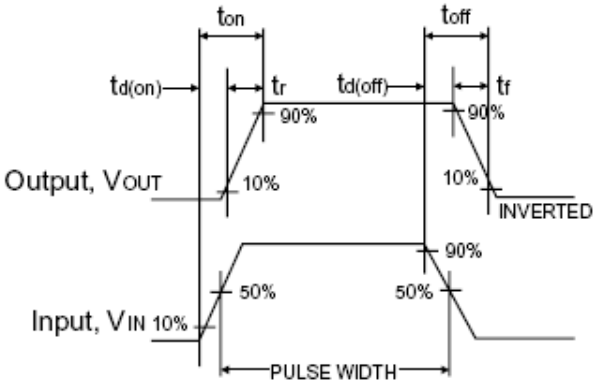
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D =250uA	BV_{DSS}	30	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D =250μA	$V_{GS(TH)}$	0.7	--	1.4	V
Gate Body Leakage	V_{GS} = ±12V, V_{DS} =0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} =0V	I_{DSS}	--	--	1.0	μA
Drain-Source On-State Resistance[a]	V_{GS} = 10V, I_D =8.5A	$R_{DS(ON)}$	--	24	30	mΩ
	V_{GS} = 4.5V, I_D =8.5A		--	27	33	
	V_{GS} = 2.5V, I_D =5A		--	40	48	
Forward Transconductance[a]	V_{DS} = 5V, I_D =5A	g_{fs}	--	16	--	S
Diode Forward Voltage	I_S = 1A, V_{GS} =0V	V_{SD}	--	0.76	1.0	V
Dynamic[b]						
Total Gate Charge	V_{DS} = 15V, I_D = 8.5A, V_{GS} = 4.5V	Q_g	--	9.7	12	nC
Gate-Source Charge		Q_{gs}	--	1.63	--	
Gate-Drain Charge		Q_{gd}	--	3.1	--	
Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	857	1030	pF
Output Capacitance		C_{oss}	--	97	--	
Reverse Transfer Capacitance		C_{rss}	--	71	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = 15V, R_L = 1.8Ω, I_D = 1A, V_{GEN} = 10V, R_G = 6Ω	$t_{d(on)}$	--	3.3	5	nS
Turn-On Rise Time		t_r	--	4.7	7	
Turn-Off Delay Time		$t_{d(off)}$	--	26	39	
Turn-Off Fall Time		t_f	--	4.1	6.2	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



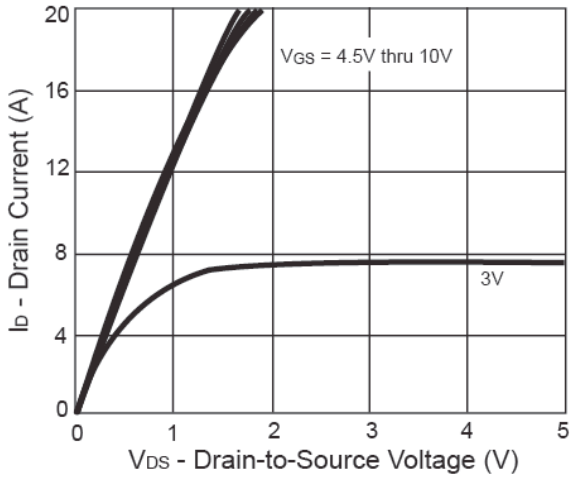
Switching Test Circuit



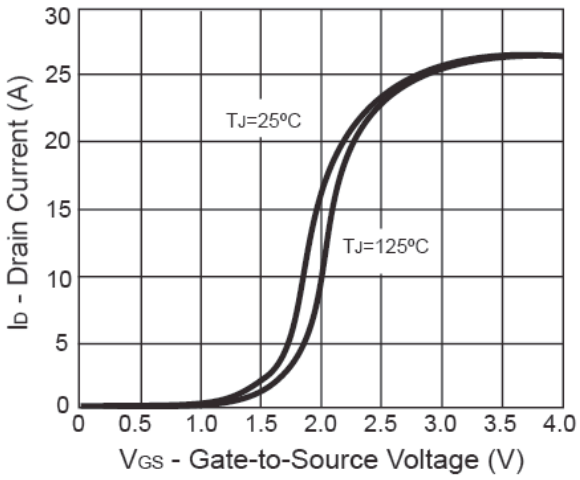
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

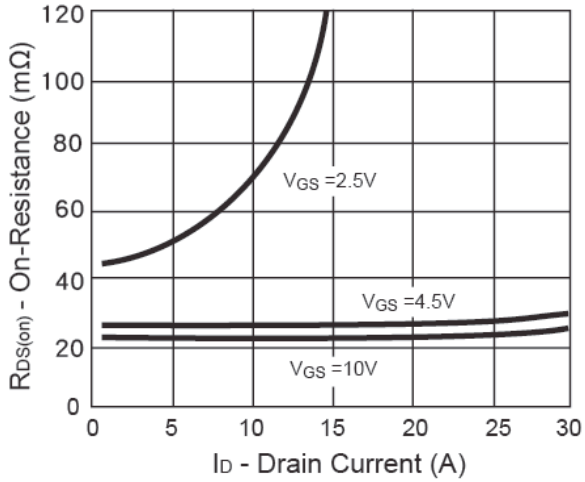
Output Characteristics



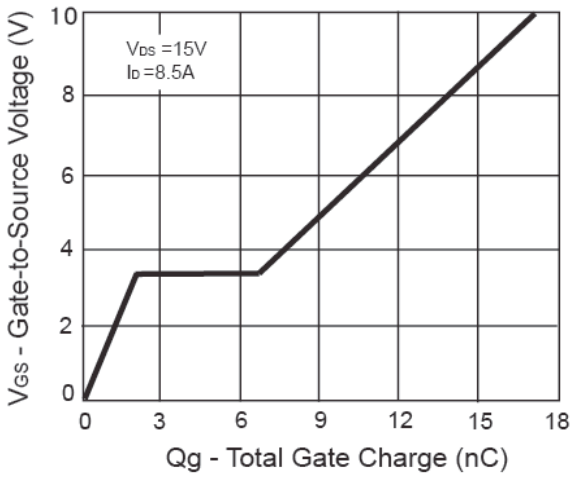
Transfer Characteristics



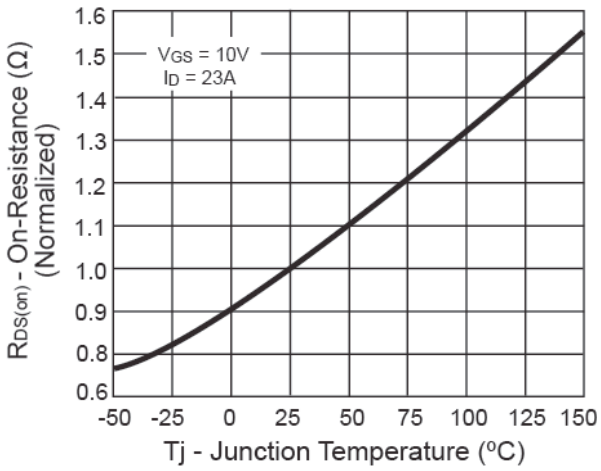
On-Resistance vs. Drain Current



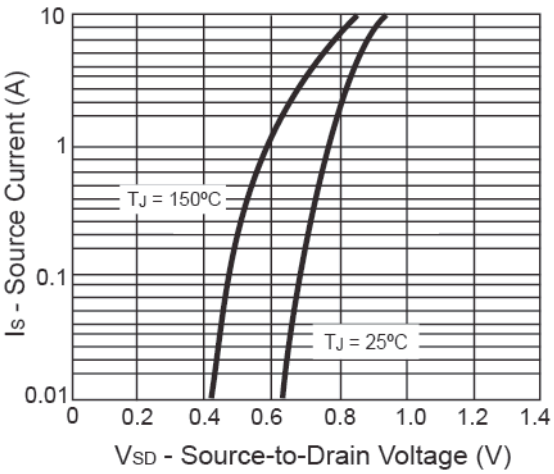
Gate Charge



On-Resistance vs. Junction Temperature

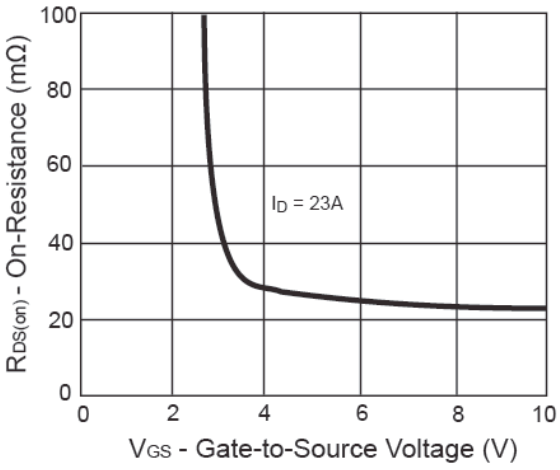


Source-Drain Diode Forward Voltage

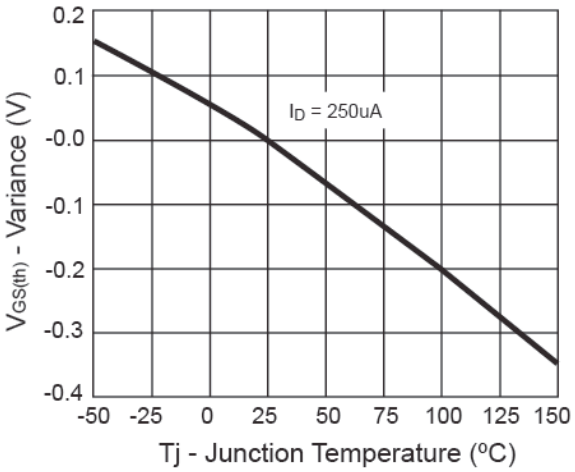


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

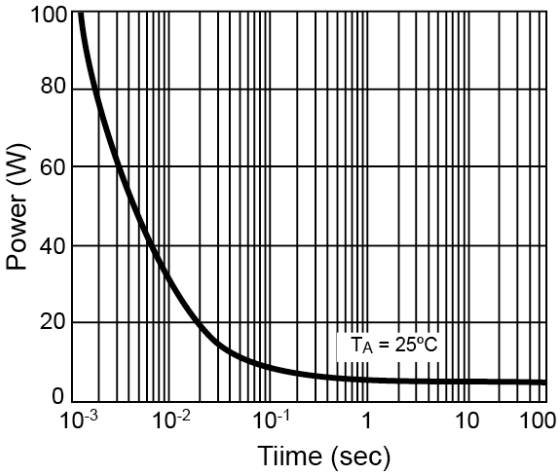
On-Resistance vs. Gate-Source Voltage



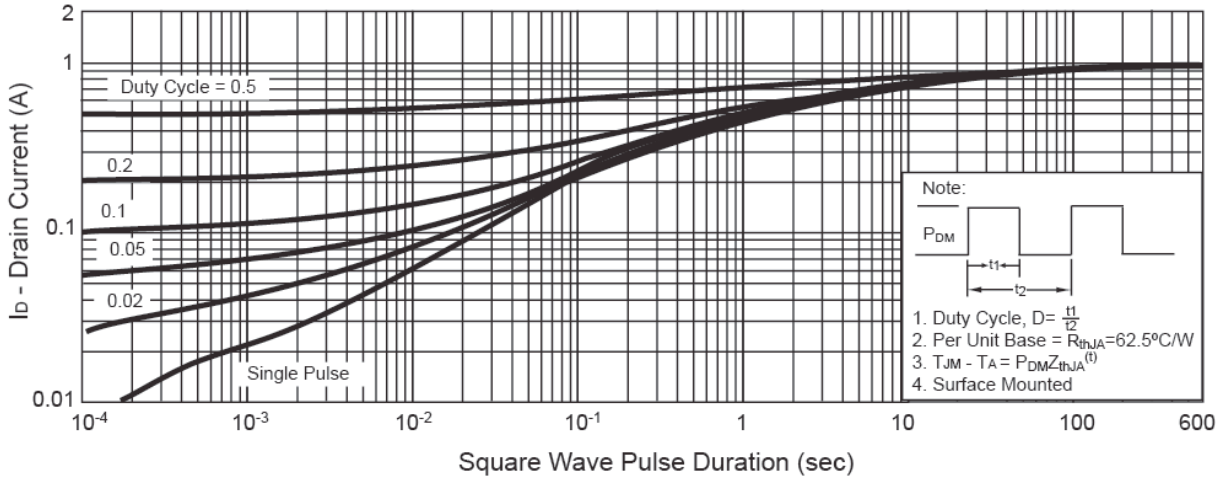
Threshold Voltage



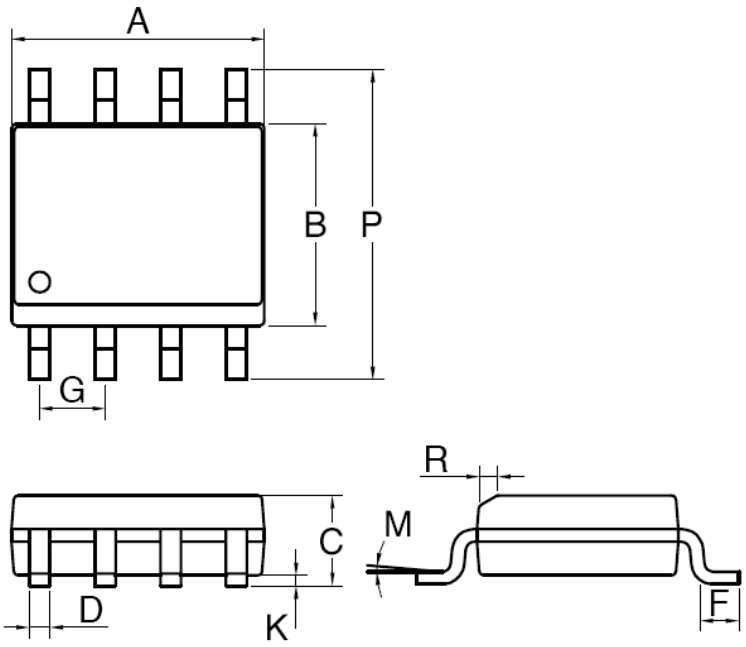
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

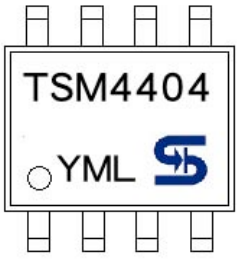


SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0º	7º	0º	7º
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Marking Diagram



Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
L = Lot Code

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