



# TSM4410

www.DataSheet4U.com  
Preliminary

## N-Channel Enhancement Mode MOSFET

SOP-8



Pin assignment:

1. Source
2. Source
3. Source
4. Gate
- 5, 6, 7, 8. Drain

$V_{DS} = 25V$

$I_D = 10A$

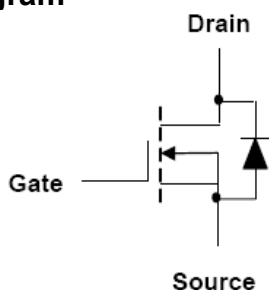
$R_{DS(on)}, V_{GS} @ 10V, I_{DS} @ 10A = 13.5m\Omega$

$R_{DS(on)}, V_{GS} @ 4.5V, I_{DS} @ 8A = 20m\Omega$

### Features

- ✧ Advanced trench process technology
- ✧ High Density Cell Design for Ultra Low On-Resistance
- ✧ Fully Characterized Avalanche Voltage and Current

### Block Diagram



### Ordering Information

Part No.	Packing	Package
TSM4410CS	Tape & Reel (2,500pcs / Reel)	SOP-8

### Absolute Maximum Rating ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	10	A
Pulsed Drain Current	$I_{DM}$	50	
Maximum Power Dissipation	$P_D$	$T_A = 25^\circ C$	2
		$T_A = 70^\circ C$	1.3
Operating Junction Temperature	$T_J$	+150	$^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ C$

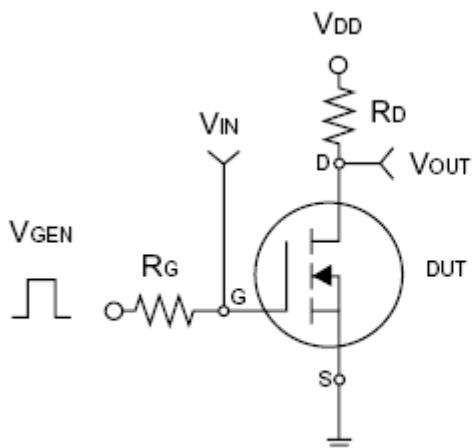
### Thermal Performance

Parameter	Symbol	Limit	Unit
Junction-to-case Thermal Resistance	$R_{\theta jc}$	2.2	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta ja}$	50	

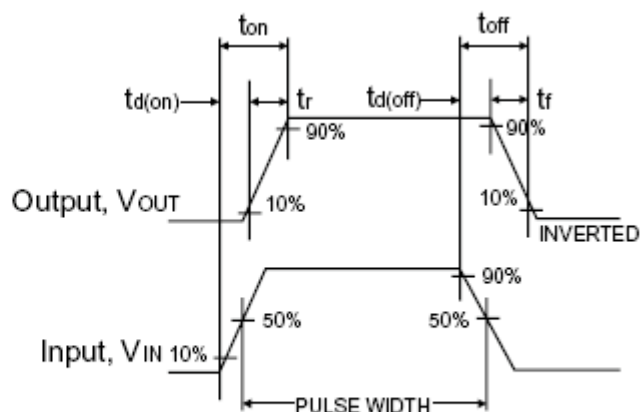
Note: 1. Maximum DC current limited by the package  
 2. 1-in<sup>2</sup> 2oz Cu PCB board

Electrical Characteristics						
$T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	$BV_{DSS}$	25	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 10\text{A}$	$R_{DS(ON)}$	--	11	13.5	m $\Omega$
	$V_{GS} = 4.5\text{V}, I_D = 5\text{A}$	$R_{DS(ON)}$	--	16.5	20	m $\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	1.0	--	3.0	V
Zero Gate Voltage Drain Current	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$	$I_{DSS}$	--	--	1.0	$\mu\text{A}$
Gate Body Leakage	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	$I_{GSS}$	--	--	$\pm 100$	nA
Gate Resistance	$f = 1\text{MHz}$	$R_g$	--	1.35	--	$\Omega$
Forward Transconductance	$V_{DS} = 15\text{V}, I_D = 10\text{A}$	$g_{fs}$	--	25	--	S
<b>Dynamic</b>						
Total Gate Charge	$V_{DS} = 15\text{V}, I_D = 10\text{A}, V_{GS} = 5\text{V}$	$Q_g$	--	7.56	--	nC
Gate-Source Charge		$Q_{gs}$	--	2.74	--	
Gate-Drain Charge		$Q_{gd}$	--	2.22	--	
Turn-On Delay Time	$V_{DD} = 15\text{V}, R_L = 25\Omega, I_D = 1\text{A}, V_{GEN} = 10\text{V}, R_G = 6\Omega$	$t_{d(on)}$	--	6.81	--	nS
Turn-On Rise Time		$t_r$	--	1.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	20.37	--	
Turn-Off Fall Time		$t_f$	--	3.42	--	
Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$	$C_{iss}$	--	1046.7	--	pF
Output Capacitance		$C_{oss}$	--	148.75	--	
Reverse Transfer Capacitance		$C_{rss}$	--	78.26	--	
<b>Source-Drain Diode</b>						
Max. Diode Forward Current		$I_S$	--	--	10	A
Diode Forward Voltage	$I_S = 2.3\text{A}, V_{GS} = 0\text{V}$	$V_{SD}$	--	0.85	1.3	V

Note: 1. pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$   
 2. Negligible, Dominated by circuit inductance.

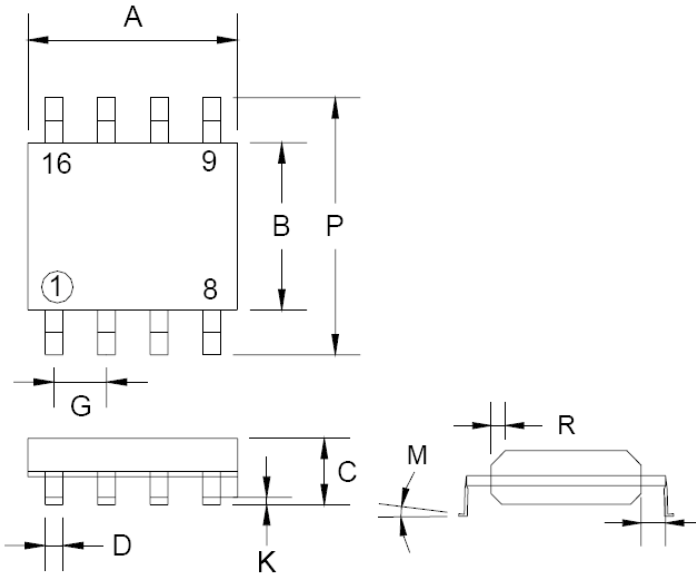


Switching Test Circuit



Switchin Waveforms

### SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 (typ)		0.05 (typ)	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019