N-Channel Power MOSFET

60V, 8A, 36mΩ

FEATURES

- Advance trench process technology
- High density cell design for ultra low on-resistance
- RoHS Compliant
- Halogen-free

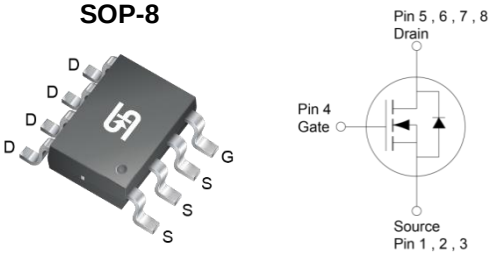
APPLICATIONS

- High-Side DC/DC conversion
- Notebook
- Industrial

KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		60	V
$R_{DS(on)}$ (max)	V_{GS} = 10V	36	mΩ
	V_{GS} = 4.5V	43	
Q_g		10	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C= 25°C	I_D	8	A
Pulsed Drain Current		I_{DM}	25	A
Single Pulse Avalanche Current (Note 1)		I_{AS}	12	A
Single Pulse Avalanche Energy (Note 1)		E_{AS}	22.7	mJ
Total Power Dissipation	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	25	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	50	°C/W

Notes:

Device on a PCB FR4 with 1 in^2 (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	1	1.6	3	V
Gate-Source Leakage Current	V_{GS} = ± 20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V_{DS} = 60V, V_{GS} = 0V	I_{DSS}	--	--	2	μA
Drain-Source On-State Resistance (Note 2)	V_{GS} = 10V, I_D = 4.6A	$R_{DS(on)}$	--	29	36	mΩ
	V_{GS} = 4.5V, I_D = 4.2A		--	33	43	
Forward Transconductance (Note 2)	V_{DS} = 15V, I_D = 4.5A	gfs	--	28	--	S
Dynamic						
Total Gate Charge	V_{DS} = 30V, I_D = 4.6A, V_{GS} = 4.5V	Q_g	--	10	16	nC
Gate-Source Charge		Q_{gs}	--	2.7	--	
Gate-Drain Charge		Q_{gd}	--	4.6	--	
Input Capacitance	V_{DS} = 30V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1216	--	pF
Output Capacitance		C_{oss}	--	59	--	
Reverse Transfer Capacitance		C_{rss}	--	42	--	
Gate Resistance	f = 1.0MHz	Rg	--	1.4	--	Ω
Switching (Note 3)						
Turn-On Delay Time	V_{DD} = 30V, R_G = 1Ω, I_D = 5.6A, V_{GS} = 10V	$t_{d(on)}$	--	6.9	15	ns
Turn-On Rise Time		t_r	--	15	25	
Turn-Off Delay Time		$t_{d(off)}$	--	20	40	
Turn-Off Fall Time		t_f	--	2	15	
Source-Drain Diode						
Forward Voltage (Note 2)	I_S = 2A, V_{GS} = 0V	V_{SD}	--	0.8	1.2	V
Reverse Recovery Time	I_S = 4.6A, dI/dt = 100A/μs	t_{rr}	--	15	--	ns
Reverse Recovery Charge		Q_{rr}	--	12	--	nC

Notes:

1. L = 0.3mH, VGS = 10V, VDD = 30V, RG = 25Ω, Starting TJ = 25°C.
2. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
3. Switching time is essentially independent of operating temperature.

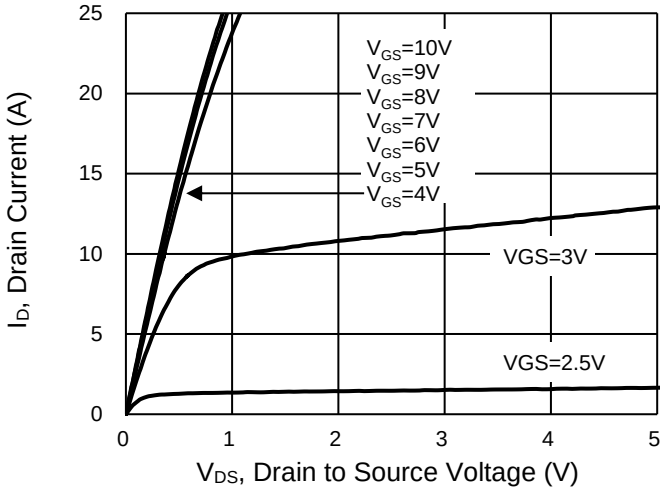
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM4436CS RLG	SOP-8	2500pcs / 13” Reel

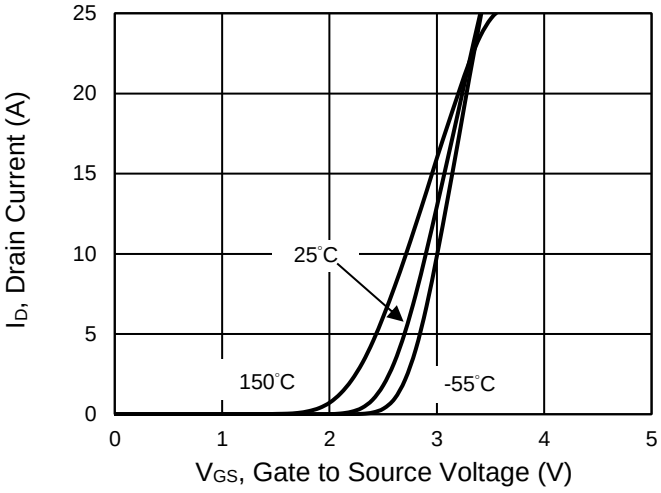
CHARACTERISTICS CURVES (N-Channel)

(T_A = 25°C unless otherwise noted)

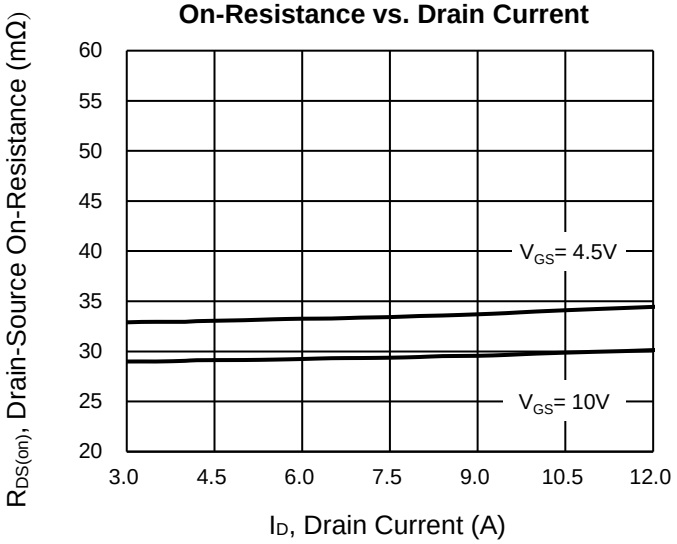
Output Characteristics



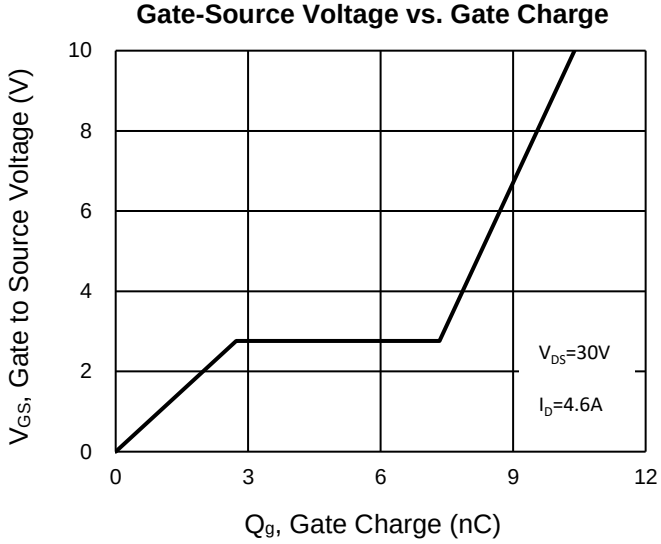
Transfer Characteristics



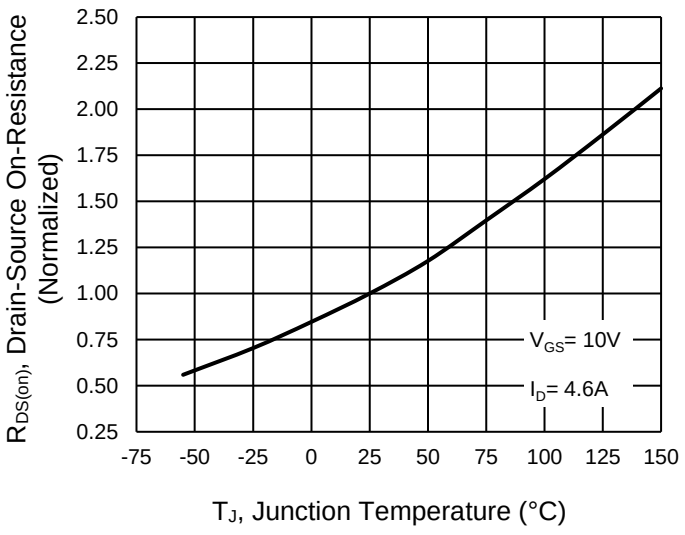
On-Resistance vs. Drain Current



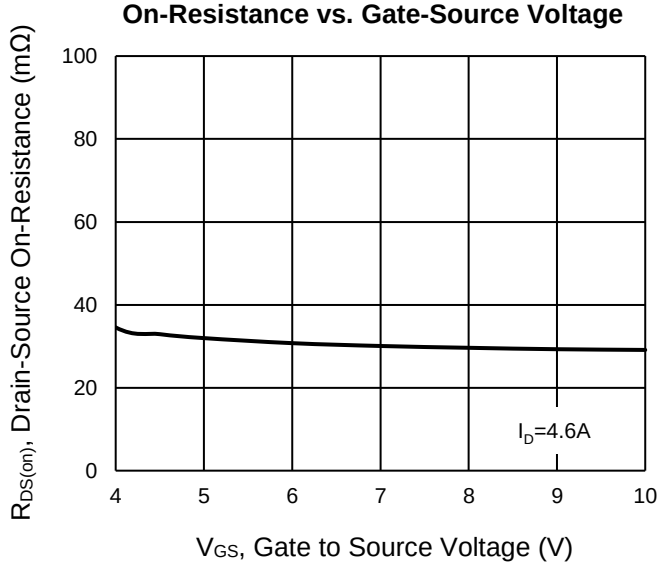
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



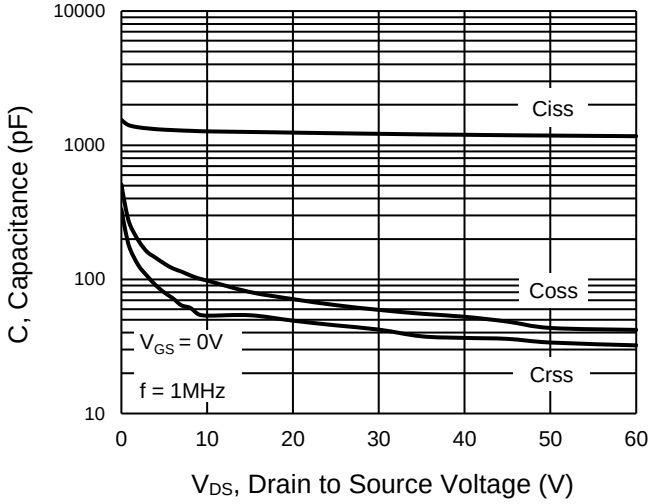
On-Resistance vs. Gate-Source Voltage



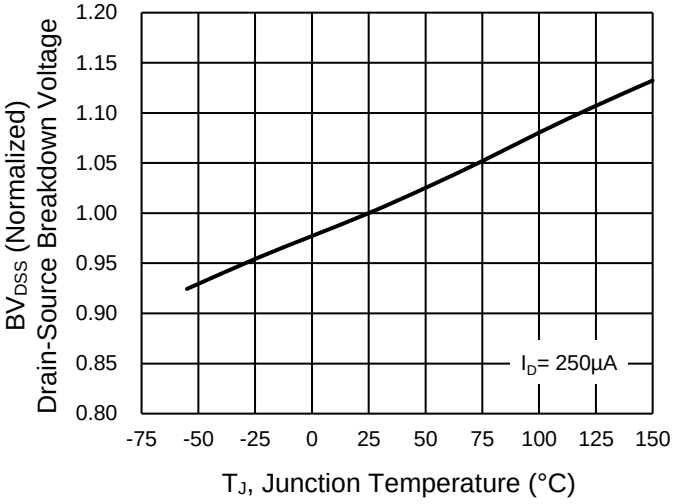
CHARACTERISTICS CURVES (N-Channel)

(T_A = 25°C unless otherwise noted)

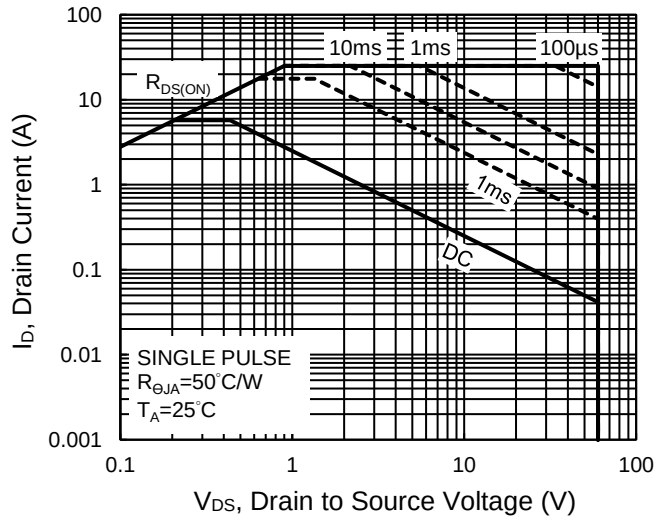
Capacitance vs. Drain-Source Voltage



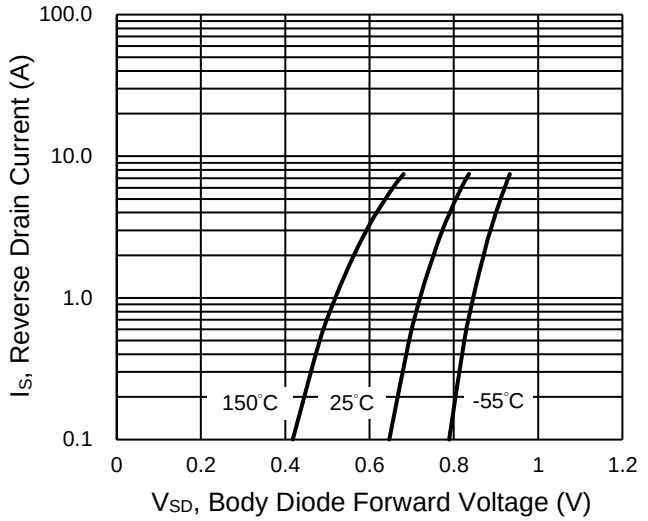
BV_{DSS} vs. Junction Temperature



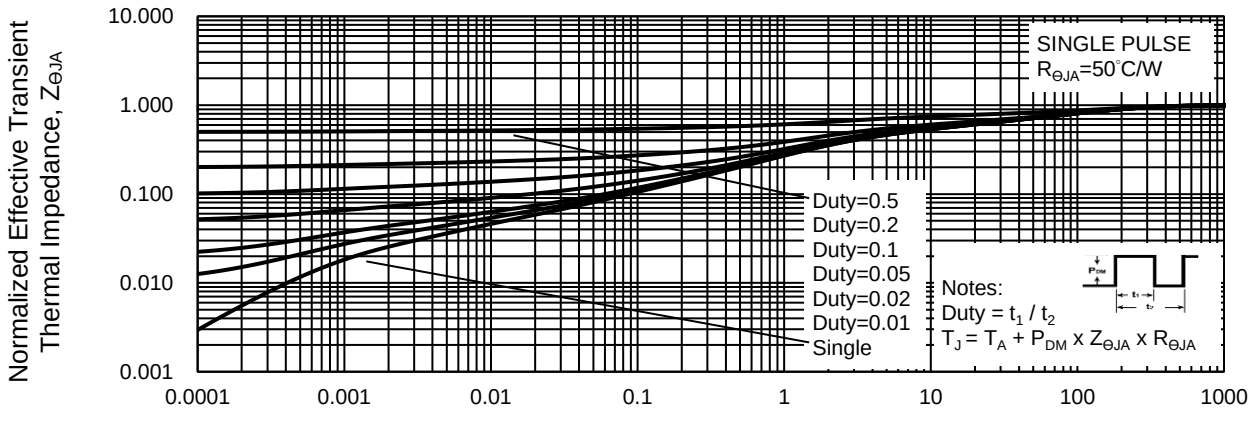
Maximum Safe Operating Area, Junction-to-Ambient



Source-Drain Diode Forward Current vs. Voltage



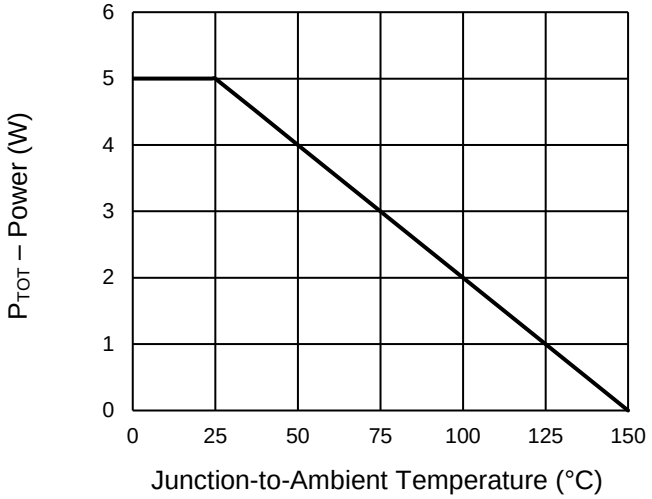
Normalized Thermal Transient Impedance, Junction-to-Ambient



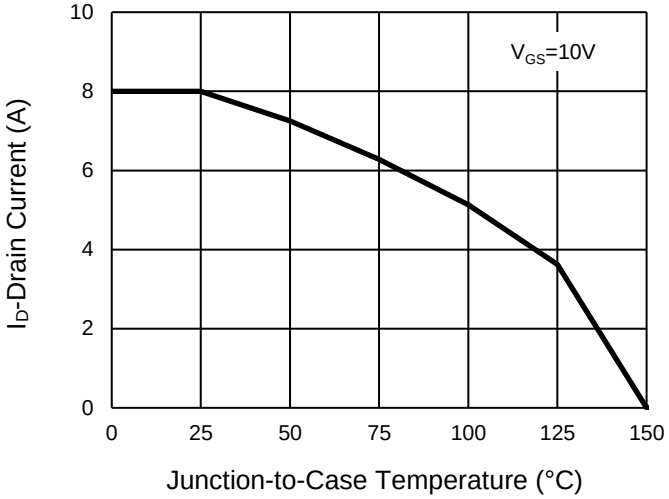
CHARACTERISTICS CURVES (N-Channel)

(T_A = 25°C unless otherwise noted)

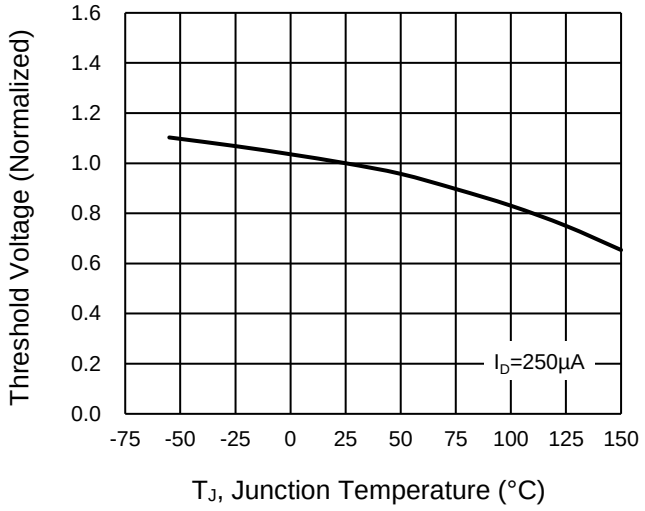
Power Dissipation



Drain Current

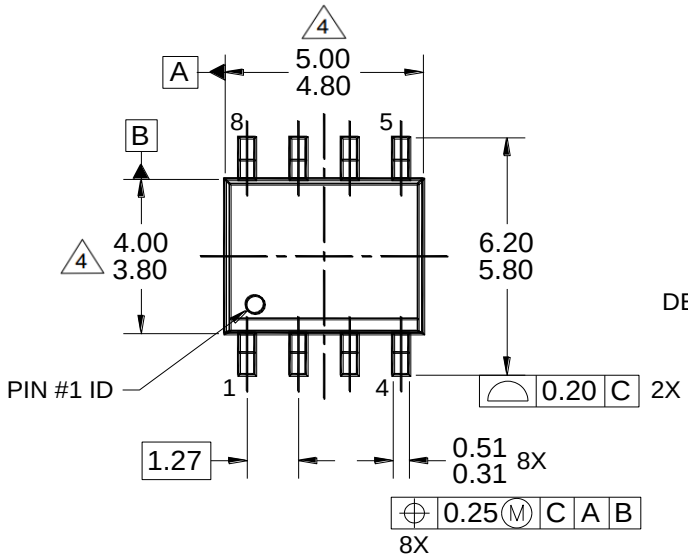


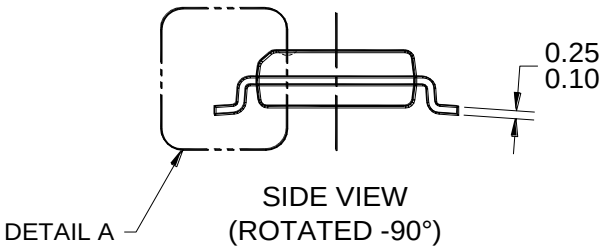
Normalized gate threshold voltage vs Temperature

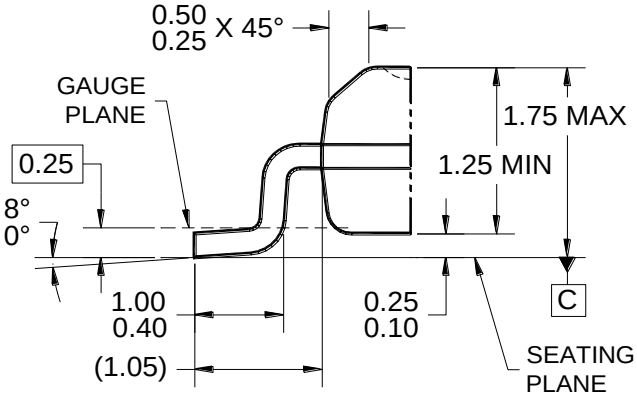


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

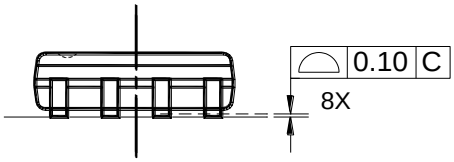
SOP-8

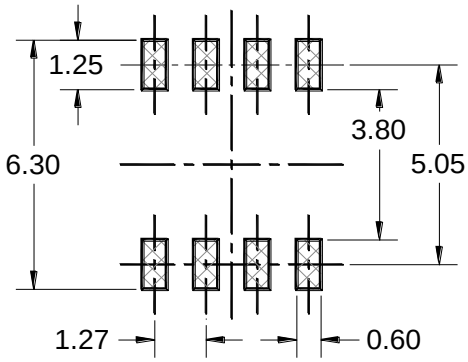




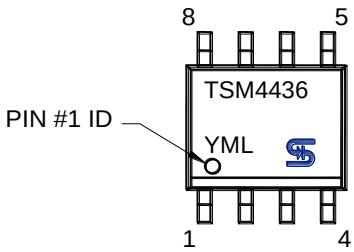


DETAIL A
(SCALE 3:1)





SUGGESTED PAD LAYOUT
(REFERENCE ONLY)



MARKING DIAGRAM

Y = Year Code
M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
S	=May	**T**	=Jun	**U**	=Jul	**V**	=Aug
W	=Sep	**X**	=Oct	**Y**	=Nov	**Z**	=Dec

L = Lot Code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC MS-012, ISSUE G, VARIATION AA.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO REF: HQ2SD07-SOP8STD-028 REV A.

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