



Pin Definition:

- | | |
|-------------|------------|
| 1. Source 1 | 8. Drain 1 |
| 2. Gate 1 | 7. Drain 1 |
| 3. Source 2 | 6. Drain 2 |
| 4. Gate 2 | 5. Drain 2 |

MOSFET PRODUCT SUMMARY

	V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
N-Channel	30	28 @ $V_{GS} = 10V$	6.5
		42 @ $V_{GS} = 4.5V$	5.0
P-Channel	-30	65 @ $V_{GS} = -10V$	-4.2
		90 @ $V_{GS} = -4.5V$	-3.5

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

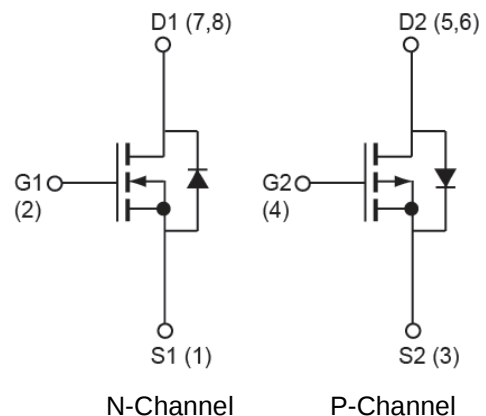
- Load Switch
- PA Switch

Ordering Information

Part No.	Package	Packing
TSM4539DCS RLG	SOP-8	2.5Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

Block Diagram



MOSFET Absolute Maximum Rating ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	N-CH Limit	P-CH Limit	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current, V_{GS}	I_D	6.5	-4.2	A
Pulsed Drain Current,	I_{DM}	28	-20	A
Drain-Source Diode Forward Current	I_S	2.5	-1.9	A
Power Dissipation @ $T_a = 25^\circ C$	P_D	2.1	2.1	W
Operating Junction Temperature	T_J	150		$^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150		$^\circ C$

Thermal Performance

Parameter	Symbol	N-CH Limit	P-CH Limit	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62.5	62.5	$^\circ C/W$
Junction to Lead Thermal Resistance	$R_{\theta JL}$	40	40	$^\circ C/W$

Notes:

- Pulse width limited by the Maximum junction temperature
- Surface Mounted on FR4 Board using 1 inch sq pad size, $t \leq 5sec$.
- Surge Applied at Rated Load Conditions, Half-Wave, Single Phase, 60Hz.

Electrical Specifications ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

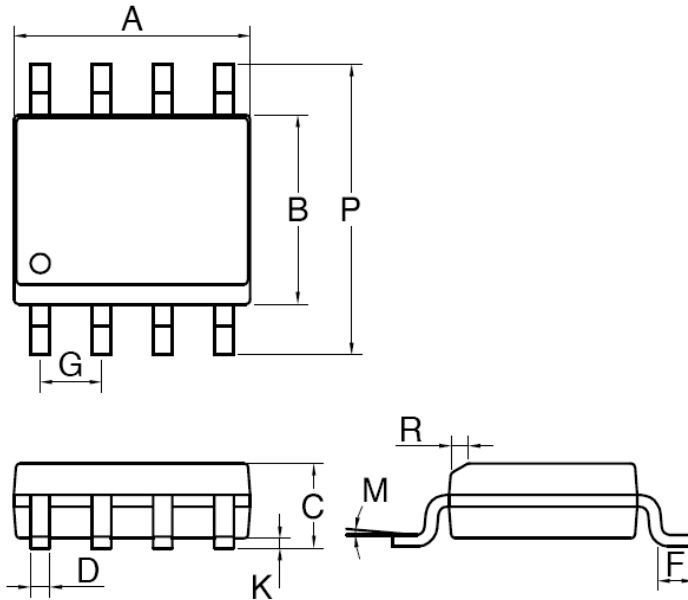
Parameter	Conditions	Symbol	Min	Typ	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = 250uA	BV _{DSS}	N-CH	30	--	--	V
	V _{GS} =0V, I _D =-250uA		P-CH	-30	--	--	
Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = 250μA	V _{GS(TH)}	N-CH	1.0	1.4	3.0	V
	V _{DS} =V _{GS} , I _D =-250μA		P-CH	-1.0	-1.5	-3.0	
Gate Body Leakage	V _{GS} = ±20V, V _{DS} =0V	I _{GSS}	N-CH	--	--	±100	nA
	V _{GS} = ±20V, V _{DS} =0V		P-CH	--	--	±10	
Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V	I _{DSS}	N-CH	--	--	1	μA
	V _{DS} =-24V, V _{GS} =0V		P-CH	--	--	-1	
Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D =6.5A	R _{DS(ON)}	N-CH	--	23	28	mΩ
	V _{GS} =-10V, I _D =-4.2A		P-CH	--	50	65	
	V _{GS} =4.5V, I _D =5A		N-CH	--	35	42	
	V _{GS} =-4.5V, I _D =-3.5A		P-CH		82	90	
Dynamic ^b							
Total Gate Charge	N-Channel V _{DS} =10V, I _D =1A, V _{GS} =10V	Q _g	N-CH	--	7	--	nC
			P-CH	--	9.7	--	
Gate-Source Charge	P-Channel V _{DS} =-15V, I _D =-5.2A, V _{GS} =-10V	Q _{gs}	N-CH	--	1.6	--	
			P-CH	--	1.6	--	
Gate-Drain Charge		Q _{gd}	N-CH	--	1.0	--	
			P-CH	--	1.3	--	
Input Capacitance	N-Channel V _{DS} =15V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	N-CH	--	610	--	pF
			P-CH	--	100	--	
Output Capacitance	P-Channel V _{DS} =-15V, V _{GS} = 0V, f = 1.0MHz	C _{oss}	N-CH	--	77	--	
			P-CH	--	551	--	
Reverse Transfer Capacitance		C _{rss}	N-CH	--	90	--	
			P-CH	--	60	--	
Switching ^b							
Turn-On Delay Time	N-Channel V _{DD} =15V, I _D = 1A, V _{GEN} =10V, R _G = 6Ω	t _{d(on)}	N-CH	--	7	--	nS
			P-CH	--	6.2	--	
Turn-On Rise Time		t _r	N-CH	--	10	--	
			P-CH	--	6.2	--	
Turn-Off Delay Time	P-Channel V _{DD} =-15V, I _D = -1A, V _{GEN} =-10V, R _G = 6Ω	t _{d(off)}	N-CH	--	16	--	
			P-CH	--	26	--	
Turn-Off Fall Time		t _f	N-CH	--	7	--	
			P-CH	--	5.5	--	
Diode Forward Voltage	I _S =1 A, V _{GS} = 0V	V _{SD}	N-CH	--	--	1.0	V
	I _S =-1.9A, V _{GS} = 0V		P-CH	--	--	-1.3	

Notes:

a. Pulse test: $PW \leq 300\mu\text{S}$, duty cycle $\leq 2\%$

b. For DESIGN AID ONLY, not subject to production testing.

SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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